

**LMN1073KX7F 20V N-Channel Enhancement Mode MOSFET**
**Features**

- 20V/0.5A,  $R_{DS(ON)}=300m\Omega@V_{GS}=4.5V$
- 20V/0.4A,  $R_{DS(ON)}=450m\Omega@V_{GS}=2.5V$
- 20V/0.2A,  $R_{DS(ON)}=800m\Omega@V_{GS}=1.8V$
- 20V/0.1A,  $R_{DS(ON)}=1200m\Omega@V_{GS}=1.5V$
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Battery Voltage Operation
- ESD Protected
- SOT-523 package design

**Product Description**

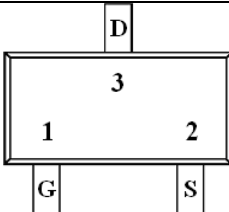
LMN1072 KX7F, N-Channel enhancement mode MOSFET, uses Advanced Trench

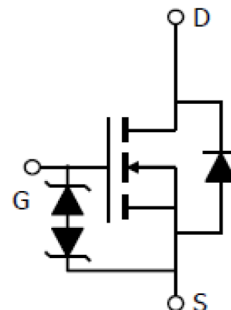
Technology to provide excellent  $R_{DS(ON)}$ , low gate charge. These devices are particularly suited for low voltage power management, such as smart phone and notebook computer, and low in-line power loss are needed in commercial industrial surface mount applications.

**Applications**

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Smart Phones, Pagers

**Pin Configuration**

LMN1072 KX5F (SOT-523)	
	
PIN	Description
1	Gate
2	Source
3	Drain



**Ordering Information**

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMN1072KX7F	LMN1072K	X7	F	SOT-523	3000 PCS

**Marking Information**

Marking Information		
Part Marking	Part Number	LFC code
2W	2	WM

**Absolute Maximum Ratings**

(T<sub>C</sub>=25°C Unless otherwise noted)

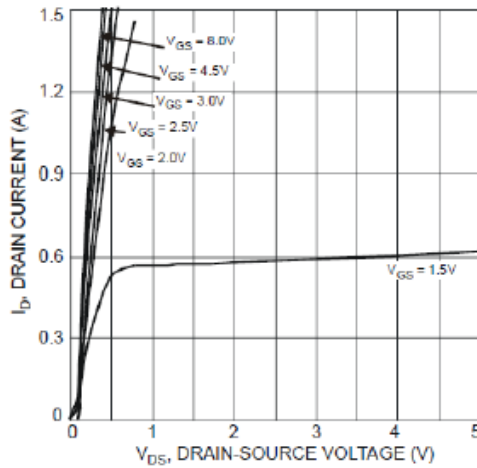
Symbol	Parameter	Typical	Unit
V <sub>DSS</sub>	Drain-Source Voltage	20	V
V <sub>GSS</sub>	Gate-Source Voltage	±10	V
I <sub>D</sub>	Continuous Drain Current	T <sub>A</sub> =25°C	A
		T <sub>A</sub> =70°C	
I <sub>DM</sub>	Pulsed Drain Current	1	A
I <sub>S</sub>	Continuous Source Current (Diode Conduction)	0.3	A
P <sub>D</sub>	Power Dissipation	T <sub>A</sub> =25°C	W
		T <sub>A</sub> =70°C	
T <sub>J</sub>	Operating Junction Temperature	-55 to +150	°C
T <sub>STG</sub>	Storage Temperature Range	-55 to +150	°C
R <sub>θJA</sub>	Thermal Resistance-Junction to Ambient	463	°C/W

**Electrical Characteristics**

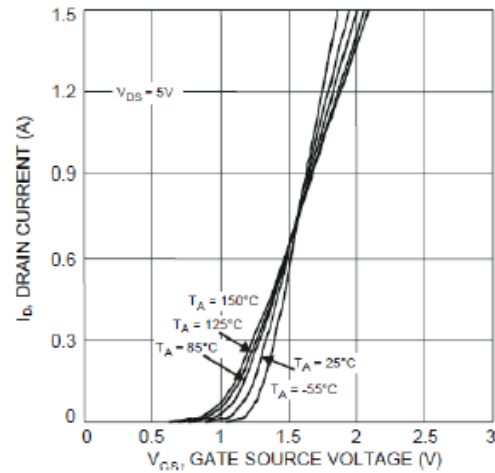
(T<sub>C</sub>=25°C Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	20			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , ID=250uA	0.3		1	
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±10V			±10	uA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =16V, V <sub>GS</sub> =0V			1	uA
		V <sub>DS</sub> =16V, V <sub>GS</sub> =0V T <sub>J</sub> =85°C			30	
R <sub>DS(on)</sub>	Drain-Source On-Resistance	V <sub>GS</sub> =4.5V, I <sub>D</sub> =0.5A		210	300	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =0.4A		285	450	
		V <sub>GS</sub> =1.8V, I <sub>D</sub> =0.2A		430	800	
		V <sub>GS</sub> =1.5V, I <sub>D</sub> =0.1A		710	1200	
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =0.4A			1.2	S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =0.5A, V <sub>GS</sub> =0V			1.3	V
Dynamic						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =10V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =0.25A		0.73		nC
Q <sub>gs</sub>	Gate-Source Charge			0.93		
Q <sub>gd</sub>	Gate-Drain Charge			0.12		
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =16V, V <sub>GS</sub> =0V, f=1MHz		60.7		pF
C <sub>oss</sub>	Output Capacitance			9.7		
C <sub>rss</sub>	Reverse Transfer Capacitance			5.4		
t <sub>d(on)</sub>	Turn-On Time	V <sub>DD</sub> =10V, R <sub>L</sub> =47Ω, I <sub>D</sub> =0.2A, V <sub>GS</sub> =4.5V, R <sub>G</sub> =10Ω		5.1		ns
t <sub>r</sub>				7.4		
t <sub>d(off)</sub>	Turn-Off Time			26.7		
t <sub>f</sub>				12.3		

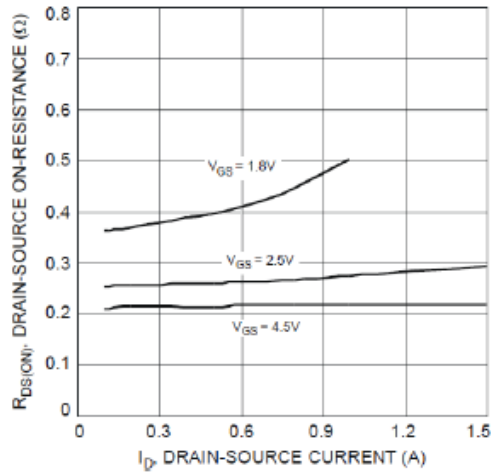
## Typical Performance Characteristics



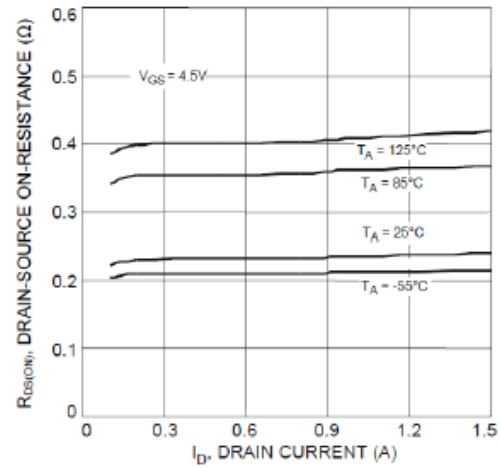
**Fig. 1 Typical Output Characteristics**



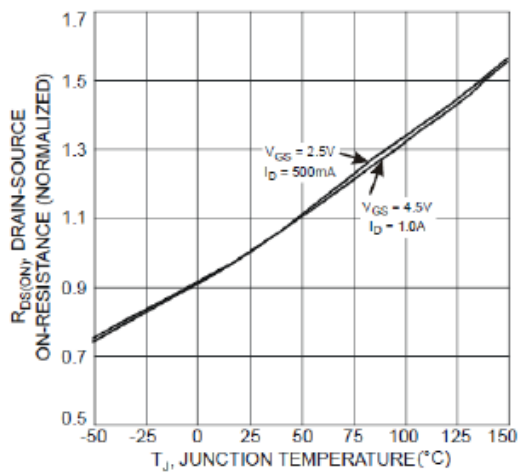
**Fig. 2 Typical Transfer Characteristics**



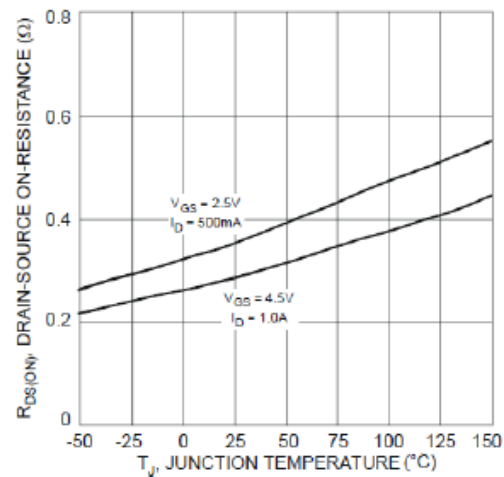
**Fig. 3 Typical On-Resistance vs.  $I_D$  and  $V_{GS}$**



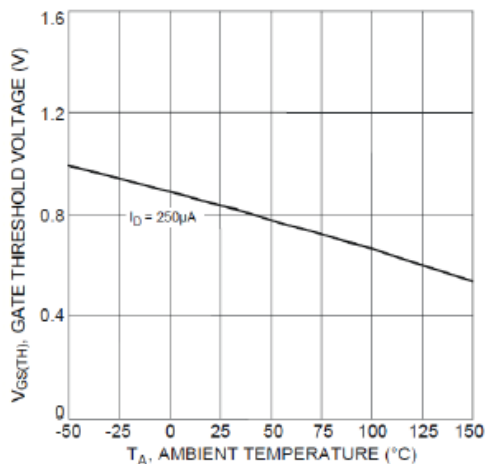
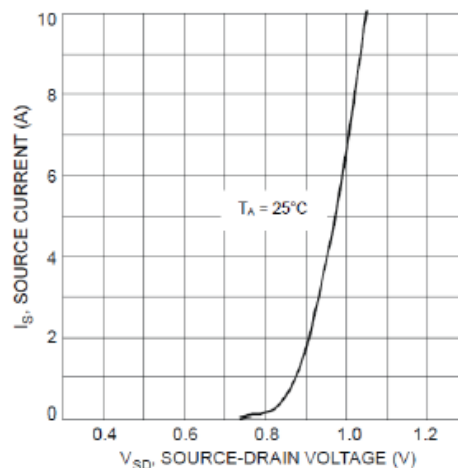
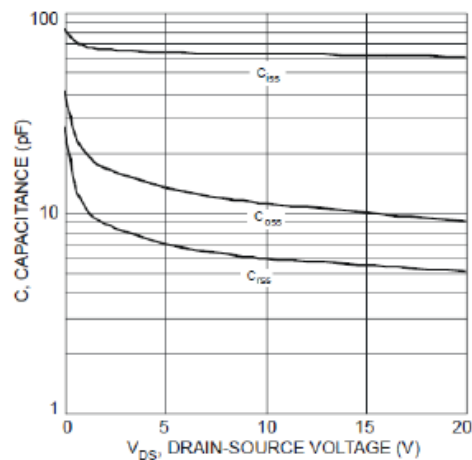
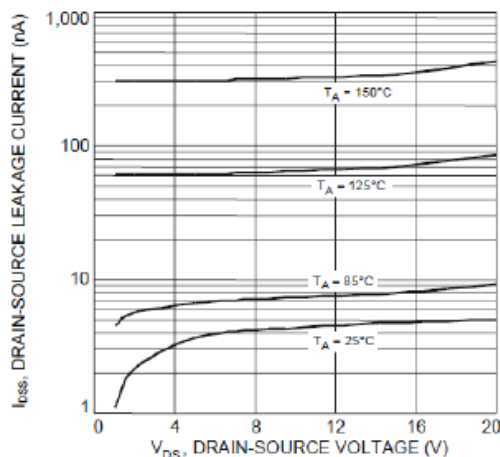
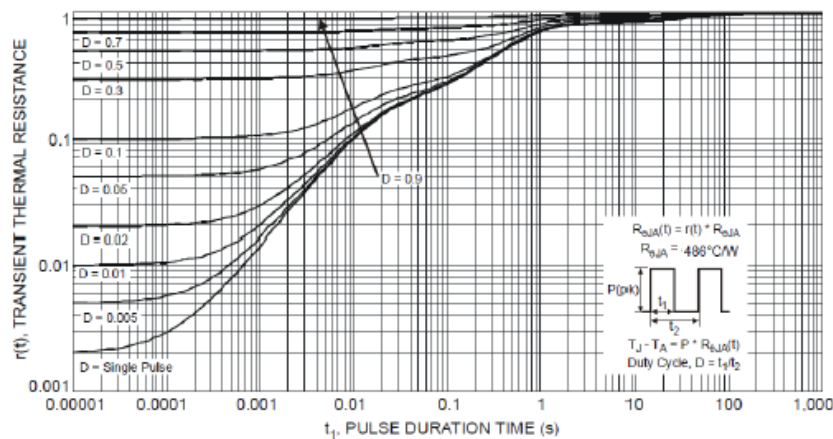
**Fig. 4 Typical Drain-Source On-Resistance vs.  $I_D$  and  $T_J$**



**Fig. 5 On-Resistance Variation with  $T_J$**

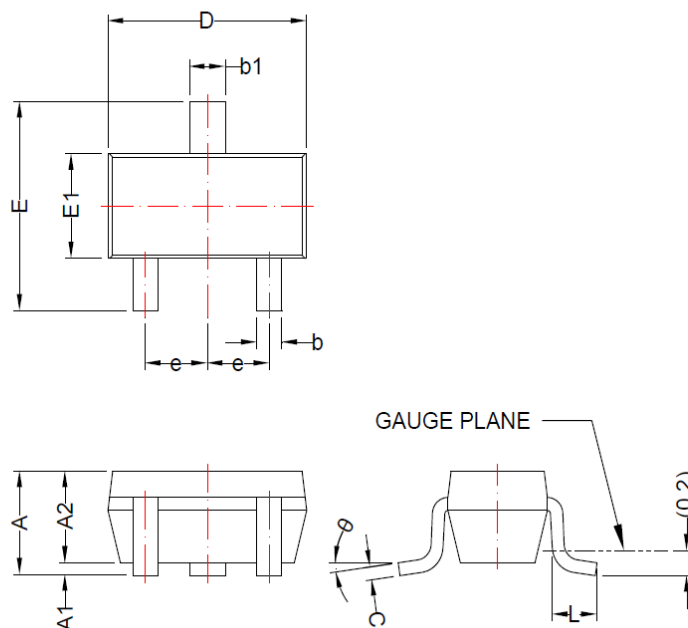


**Fig. 6 On-Resistance Variation with  $T_J$**

**Typical Performance Characteristics(continue)**

**Fig. 7 Gate Threshold Variation vs.  $T_A$** 

**Fig. 8 Diode Forward Voltage vs. Current**

**Fig. 9 Typical Capacitance**

**Fig. 10 Typical Drain-Source Leakage Current vs. Drain-Source Voltage**

**Fig. 11 Transient Thermal Response**

**Package Dimension:**

# **SOT-523**



Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
<b>A</b>	0.60	0.95	0.024	0.037
<b>A1</b>	0.00	0.10	0.000	0.004
<b>A2</b>	0.60	0.85	0.024	0.033
<b>b</b>	0.15	0.30	0.006	0.012
<b>b1</b>	0.25	0.40	0.010	0.016
<b>c</b>	0.08	0.25	0.003	0.010
<b>D</b>	1.40	1.80	0.055	0.071
<b>E</b>	1.40	1.80	0.055	0.071
<b>E1</b>	0.70	0.90	0.028	0.035
<b>e</b>	0.50BSC		0.020BSC	
<b>L</b>	0.26	0.46	0.010	0.018
<b><math>\theta</math></b>	0°	8°	0°	8°

**NOTICE:**

LFC Semiconductor assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all LFC Semiconductor products described or contained herein. LFC Semiconductor products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

Applications shown on the herein document are examples of standard use and operation. Customers are responsible in comprehending the suitable use in particular applications. LFC Semiconductor makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Information furnished is believed to be accurate and reliable. However LFC Semiconductor assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties, which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of LFC Semiconductor. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information without express written approval of LFC Semiconductor.