LMN22N10DF 100V N-Channel MOSFET

Features

- 100V,40A, $R_{DS(ON)}$ =24mΩ@V_{GS} = 10V
- Improved dv/dt capability
- Fast switching
- 100% EAS guaranteed
- Green Device Available
- TO-252-2L package design

These devices are well suited for high efficiency fast switching applications.

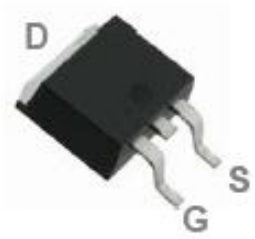
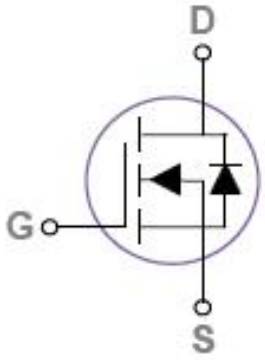
Product Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Applications

- Networking
- Load Switch
- LED applications

Pin Configuration

LMN22N10DF (TO-252-2L)	
	
Description	
Gate	
Source	
Drain	

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Ordering Information

Part Number	P/N	PKG Code	Pb Free Code	Package	Quantity Reel
LMN22N10DF	LMN22N10	D	F	TO-252-2L	2500 pcs

Marking Information

Part Marking	Part Number	LFC code
22N10D XWMMMM	22N10D	XWMMMM

Absolute Maximum Ratings

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DS}	Drain-Source Voltage		100	V
V_{GS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current[1]	T_C=25ºC	40	A
		T_C=70ºC	22	
I_{DM}	Pulsed Drain Current[2]		75	A
EAS	Single Pulse Avalanche Energy[3]		81	mJ
I_{AS}	Single Pulse Avalanche Current		18	A
P_D	Power Dissipation T_C=25ºC		62.5	W
T_J	Operating Junction Temperature Range		-50 to +150	ºC
T_{STG}	Storage Temperature Range		-50 to +150	ºC
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		50	ºC/W
$R_{\theta JC}$	Thermal Resistance-Junction to Case		2	ºC/W

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Electrical Characteristics

(T_J=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	100			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	2	3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V			1	uA
I_S	Continuous Source Current	V_G=V_D=0V, Force Current			40	A
$R_{DS(on)}$	Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=25A		18	24	mΩ
		V_{GS}=4.5V, I_D=6A		19	38	
g_{FS}	Forward Transconductance	V_{DS}=10V, I_D=3A		14		S
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_S=1A			1	V
Dynamic						
C_{iss}	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		4708		pF
C_{oss}	Output Capacitance			326		
C_{rss}	Reverse Transfer Capacitance			247		
R_g	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		1.6		Ω
Q_g	Total Gate Charge	V_{DS}=80V, V_{GS}=10V, I_D=20A		36		nC
Q_{gs}	Gate-Source Charge			5		
Q_{gd}	Gate-Drain Charge			10		
$t_{d(on)}$	Turn-On Time	V_{DD}=40V, I_D=20A, V_{GS}=10V, R_G=3.3Ω		11.5		ns
T_r				29		
$t_{d(off)}$	Turn-Off Time			42		
T_f				18		

Note:
1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The EAS data shows Max. rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.5mH, I_D=18A.

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Typical Performance Characteristics

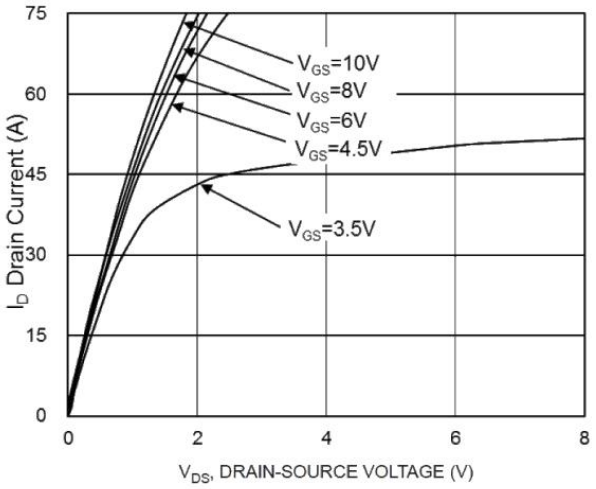

Fig.1 Typical Output Characteristics

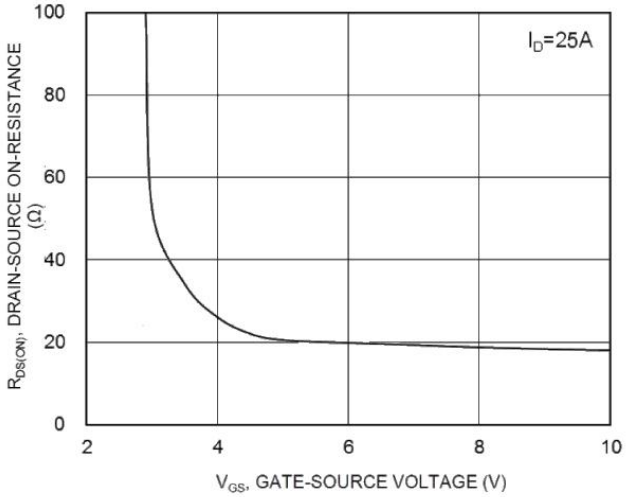

Fig.2 Typical Transfer Characteristics

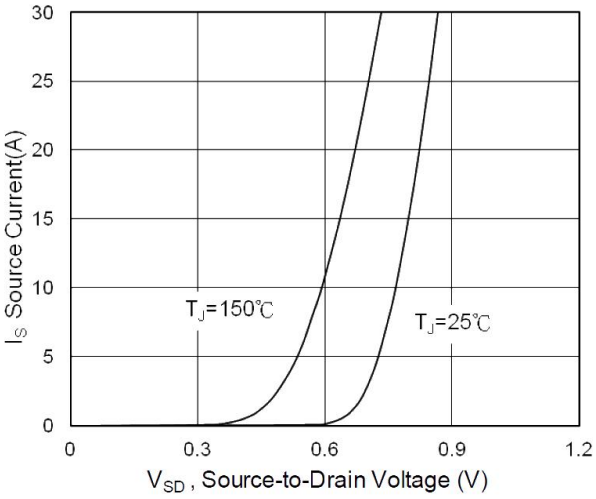

Fig.3 Diode Forward Voltage vs. Current

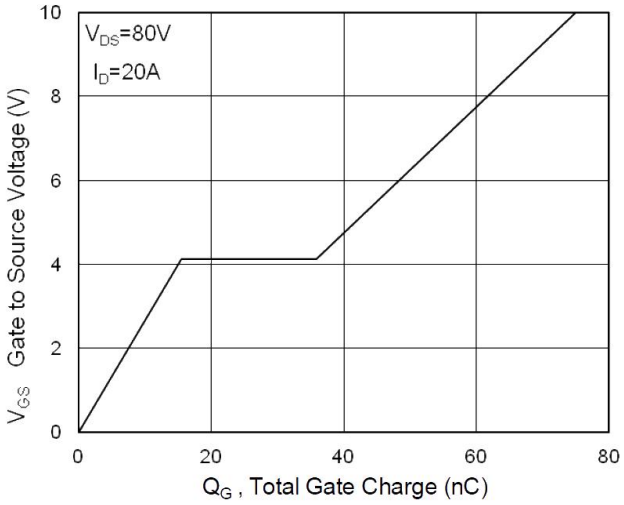

Fig.4 Gate Charge

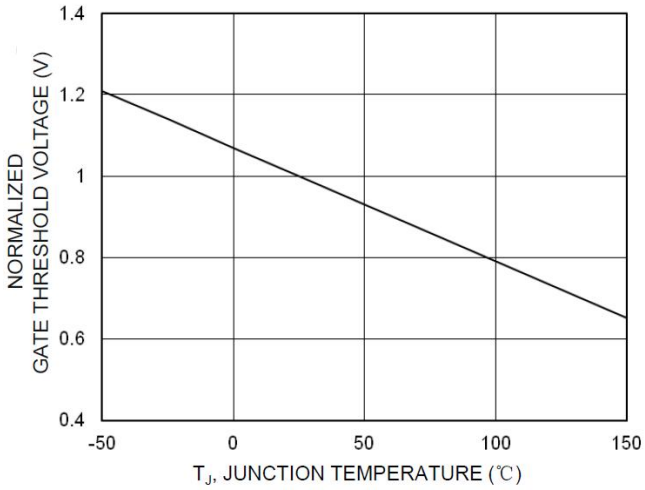

Fig.5 Gate Threshold Variation vs. T_J

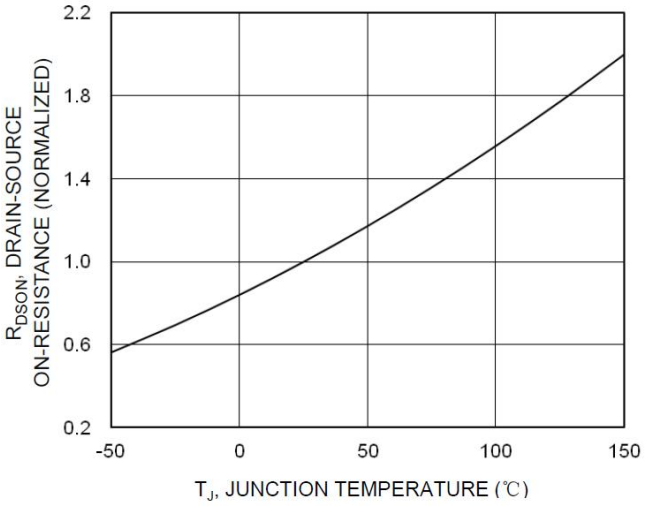

Fig.6 On-Resistance Variation with T_J

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Typical Performance Characteristics (continue.)

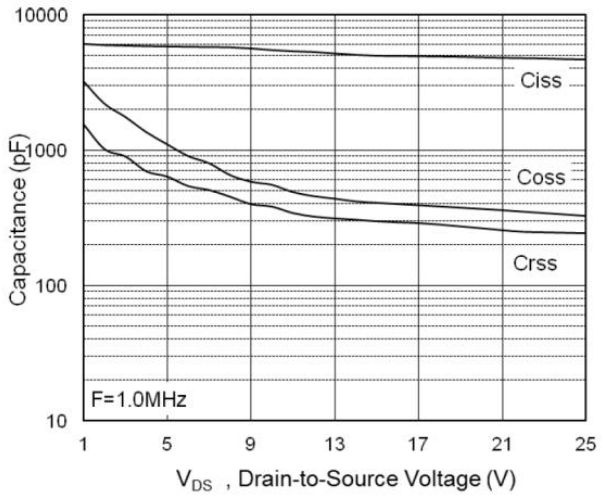

Fig.7 Typical Capacitance

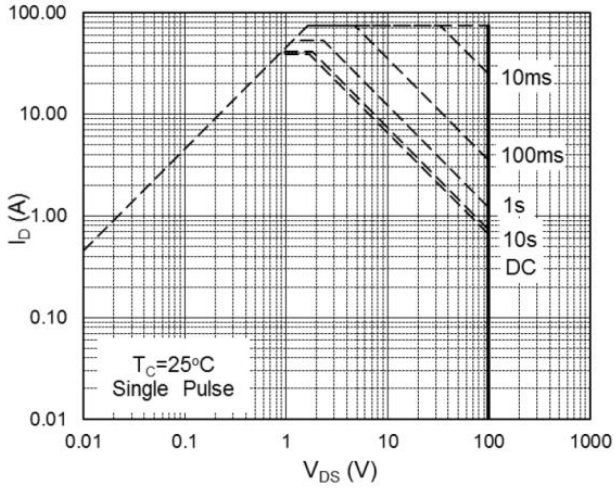

Fig.8 Safe Operating Area

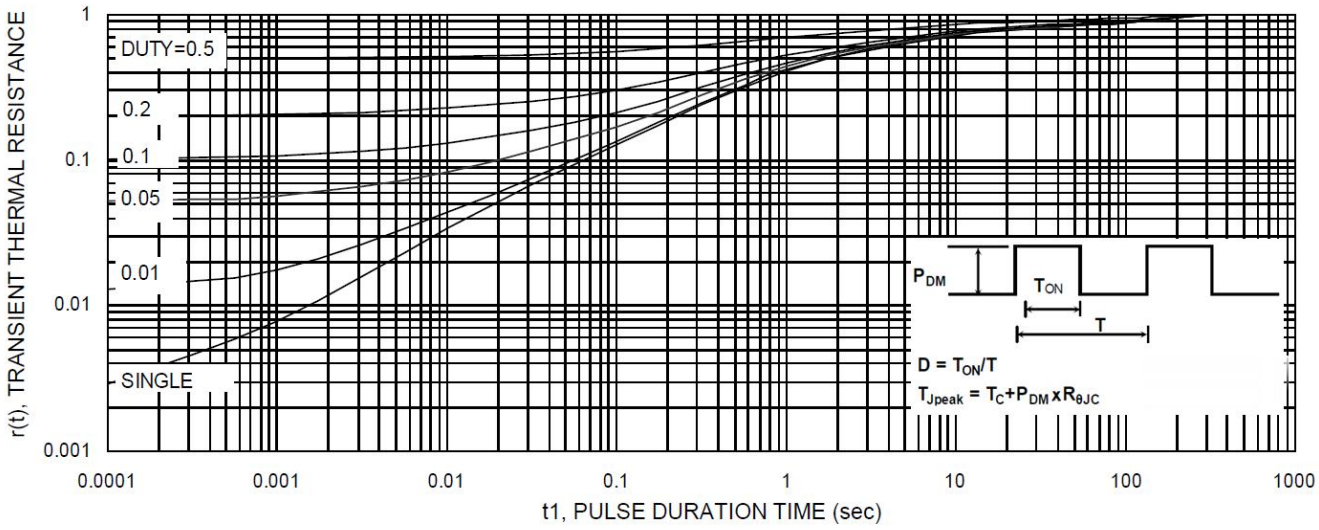

Fig.9 Transient Thermal Response

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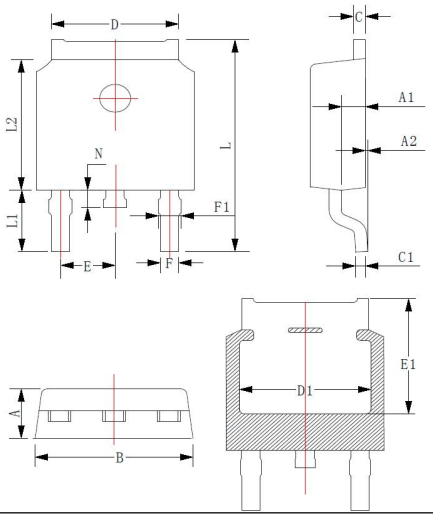
Package Dimension

TO-252-2L



Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.910	1.110	0.036	0.043
A2	-	0.250	-	0.010
B	6.500	6.700	0.256	0.264
C	0.400	0.600	0.016	0.023
C1	0.400	0.600	0.016	0.023
D	5.150	5.450	0.203	0.214
D1	5.100	5.400	0.200	0.212
E	2.200	2.400	0.087	0.094
E1	4.950	5.350	0.195	0.210
F	0.660	0.860	0.026	0.034
F1	0.700	0.950	0.028	0.037
L	9.700	10.100	0.382	0.397
L1	2.670	3.070	0.105	0.121
L2	6.000	6.200	0.236	0.244
N	0.600	1.000	0.024	0.039

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