LMN22N10SF 100V N-Channel Enhancement Mode MOSFET

Features

- $R_{DS(ON)}$ = 22mΩ@V_{GS} = 10V
- $R_{DS(ON)}$ = 32mΩ@V_{GS} = 4.5V
- Improved dv/dt capability
- Fast switching
- Green Device Available
- SOP-8 package design

These devices are well suited for high efficiency fast switching applications.

Product Description

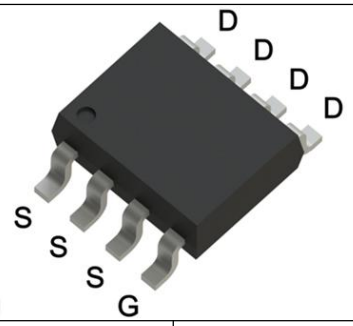
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Applications

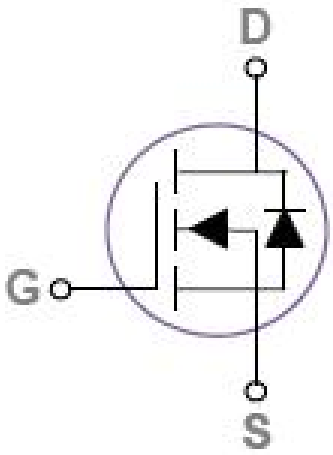
- Networking
- Load Switch
- LED applications

Pin Configuration

LMN22N10SF (SOP-8)



Pin	Description
1	Source
2	Source
3	Source
4	Gate
5	Drain
6	Drain
7	Drain
8	Drain



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Ordering Information

Part Number	P/N	PKG Code	Pb Free Code	Package	Quantity Reel
LMN22N10SF	LMN22N10	S	F	SOP-8	4000 pcs

Marking Information

Part Marking	Part Number	LFC code
22N10S XWMMMM	22N10S	XWMMMM

Absolute Maximum Ratings

(T_A=25ºC Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DS}	Drain-Source Voltage		100	V
V_{GS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current[1]	T_A=25ºC	7.3	A
		T_A=70ºC	5.8	
I_{DM}	Pulsed Drain Current[2]		12	A
P_D	Total Power Dissipation[3]	T_A=25ºC	2.5	W
		T_A=70ºC	1.6	
T_J	Operating Junction Temperature Range		-50 to +150	ºC
T_{STG}	Storage Temperature Range		-50 to +150	ºC
$R_{\theta JC}$	Thermal Resistance-Junction to Case[1]		50	ºC/W

Note:
1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2oz copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The power dissipation is limited by 150ºC junction temperature.

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Electrical Characteristics

(T_A=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	100			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	2	3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V			1	uA
I_S	Continuous Source Current	V_G=V_D=0V, Force Current			7.3	A
I_{SM}	Pulsed Source Current				30	
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=10A		18	22	mΩ
		V_{GS}=6V, I_D=5A		18.7	24	
		V_{GS}=4.5V, I_D=5A		19.6	32	
g_{FS}	Forward Transconductance	V_{DS}=10V, I_D=3A		14.5		S
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_S=1A			1	V
Dynamic						
C_{iss}	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		4708		pF
C_{oss}	Output Capacitance			326		
C_{rss}	Reverse Transfer Capacitance			247		
R_g	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		1.6		Ω
Q_g	Total Gate Charge	V_{DS}=80V, V_{GS}=10V, I_D=20A		75		nC
Q_{gs}	Gate-Source Charge			15.5		
Q_{gd}	Gate-Drain Charge			20.3		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=50V, I_D=1A, V_{GS}=10V, R_G=6Ω		11.5		ns
T_r	Turn-On Rise Time			29		
$t_{d(off)}$	Turn-Off Delay Time			42		
T_f	Turn-Off Fall Time			18		

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Typical Performance Characteristics

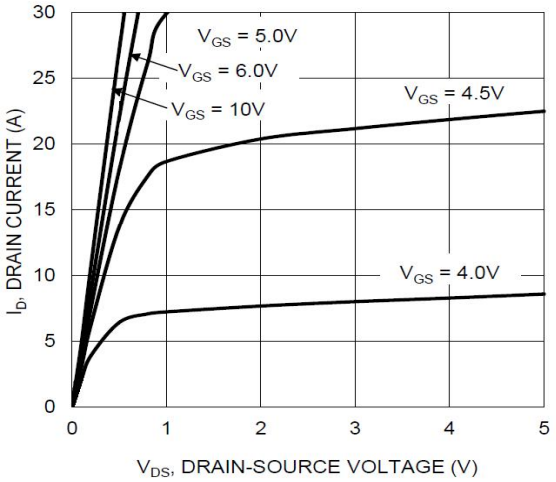

Fig.1 Typical Output Characteristics

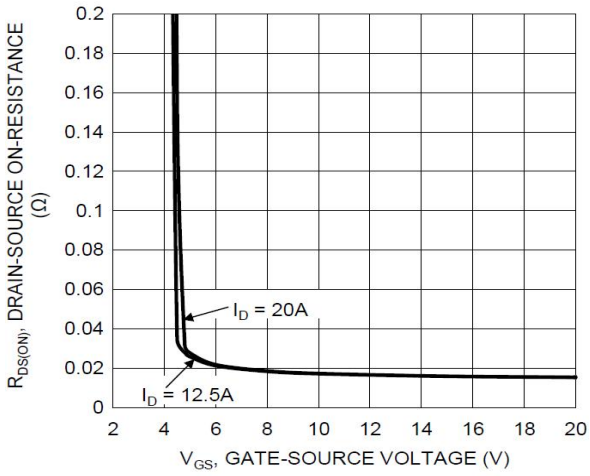

Fig.2 On-Resistance vs. Gate-Source Voltage

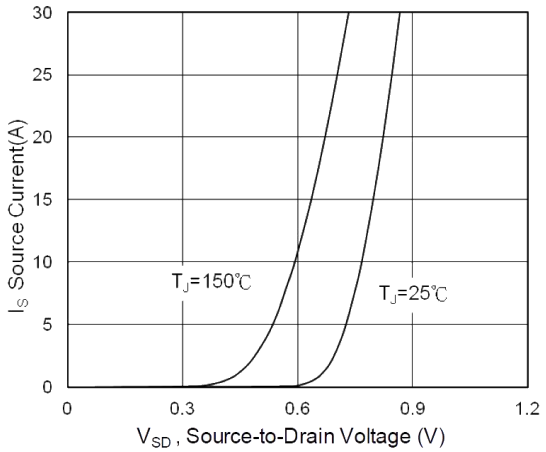

Fig.3 Diode Forward Voltage vs. Current

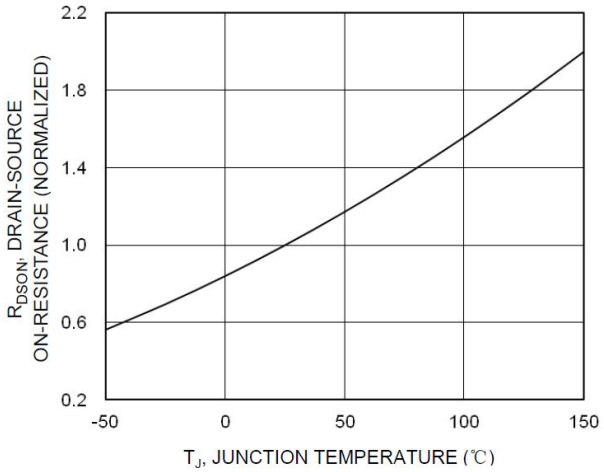

Fig.4 On-Resistance Variation with T_J

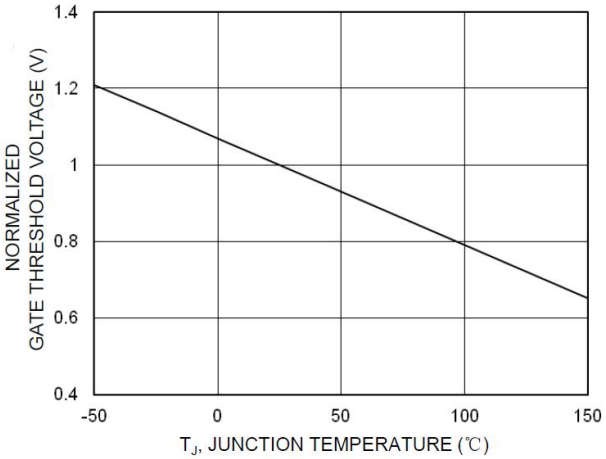

Fig.5 Gate Threshold Variation vs. T_J

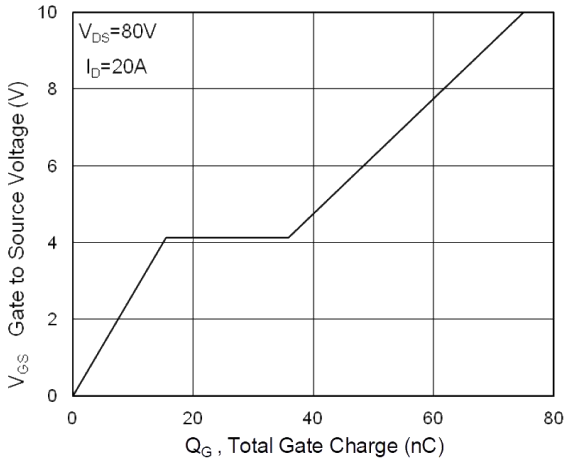

Fig.6 Gate Charge

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Typical Performance Characteristics (continue.)

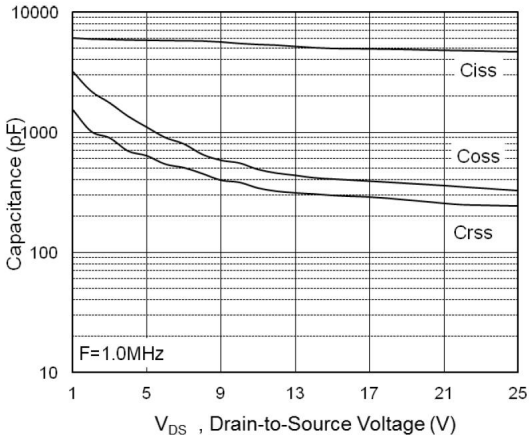

Fig.7 Typical Capacitance

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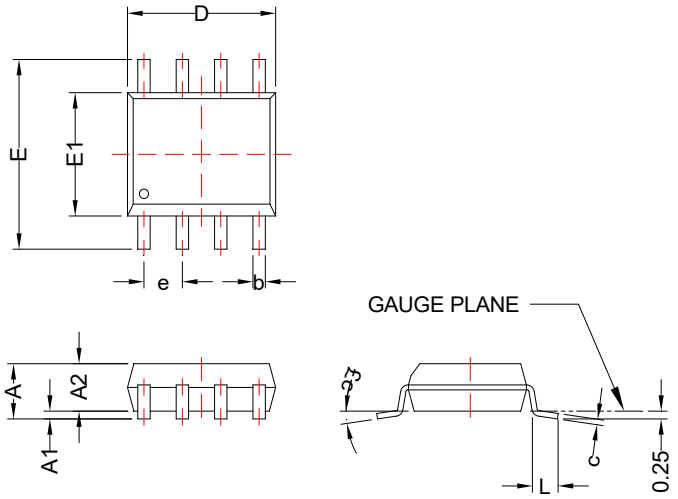
Package Dimension

SOP-8



Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	-	1.750	-	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	-	0.049	-
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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