LMN3112DF 30V N-Channel MOSFET

Features

- 30V, 40A, $R_{DS(ON)}$=12mΩ@V_{GS}=10V
- Improved dv/dt capability
- Fast switching
- 100% EAS guaranteed
- Green Device Available

Product Description

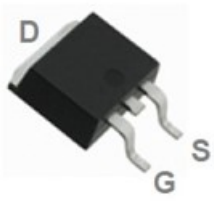
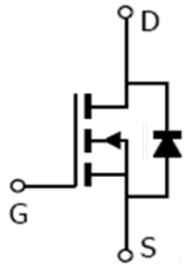
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for high efficiency fast switching applications.

Applications

- MB / VGA / Vcore
- DC-DC Converters
- Power Management Functions

Pin Configuration

LMN3112DF (TO-252-2L)	
	
Description	
Gate	
Source	
Drain	

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Ordering Information

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMN3112DF	LMN3112	D	F	TO-252	2500 PCS

Marking Information

Marking Information		
Part Marking	Part Number	LFC code
3112D XWMMMM	3112D	XWMMMM

Absolute Maximum Ratings

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DS}	Drain-Source Voltage		30	V
V_{GS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current (T_J=150℃)	T_A=25℃	40	A
		T_A=75℃	30	
		T_C=25℃	11.8	
I_{DM}	Pulsed Drain Current[1]		50	A
E_{AS}	Single Pulse Avalanche Energy[2]		13	
I_S	Continuous Source Current (Diode Conduction)		0.3	A
P_D	Power Dissipation	T_A=25℃	2.5	W
		T_A=75℃	1.6	
		T_C=25℃	40.3	
T_J	Operating Junction Temperature		-55 to +150	℃
T_{STG}	Storage Temperature Range		-55 to +150	℃
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		50	℃/W
$R_{\theta JC}$	Thermal Resistance-Junction to Case		3.1	℃/W

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Electrical Characteristics

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1.2		2.5	
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	uA
$R_{DS(on)}$	Drain-Source On-Resistance[3]	V_{GS}=10V, I_D=10A		9.8	12	mΩ
		V_{GS}=4.5V, I_D=5A		15.7	18	
g_{FS}	Forward Transconductance	V_{DS}=10V, I_D=3A			10	S
V_{SD}	Diode Forward Voltage[3]	I_S=1A, V_{GS}=0V		0.7	1	V
Dynamic						
Q_g	Total Gate Charge[3,4]	V_{DS}=15V, V_{GS}=4.5V, I_D=12.5A		8		nC
Q_{gs}	Gate-Source Charge[3,4]			4		
Q_{gd}	Gate-Drain Charge[3,4]			2		
C_{iss}	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz		1040		pF
C_{oss}	Output Capacitance			445		
C_{rss}	Reverse Transfer Capacitance			40		
$t_{d(on)}$	Turn-On Time[3,4]	V_{DD}=15V, I_D=12.5A, V_{GS}=10V, R_G=6Ω		10		ns
t_r	Rise Time[3,4]			9		
$t_{d(off)}$	Turn-Off Time[3,4]			24		
t_f	Fall Time[3,4]			8		
R_g	Gate Resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1		Ω

Note :

1. Repetitive Rating: Pulsed width limited by maximum junction temperature.
2. VDD=15V, VGS=10V, L=0.1mH, IAS=13A, Starting TJ=25℃.
3. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
4. Essentially independent of operating temperature.

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Typical Performance Characteristics

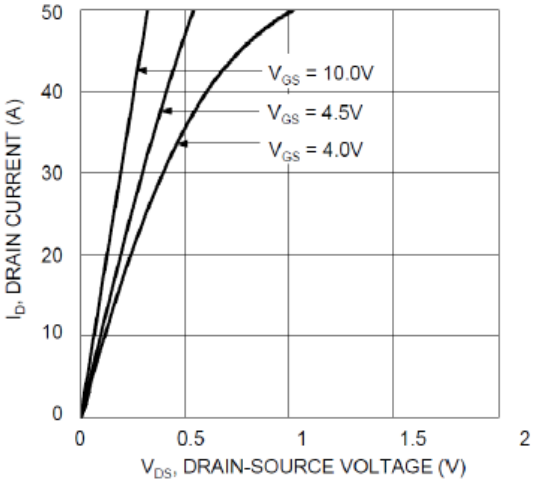

Fig. 1 Typical Output Characteristics

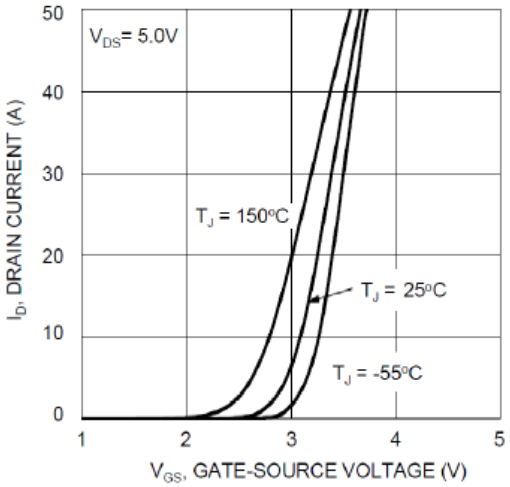

Fig. 2 Typical Transfer Characteristics

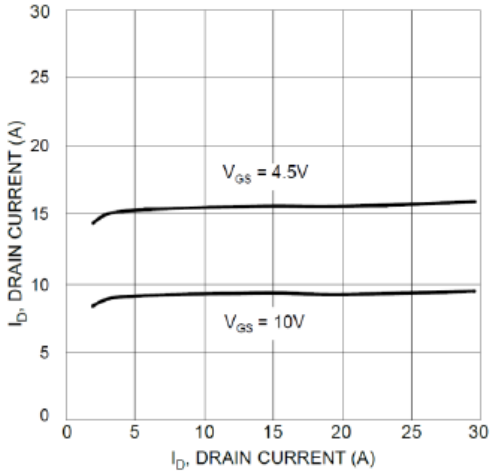

Fig. 3 Typical On-Resistance vs I_D and V_{GS}

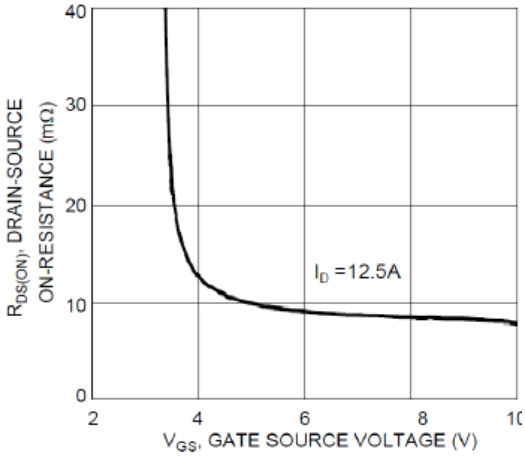

Fig. 4 Typical Transfer Characteristic

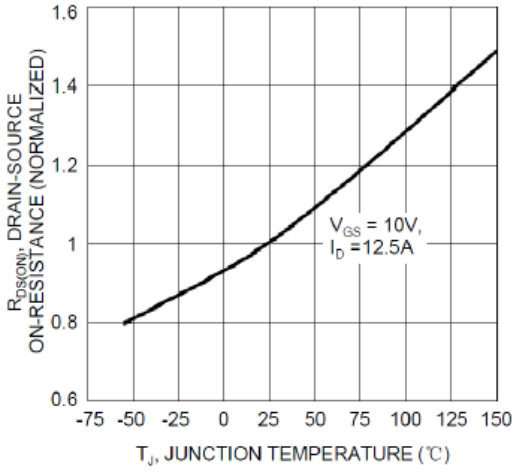

Figure. 5 On-Resistance Variation with T_J

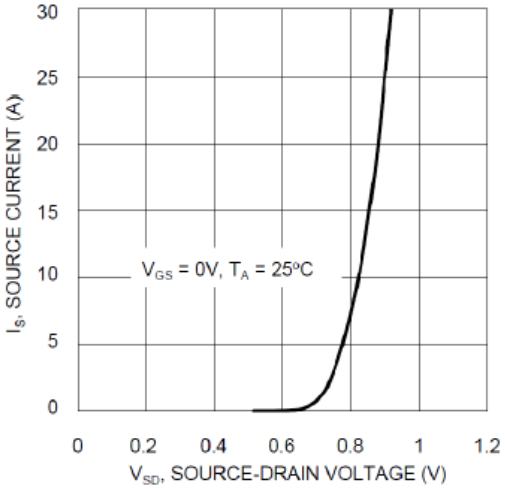

Fig. 6 Diode Forward Voltage vs. Current

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Typical Performance Characteristics(continue)

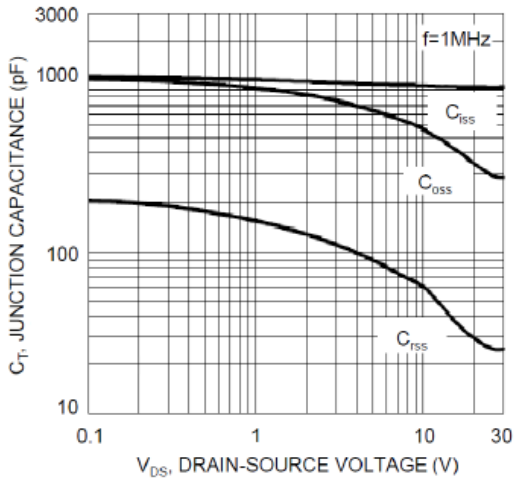

Fig. 7 Typical Capacitance

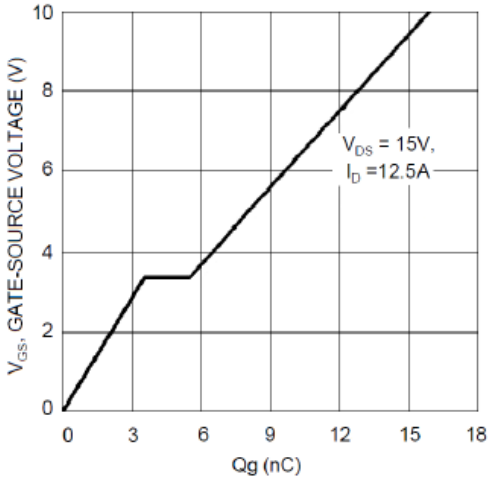

Fig. 8 Gate Charge

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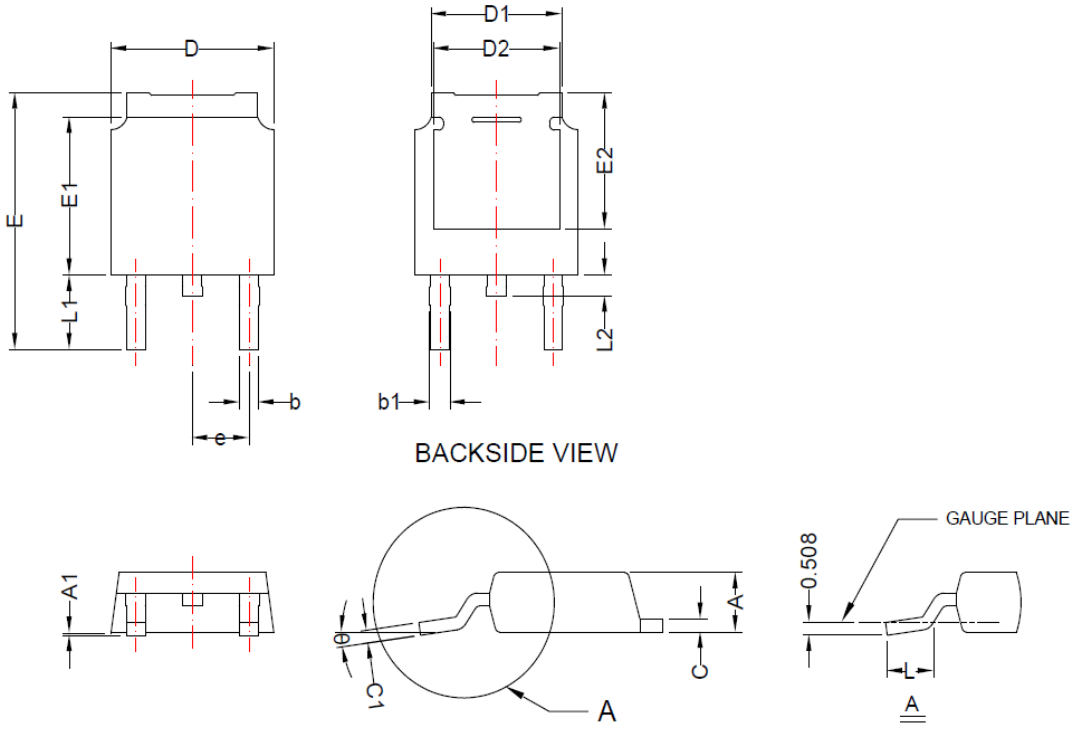
Package Dimension:

TO-252(AA)



THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM.DIMENDIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMS OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURSS, GATE BURS AND INTETLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

DIMENSION D DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH
OR PROTRUSION SHALL NOT EXCEED 0.15mm PER DNE. DIMENSION E1 DOES NOT INCLUDE MOLD FLASH, PROTRUSION. OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE
BURRS SHALL EXCEED 0.15mm INCHES PER DNE.

Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.18	2.40	0.086	0.094
A1	0.00	0.15	0.000	0.006
b	0.64	0.90	0.025	0.035
b1	0.76	1.14	0.030	0.045
c	0.40	0.89	0.016	0.035
c1	0.40	0.61	0.016	0.024
D	6.35	6.73	0.250	0.265
D1	4.95	5.46	0.195	0.215
D2	4.32	-	0.170	-

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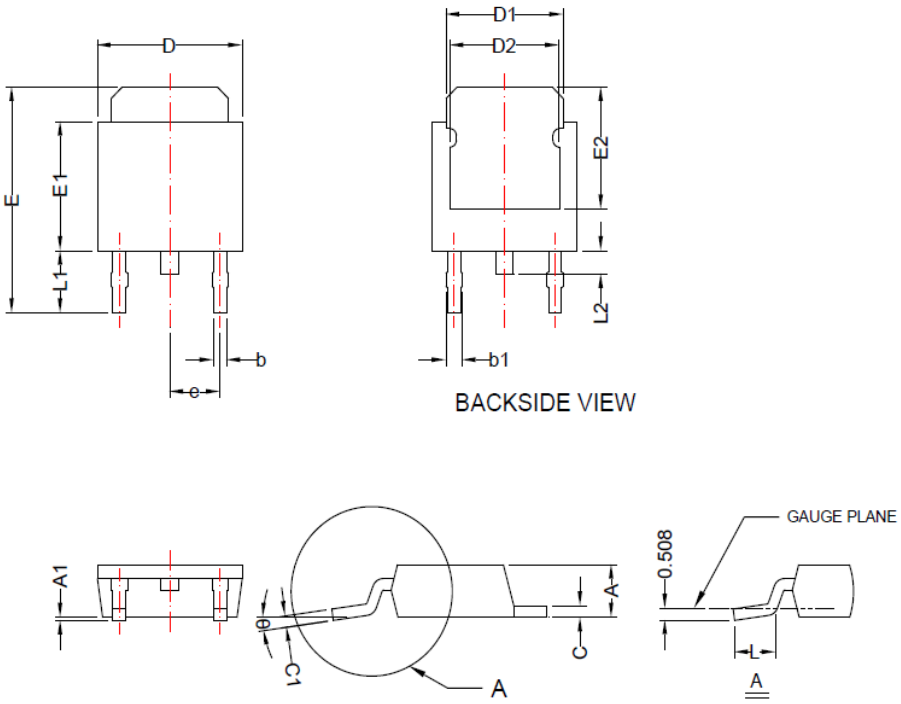
TO-252(AB)



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b1	0.76	1.14	0.030	0.045
c	0.40	0.89	0.016	0.035
c1	0.40	0.61	0.016	0.024
D	6.35	6.73	0.250	0.265
D1	4.95	5.46	0.195	0.215
D2	4.32	-	0.170	-
E	9.40	10.41	0.370	0.410
E1	5.33	5.80	0.210	0.228
E2	4.57	-	0.180	-
e	2.286 BSC		0.090 BSC	
L	1.40	1.78	0.055	0.070
L1	2.40	3.00	0.094	0.118
L2	-	1.20	-	0.047
θ	0°	8°	0°	8°

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