

LMN3112S 30V N-Channel MOSFET

Features

- 30V, 10.6A, $R_{DS(ON)}=12m\Omega@V_{GS}=10V$
- Improved dv/dt capability
- Fast switching
- 100% EAS guaranteed
- Green Device Available

been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for high efficiency fast switching applications.

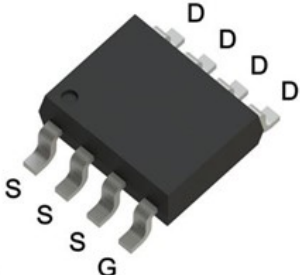
Product Description

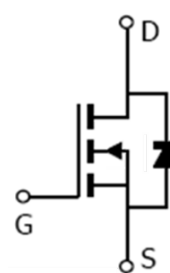
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has

Applications

- MB / VGA / Vcore
- DC-DC Converters
- Power Management Functions

Pin Configuration

LMN3112SF (SOP-8L)	
	
Pin	Description
1,2,3	Source
4	Gate
5,6,7,8	Drain



Ordering Information

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMN3112SF	LMN3112	S	F	SOP-8	4000 PCS

Marking Information

Marking Information		
Part Marking	Part Number	LFC code
3112S XWMMMM	3112S	XWMMMM

Absolute Maximum Ratings

(T_C=25°C Unless otherwise noted)

Symbol	Parameter	Typical	Unit
V _{DS}	Drain-Source Voltage	30	V
V _{GS}	Gate-Source Voltage	±20	V
I _D	Continuous Drain Current (T _J =150°C)	T _A =25°C	A
		T _A =75°C	
		T _C =25°C	
I _{DM}	Pulsed Drain Current ¹	40	A
E _{AS}	Single Pulse Avalanche Energy ²	21	
P _D	Power Dissipation	T _A =25°C	W
		T _A =75°C	
		T _C =25°C	
T _J	Operating Junction Temperature	-55 to +150	°C
T _{STG}	Storage Temperature Range	-55 to +150	°C
R _{θJA}	Thermal Resistance-Junction to Ambient	60	°C/W
R _{θJC}	Thermal Resistance-Junction to Case	25	°C/W

Electrical Characteristics

LMN3112S

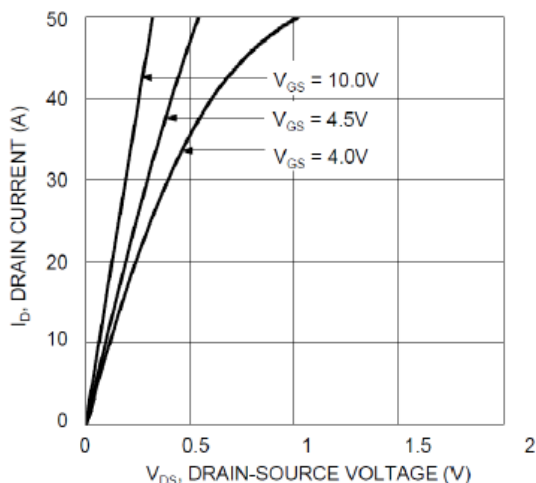
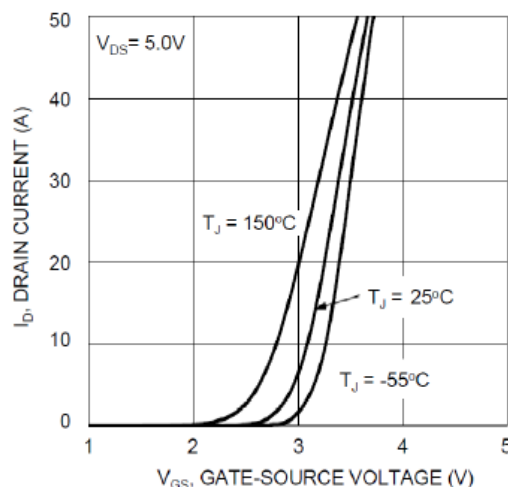
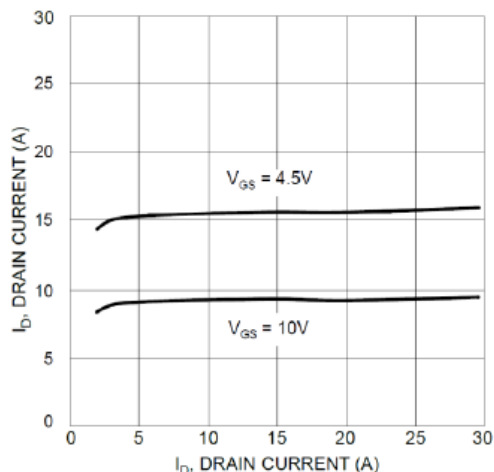
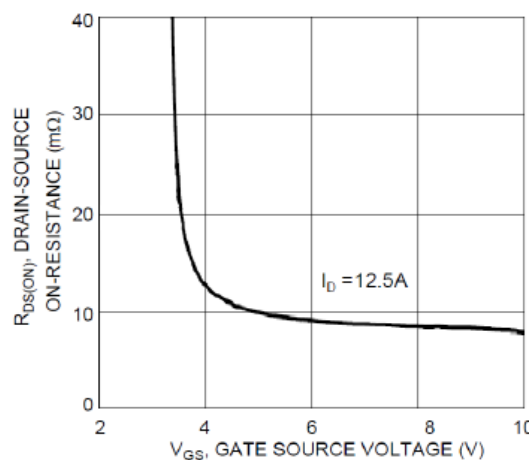
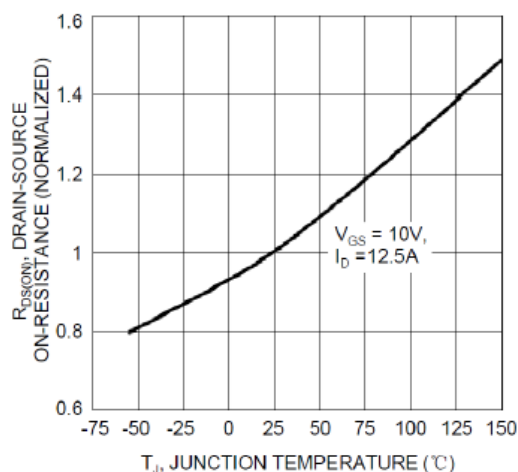
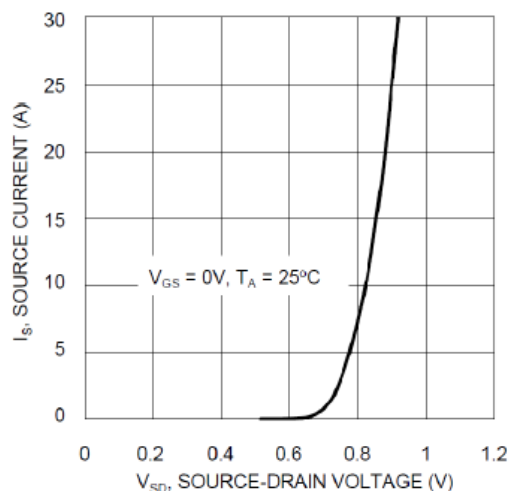
(T_C=25°C Unless otherwise noted)

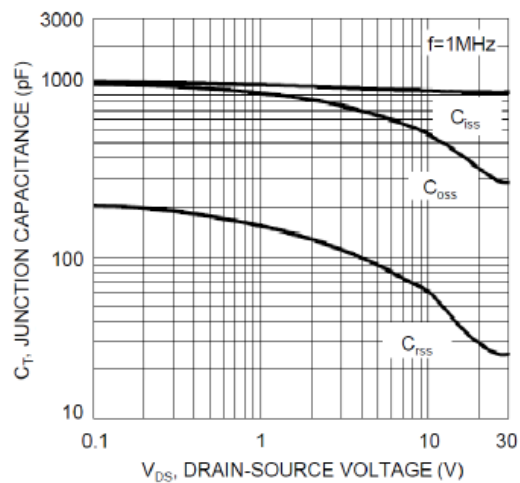
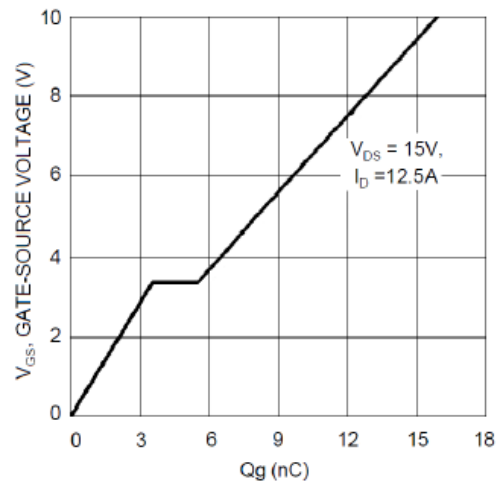
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1.2		2.5	
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V			1	uA
R _{DS(on)}	Drain-Source On-Resistance ³	V _{GS} =10V, I _D =10A		9.8	12	mΩ
		V _{GS} =4.5V, I _D =5A		15.7	18	
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =3A			10	S
V _{SD}	Diode Forward Voltage ³	I _S =1A, V _{GS} =0V		0.7	1	V
Dynamic						
Q _g	Total Gate Charge ^{3,4}	V _{DS} =15V, V _{GS} =4.5V, I _D =12.5A		8		nC
Q _{gs}	Gate-Source Charge ^{3,4}			4		
Q _{gd}	Gate-Drain Charge ^{3,4}			2		
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		1040		pF
C _{oss}	Output Capacitance			445		
C _{rss}	Reverse Transfer Capacitance			40		
t _{d(on)}	Turn-On Time ^{3,4}	V _{DD} =15V, I _D =12.5A, V _{GS} =10V, R _G =6Ω		10		ns
t _r	Rise Time ^{3,4}			9		
t _{d(off)}	Turn-Off Time ^{3,4}			24		
t _f	Fall Time ^{3,4}			8		
R _g	Gate Resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		1		Ω

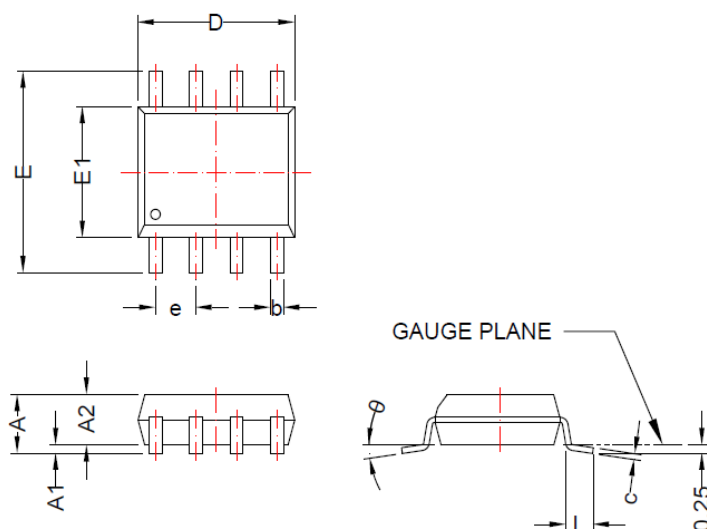
Note :

1. Repetitive Rating: Pulsed width limited by maximum junction temperature.
2. V_{DD}=15V, V_{GS}=10V, L=0.1mH, I_{AS}=13A, Starting T_J=25°C.
3. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
4. Essentially independent of operating temperature.

Typical Performance Characteristics


Fig. 1 Typical Output Characteristics

Fig. 2 Typical Transfer Characteristics

Fig. 3 Typical On-Resistance vs I_D and V_{GS}

Fig. 4 Typical Transfer Characteristic

Figure 5 On-Resistance Variation with T_J

Fig. 6 Diode Forward Voltage vs. Current

Typical Performance Characteristics(continue)

Fig. 7 Typical Capacitance

Fig. 8 Gate Charge

Package Dimension:
SOP-8


DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END.

Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.10	0.26	0.004	0.010
D	4.70	5.10	0.185	0.201
E	5.80	6.20	0.228	0.244
E1	3.70	4.10	0.146	0.161
e	1.27 BSC		0.050 BSC	
L	0.4	1.27	0.016	0.050
θ	0°	8°	0°	8°

NOTICE:

LFC Semiconductor assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all LFC Semiconductor products described or contained herein. LFC Semiconductor products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

Applications shown on the herein document are examples of standard use and operation. Customers are responsible in comprehending the suitable use in particular applications. LFC Semiconductor makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Information furnished is believed to be accurate and reliable. However LFC Semiconductor assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties, which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of LFC Semiconductor. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information without express written approval of LFC Semiconductor.