LMNN3218SF 30V Dual N-Channel MOSFETs

Features

- 30V, 7.3A, $R_{DS(ON)}$=22mΩ@V_{GS}=10V
- Improved dv/dt capability
- Fast switching
- 100% EAS Guaranteed
- Green Device Available
- SOP-8 package design

Product Description

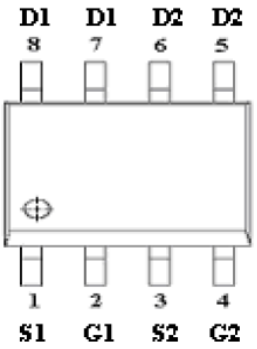
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.
These devices are well suited for high efficiency fast switching applications.

Applications

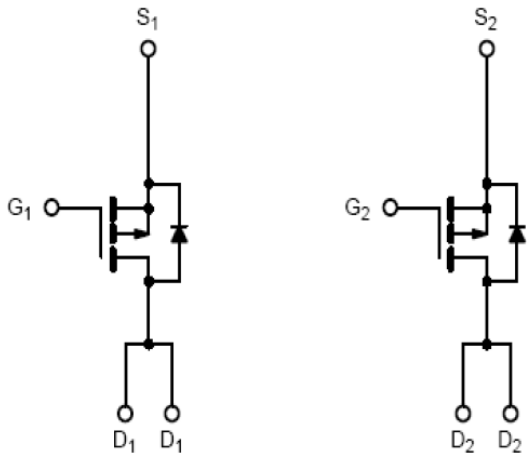
- MB / VGA / Vcore
- POL Applications
- SMPS 2nd SR

Pin Configuration

LMNN3218SF (SOP-8)



PIN	Description
1	Source 1
2	Gate 1
3	Source 2
4	Gate 2
5	Drain 2
6	Drain 2
7	Drain 1
8	Drain 1



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Ordering Information

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMNN3218SF	LMNN3218	S	F	SOP-8	4000pcs

Marking Information

Marking Information	
Part Number	LFC code
3218S	XWMMMM

Absolute Maximum Ratings

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DS}	Drain-Source Voltage		30	V
V_{GS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current	T_A=25℃	7.3	A
		T_A=100℃	3.3	
I_{DM}	Pulsed Drain Current[1]		29	A
EAS	Single Pulse Avalanche Energy		32	mJ
IAS	Single Pulse Avalanche Current		8	A
P_D	Power Dissipation	T_A=25℃	1.8	W
		T_A=100℃	0.4	
T_J	Operating Junction Temperature		-55 to +150	℃
T_{STG}	Storage Temperature Range		-55 to +150	℃
$R_{\theta JA}$	Thermal Resistance-Junction to Case		70	℃/W

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Electrical Characteristics

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30			V
$V_{GS\ (th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1.2	1.6	2.5	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	uA
		V_{DS}=24V, V_{GS}=0V T_J=125ºC			10	
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V			1	V
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=7A		19	22	mΩ
		V_{GS}=4.5V, I_D=5A		24	28	
Dynamic characteristics						
Q_g	Total Gate Charge	V_{DD}=15V, V_{GS}=4.5V, I_D=7A		4.1	6	nC
Q_{gs}	Gate-Source Charge			1	1.4	
Q_{gd}	Gate-Drain Charge			2.1	4	
C_{iss}	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1.0MHz		345	500	pF
C_{oss}	Output Capacitance			55	80	
C_{rss}	Reverse Transfer Capacitance			32	45	
$t_{d(on)}$	Turn-On Time	V_{DD}=75V, V_{GS}=10V, R_g=10Ω, I_D=1.0A		2.8	5	ns
t_r				7.2	14	
$t_{d(off)}$	Turn-Off Time			15.8	30	
t_f				4.6	9	
R_g	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		3.2	6.4	Ω

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Typical Performance Characteristics

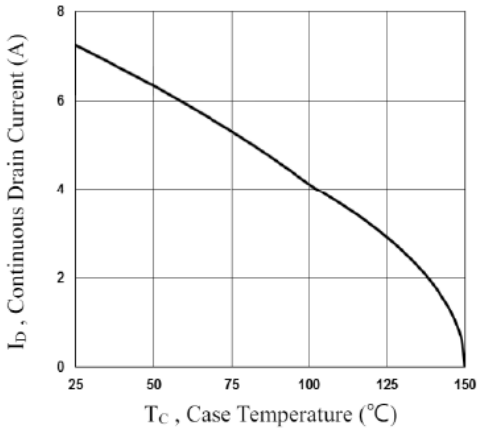

Fig.1 Continuous Drain Current vs. T_C

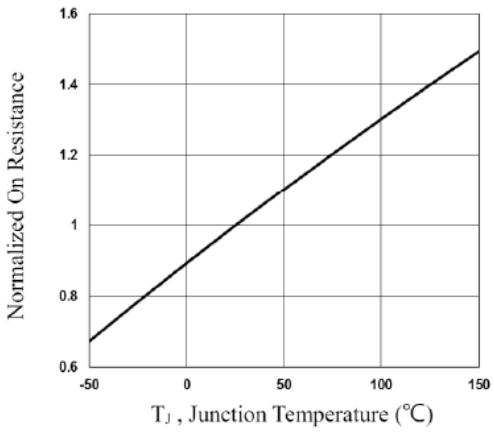

Fig.2 Normalized RDSON vs. T_J

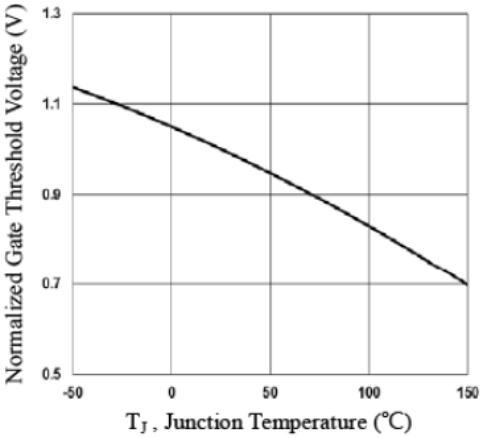

Fig.3 Normalized V_{th} vs. T_J

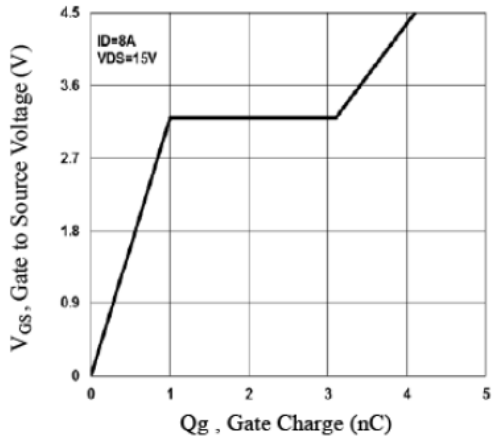

Fig.4 Gate Charge Waveform

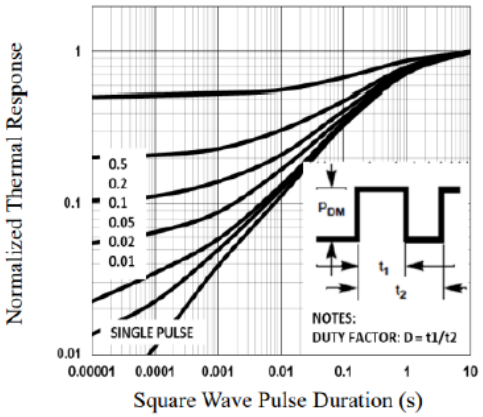

Fig.5 Normalized Transient Response

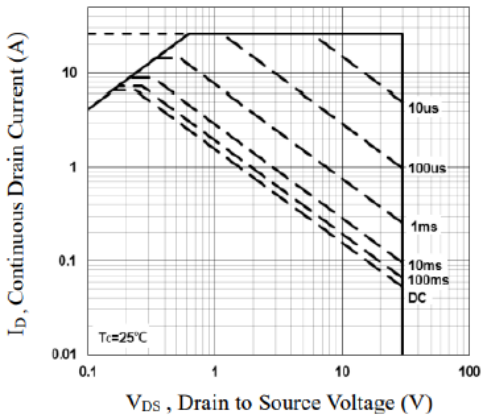

Fig.6 Maximum Safe Operation Area

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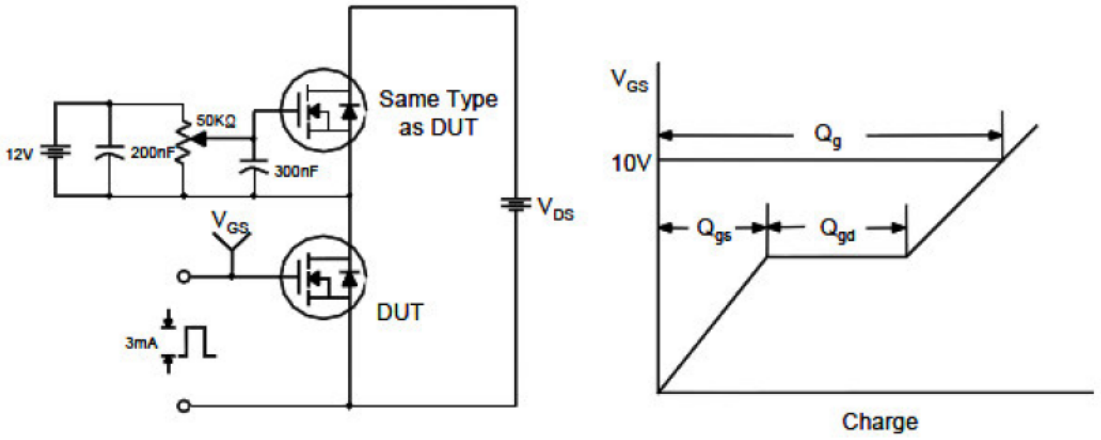
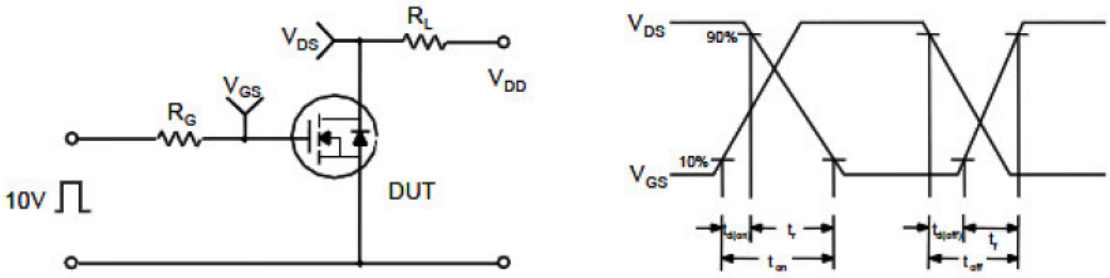
Typical Performance Characteristics(continue)

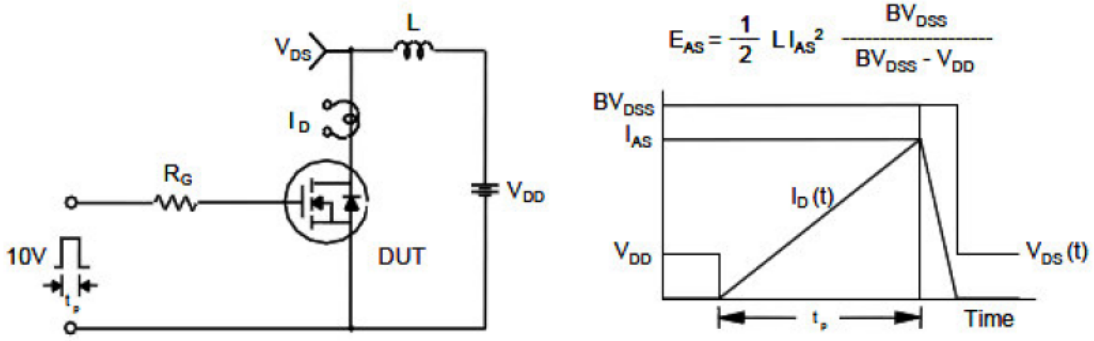
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



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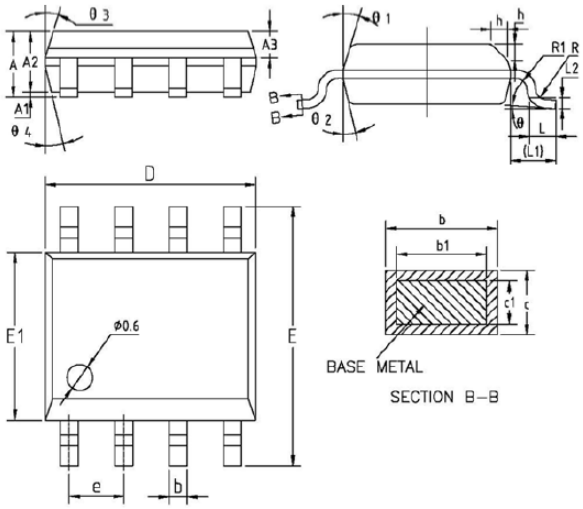
Package Dimension:

SOP-8



Dimensions				
Symbol	**Millimeters**		**Inches**	
	Min	Max	Min	Max
A	1.350	1.750	0.531	0.689
A1	0.100	0.250	0.039	0.098
A2	1.250	1.650	0.492	0.650
A3	0.500	0.700	0.197	0.276
b	0.380	0.510	0.150	0.201
b1	0.370	0.470	0.146	0.185
c	0.180	0.250	0.071	0.098
c1	0.170	0.230	0.067	0.091
D	4.800	5.000	1.890	1.969
E	5.800	6.200	2.283	2.441
E1	3.800	4.000	1.496	1.575
e	1.170	1.370	0.461	0.539
L	0.450	0.800	0.177	0.315
L1	1.040 (BSC)		0.409 (BSC)	
L2	0.250 (BSC)		0.098 (BSC)	
R/R1	0.070	-	0.028	-
h	0.300	0.500	0.118	0.197
Θ	0°	8°	0°	8°

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