LMP2165RF 20V P-Channel Enhancement MOSFET

Features

- $R_{DS(ON)}$ =65mΩ@V_{GS} = -4.5V
- Improved dv/dt capability
- Fast switching
- Suit for -1.8V Gate Drive Applications
- Green Device Available
- SOT-23-6L package design

Product Description

These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

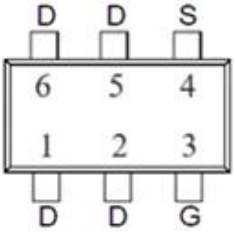
These devices are particularly suited for high efficiency fast switching applications.

Applications

- Notebook
- Load Switch
- Hand-held Instruments

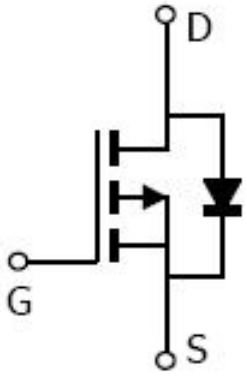
Pin Configuration

LMP2165RF (SOT-23-6L)



Top Views

Pin	Description
1	Drain
2	Drain
3	Gate
4	Source
5	Drain
6	Drain



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Ordering Information

Part Number	P/N	PKG Code	Pb Free Code	Package	Quantity Reel
LMP2165RF	LMP2165	R	F	SOT-23-6L	3000 pcs

Marking Information

Part Marking	Part Number	LFC code
P1 XWM	P1	XWM

Absolute Maximum Ratings

(T_A=25ºC Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DS}	Drain-Source Voltage		-20	V
V_{GS}	Gate-Source Voltage		±12	V
I_D	Continuous Drain Current[1]	T_A=25ºC	-3.5	A
		T_A=70ºC	-2.6	
I_{DM}	Pulsed Drain Current[2]		-12	A
P_D	Total Power Dissipation[3]	T_A=25ºC	1.25	W
		T_A=70ºC	0.8	
T_J	Operating Junction Temperature Range		-55 to +150	ºC
T_{STG}	Storage Temperature Range		-55 to +150	ºC
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		100	ºC/W

Note:
1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2oz copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The power dissipation is limited by 150ºC junction temperature.

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Electrical Characteristics

(T_A=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-0.4		-0.9	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±12V			±100	nA
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-20V, V_{GS}=0V			-1	uA
I_S	Continuous Source Current	V_G=V_D=0V, Force Current			-4.1	A
I_{SM}	Pulsed Source Current				-8.2	
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=-4.5V, I_D=-4.5A		59	65	mΩ
		V_{GS}=-2.5V, I_D=-3A		80	85	
		V_{GS}=-1.8V, I_D=-1.5A		110	130	
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-4.5A		10		S
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_S=-1A		-0.8	-1.2	V
Dynamic						
C_{iss}	Input Capacitance	V_{DS}=-10V, V_{GS}=0V, f=1MHz		515		pF
C_{oss}	Output Capacitance			55		
C_{rss}	Reverse Transfer Capacitance			20		
Q_g	Total Gate Charge[4,5]	V_{DS}=-10V, V_{GS}=-4.5V, I_D=-3A		6.4		nC
Q_{gs}	Gate-Source Charge[4,5]			0.9		
Q_{gd}	Gate-Drain Charge[4,5]			1.6		
$t_{d(on)}$	Turn-On Delay Time[4,5]	V_{DD}=-10V, I_D=-1A, V_{GS}=-4.5V, R_G=25Ω		5		ns
T_r	Turn-On Rise Time[4,5]			17.4		
$t_{d(off)}$	Turn-Off Delay Time[4,5]			40.7		
T_f	Turn-Off Fall Time[4,5]			11.4		

Note:

4. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
5. Essentially independent of operating temperature..

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Typical Performance Characteristics

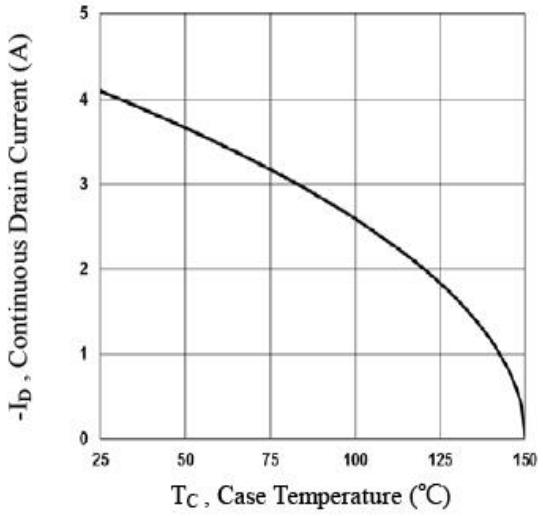

Fig.1 Continuous Drain Current vs T_C

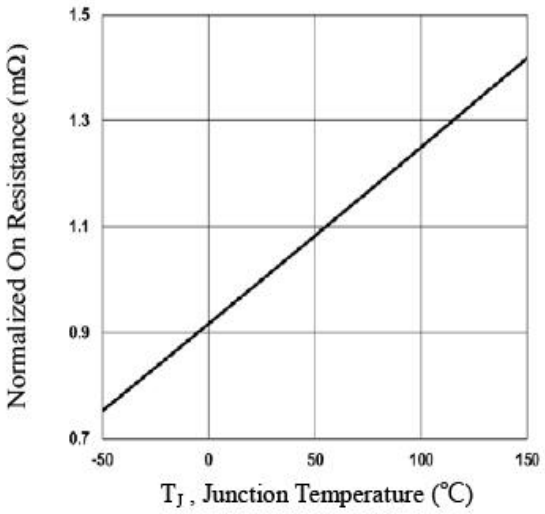

Fig.2 Normalized R_{DSON} vs T_J

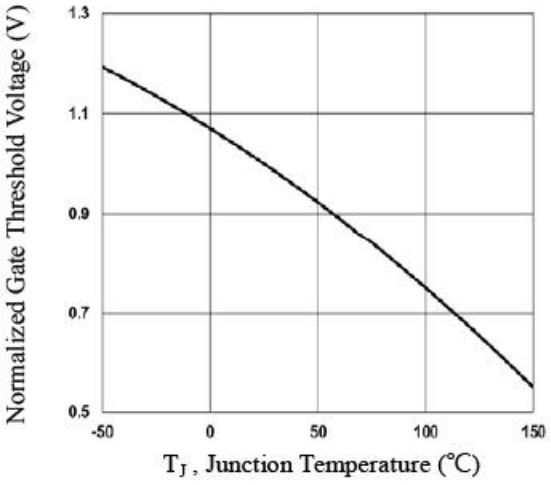

Fig.3 Normalized V_{TH} vs T_J

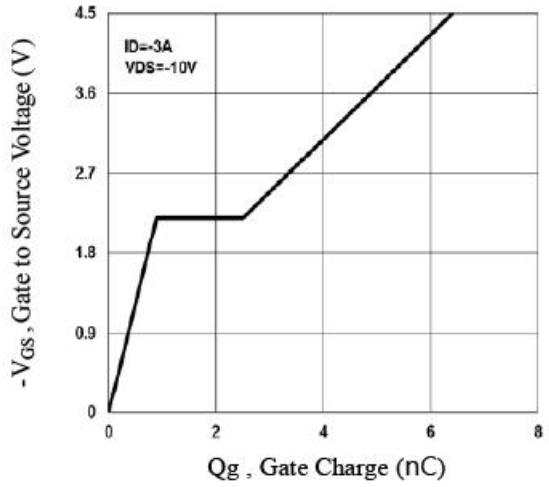

Fig.4 Gate Charge Waveform

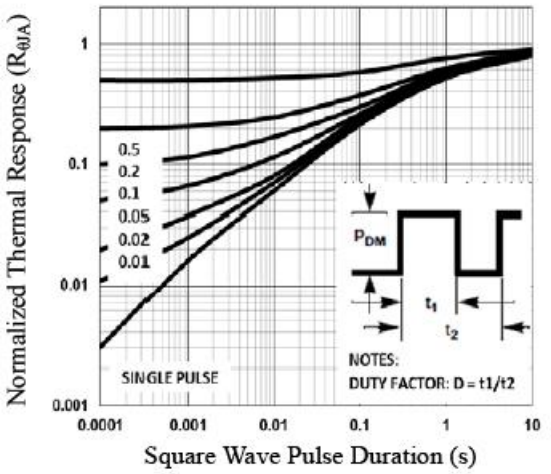

Fig.5 Normalized Transient Impedance

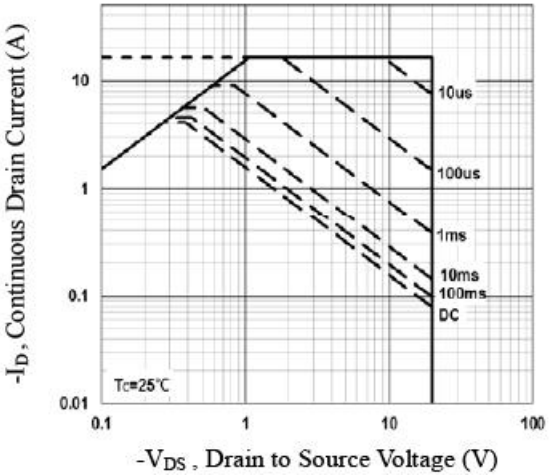

Fig.6 Maximum Safe Operating Area

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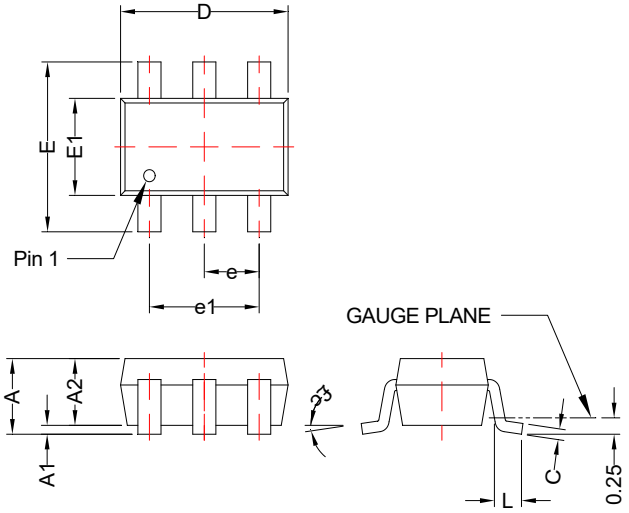
Package Dimension

SOT-23-6L



Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.900	1.450	0.035	0.057
A1	0.000	0.150	0.000	0.006
A2	0.900	1.300	0.035	0.051
b	0.300	0.500	0.012	0.020
c	0.080	0.260	0.003	0.010
D	2.700	3.100	0.106	0.122
E	2.200	3.000	0.087	0.118
E1	1.300	1.750	0.051	0.069
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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