

LMP3117ZF 30V P-Channel Enhancement Mode MOSFET

Features

- $R_{DS(ON)}=13.5m\Omega@V_{GS}=-10V$
- Fast switching
- Suit for -4.5V Gate Drive Applications
- Green Device Available
- DFN3X3-8L package design

Product Description

The P-Channel enhancement mode power field effect transistors is using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and

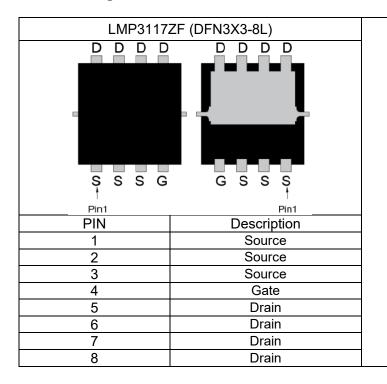
commutation mode.

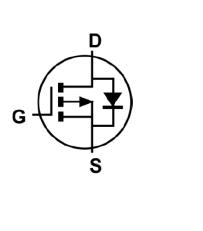
This device is well suited for high efficiency fast switching applications.

Applications

- MB / VGA / Vcore
- POL Applications
- Load Switch
- LED Application

Pin Configuration







Ordering Information

Ordering Information						
Part Number	P/N	PKG code	Pb Free code	Package	Quantity	
LMP3117ZF	LMP3117	Z	F	DFN3x3-8L	5000pcs	

Marking Information

Marking Information					
Product Code	LFC code				
<u>3117ZF</u>					

Absolute Maximum Ratings

(T_C=25°C Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DS}	Drain-Source Voltage		-30	V
V_{GS}	Gate-Source Voltage		±25	V
	Continuous Drain Current (T _J =150°C)	T _A =25℃	-31	Δ.
ID		T _A =100℃	-20	A
I _{DM}	Pulsed Drain Current		-70	А
P_D	Davier Dissipation	T _A =25℃	T _A =25℃ 22	
	Power Dissipation	T _A =100°C	9	W
ТJ	Operating Junction Temperature	·	-55 to +150	$^{\circ}$
T _{STG}	Storage Temperature Range		-55 to +150	$^{\circ}$ C
$R_{ heta JC}$	Thermal Resistance Junction to ambient		5.8	°C/W



Electrical Characteristics

(T_C=25°C Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
	St	atic characteristics		<u>'</u>	'	
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30			V
$V_{GS\ (th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_{D}=-250uA$	-1.2	-1.6	-2.5	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±25V			±100	nA
I _{DSS}	Drain-Source Leakage Current	V_{DS} =-30V, V_{GS} =0V			-1	uA
V_{SD}	Diode Forward Voltage ³	I _S =-1A, V _{GS} =0V			-1	V
R _{DS(on)}	Drain-Source On-Resistance ³	V _{GS} =-10V, I _D =-10A		10.8	13.5	mO.
		V _{GS} =-4.5V, I _D =-6A		17	25	mΩ
	Gate	charge characteristics				
Q_g	Total Gate Charge ^{3,4}	45)/)/ 45)/		22		
Q_{gs}	Gate-Source Charge ^{3,4}	-V _{DD} =-15V, V _{GS} =-4.5V, -I _D =-15A		8.7		nC
Q_{gd}	Gate-Drain Charge ^{3,4}	-ID IDA		7.2		
	Dyr	namic characteristics	•			
C _{iss}	Input Capacitance	\(- 45\(\) \(-0\(\)		2215		
Coss	Output Capacitance	-V _{DS} =-15V, V _{GS} =0V, -f=1.0MHz		310		pF
C_{rss}	Reverse Transfer Capacitance	-I - I .UIVIMZ		237		1
t _{d(on)}	Turn-On Time	V_{DD} =-15V, V_{GS} =-10V, R_g =3.3 Ω , I_D =-15A		8		
t _r				73.7		ne
$t_{d(off)}$	Turn-Off Time			61.8		ns -
t _f				24.4		



Typical Performance Characteristics

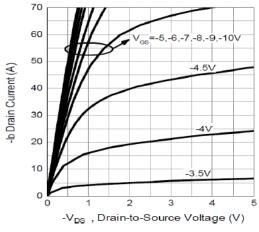


Figure 1. Output Characteristics

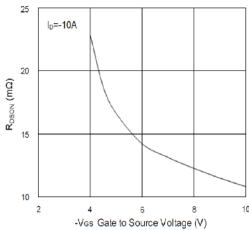


Figure 2. On-Resistance Variation with VGS

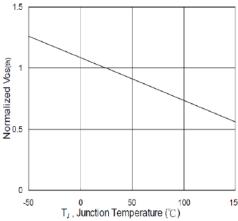


Figure 3. Normalized $V_{GS(th)}$ vs. T_J

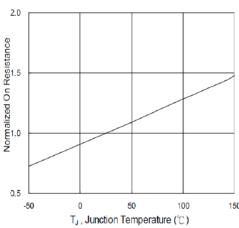


Figure 4. Normalized RDSON vs. TJ

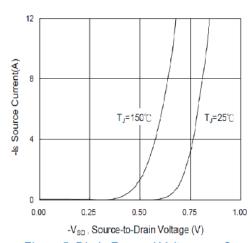


Figure 5. Diode Forward Voltage vs. Current

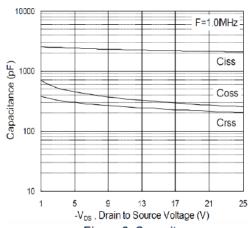


Figure 6. Capacitance



Typical Performance Characteristics(continue)

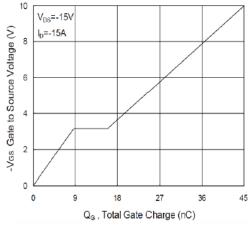


Figure 7. Gate Charge Waveform

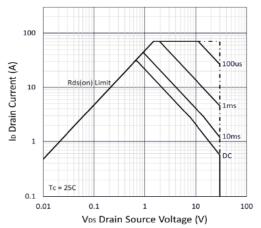


Figure 8. Maximum Safe Operating Area

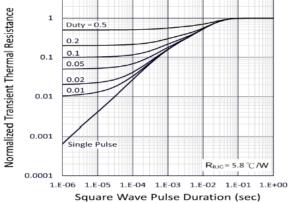


Figure 9. Normalized Transient Thermal Resistance

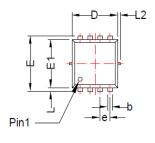
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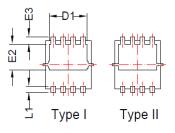


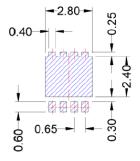
Package Dimension:

DFN3x3-8L

Package Dimension







Recommended Land Pattern





BACKSIDE VIEW

	Dimensions						
Symbol	Millimeters		Inches				
Symbol	Min	Max	Min	Max			
Α	0.70	0.90	0.028	0.035			
A1	0.00	0.05	0.000	0.002			
b	0.24	0.37	0.009	0.015			
С	0.10	0.25	0.004	0.010			
D	2.90	3.25	0.114	0.128			
D1	2.35	2.60	0.093	0.102			
E	3.05	3.45	0.120	0.136			
E1	2.90	3.20	0.114	0.126			
E2	1.35	2.00	0.053	0.079			
E3	0.30	0.60	0.012	0.024			
е	0.65 BSC		0.026 BSC				
L	0.02	0.2	0.001	0.008			
L1	0.28	0.5	0.011	0.020			
L2	-	0.15	-	0.006			

Dimensions are exclusive of Burrs, Mold Flash & Tie Bar extrusions

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