

TOPWAY

SPECIFICATIONS

PASSIVE MATRIX LCD MODULE

(192 X 128 DOTS , EL BACKLIGHT)

LMS195-F

REV. 2 June, 28, 2001

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SHENZHEN TOPWAY ELECTRONIC CO., LTD

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영양부 13-01-94-145-A 1995. 10. 31

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NO.	PART NO.	DESCRIPTION	SPECIFICATIONS NO.
	HQ 19501NY-EWS	LCD MODULE (192 x 128 DOTS)	
	Rev. 1		

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HYUNDAI ELECTRONICS INDUSTRIES CO., LTD.

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1. FEATURES

- * 192 × 128 dots graphic LCD module
- * STN Yellow/Green type display
- * Control IC : SED1330F_{BA} (SEIKO EPSON)
- * Driving method : 1/128 Duty, 1/10.8 Bias
- * Viewing direction : 6 O'clock
- * Backlighting : EL Unit (White + Transflective)

2. MECHANICAL SPECIFICATIONS

Item	Specification	Unit
Outline dimension (W × H × T)	98.0 × 86.0 × 13.0 Max	mm
Viewing Area (W × H)	77.5 × 54.0	mm
Dot Size (W × H)	0.33 × 0.33	mm
Dot Pitch	0.37 × 0.37	mm
Weight	About 110	g

3. ABSOLUTE MAXIMUM RATINGS

3-1. Electrical absolute maximum ratings

Item	Symbol	Value		Unit	Condition	
		Min.	Max.			
Power supply voltage	Logic	$V_{DD} - V_{SS}$	0	7.0	V	$T_a = 25\text{ }^\circ\text{C}$ $V_{DD} = 5\text{ V} \pm 10\%$ $V_{SS} = 0\text{ V}$
	LCD	$V_{DD} - V_0$	0	28	V	
Input Voltage	V_I	- 0.3	$V_{DD} + 0.3$	V		

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3-2. Enviromental conditions

Item	Symbol	Min.	Max.	Unit
Operating temperature	Topr	0	50	℃
Storage temperature	Tstg	- 20	70	℃
Humidity (Ambient temperature=Ta)	Ta ≤ 40℃		95%RH max.	
	Ta > 40℃		Absolute humidity must be lower than the humidity of 95%RH at Ta = 40℃.	

4. ELECTRICAL SPECIFICATIONS

4-1. Electrical characteristics

Item	Symbol	Spec. Value			Unit	Condition	
		Min.	Typ.	Max.			
Supply voltage	Logic	$V_{DD} - V_{SS}$	4.5	5.0	5.5	V	Ta = 0℃ Ta = 25℃ Ta = 50℃
	LCD	$V_{DD} - V_0$	- 16.7	18.6 17.6 15.6	- 18.5 -		
Supply current	Logic	I_{DD}	-	10.0	15.0	mA	Note 1)
	LCD	I_0	-	5.0	7.5		
Power consumption		P_d	-	114.0	171.0	mW	
Input voltage	High level	V_{IH}	0.8 V_{DD}	-	V_{DD}	V	-
	Low level	V_{IL}	0	-	0.2 V_{DD}	V	-

Note 1) Condition : $V_{DD} = 5\text{ V}$
 $V_{DD} - V_0 = 17.6\text{ V}$
 Display pattern : Full dot ON

5. CHARACTERISTICS OF BACKLIGHTING (EL UNIT)

5-1. Absolute maximum ratings

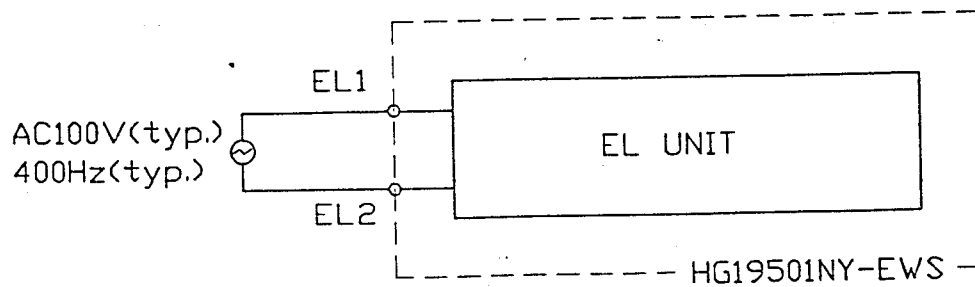
Item	Symbol	Condition	Min.	Max.	Unit
Applied voltage	Va	Ta = 25 °C	-	150	AC Vrms
Applied frequency	Fa	Ta = 25 °C	-	1000	Hz
Operating temperature	Topr		- 20	+ 60	°C
Storage temperature	Tstg		- 30	+ 70	°C
Operating humidity		40 °C	-	95	% RH

5-2. Opto-electric Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Applied voltage	Va	Ta = 25 °C	80	100	120	AC Vrms
Applied frequency	Fa	Ta = 25 °C	-	400	-	Hz
Luminous		Va = 100 Vrms Fa = 400 Hz Ta = 25 °C	45	55	-	cd / m ²
Current	Id		-	0.12	0.17	mA / cm ²

5-3. EL circuit diagram

To the EL backlight, apply AC signal from low-frequency constant voltage source or from EL inverter.



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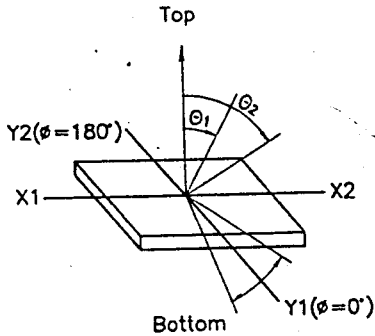
6. OPTICAL CHARACTERISTICS

$T_a = 25\text{ }^\circ\text{C}$, $V_{DD} = 5\text{ V} \pm 10\%$

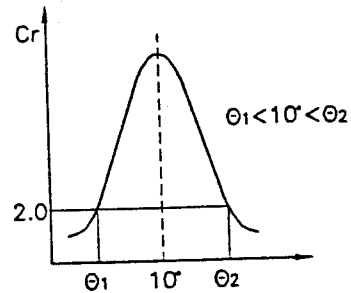
Item	Symbol	Min.	Typ.	Max.	Unit	Condition	Note
Viewing Angle	$\theta_2 - \theta_1$	50	60	+ 30	deg.	$Cr = 2.0$	1.2
	ϕ	- 30					
Contrast Ratio	Cr	2	3	-	-	$\theta = 10^\circ$ $\phi = 0^\circ$	3
Response Time(rise)	Tr	-	250	350	ms	$\theta = 10^\circ$ $\phi = 0^\circ$	4
Response Time(fall)	Tf	-	250	350	ms	$\theta = 10^\circ$ $\phi = 0^\circ$	4

* Above data are measured under 1/128 duty STN yellow/green mode.
* $\phi = 0$ means viewing direction.

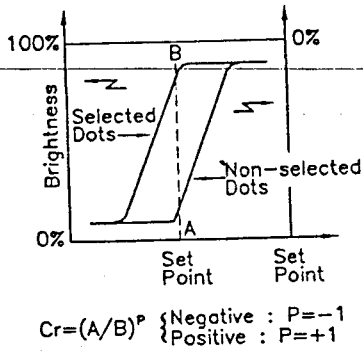
Note 1. Definition of angle θ and ϕ



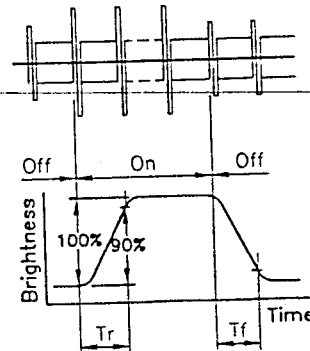
Note 2. Definition of viewing angle θ_1 and θ_2



Note 3. Definition of contrast Cr



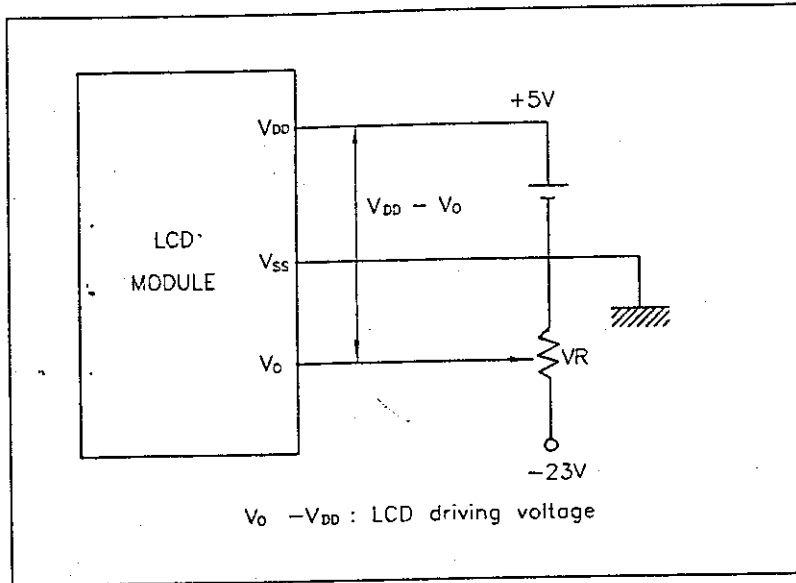
Note 4. Definition of optical response



6. INTERFACE PIN ASSIGNMENT

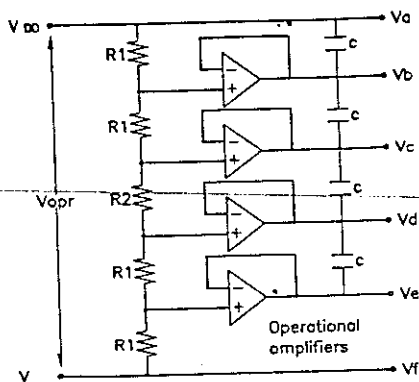
Pin No.	Symbol(CN2)	Level	Description
1	FG	0 V	Frame ground
2	V _{SS} (GND)	0 V	Ground
3	V _{DD} (V _{CC})	+ 5 V	Power supply voltage for logic and LCD
4	V _O	-	Operating voltage for LCD. (Variable)
5	/RES	H/L	Reset signal
6	/RD	H/L	Read signal
7	/WR	H/L	Write signal
8	/CS	H/L	Chip select signal
9	A0	H/L	Data type select signal
10	DB0	H/L	Display data bit 0
11	DB1	H/L	Display data bit 1
12	DB2	H/L	Display data bit 2
13	DB3	H/L	Display data bit 3
14	DB4	H/L	Display data bit 4
15	DB5	H/L	Display data bit 5
16	DB6	H/L	Display data bit 6
17	DB7	H/L	Display data bit 7
18	NC	-	No connection
19	EL1	AC100V _{rms} 400Hz	EL power
20	EL2		

8. POWER SUPPLY BLOCK DIAGRAM



9. BIAS VOLTAGE GENERATION CIRCUIT

Six levels of voltage, V_a to V_f are applied to the common and segment drivers. The voltage is generated through operational amplifier by resistance-division from liquid crystal operating voltage (V_{opr}). Here, an operational amplifier is used as a voltage follower.



V_a	Common and segment selection high level
V_b	Common non-selection high level
V_c	Segment non-selection high level
V_d	Segment non-selection low level
V_e	Common non-selection low level
V_f	Common and segment selection low level

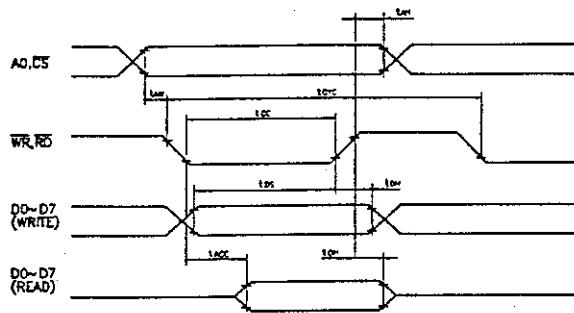
9. TIMING CHARACTERISTICS

9-1. Interface timing chart

* 8080 family interface

$V_{DD} = 5 V \pm 10 \%$, $V_{SS} = 0 V$, $T_a = 25 \text{ }^\circ\text{C}$

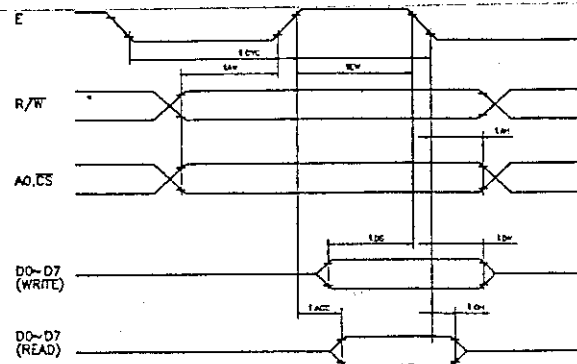
Signal	Symbol	Parameter	Rating		Unit
			min.	max.	
A0, /CS	tAH	Address hold time	10	-	ns
	tAW	Address setup time	30	-	ns
/WR, /RD	tCC	Strobe pulse width	220	-	ns
D0 - D7	tDS	Data setup time	120	-	ns
	tDH	Data hold time	10	-	ns
	tACC	/RD access time	-	120	ns
	tOH	Output disable time	10	50	ns



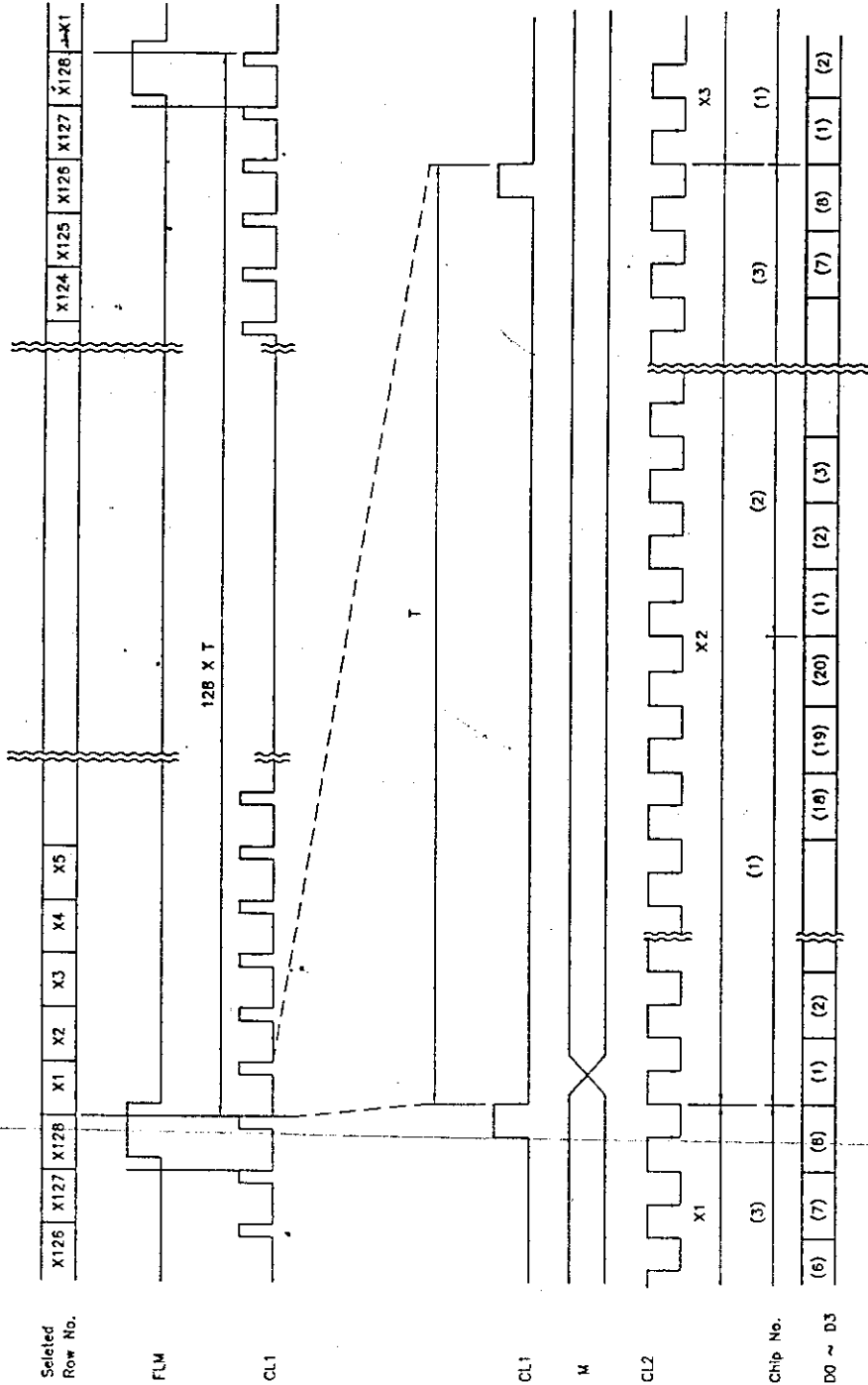
* 6800 family interface

$V_{DD} = 5 V \pm 10 \%$, $V_{SS} = 0 V$, $T_a = 25 \text{ }^\circ\text{C}$

Signal	Symbol	Parameter	Rating		Unit
			min.	max.	
A0, /CS	tAW	Address setup time	30	-	ns
R/ \bar{W}	tAH	Address hold time	10	-	ns
D0-D7	tDS	Data setup time	120	-	ns
	tDH	Data hold time	10	-	ns
	tOH	Output disable time	10	50	ns
	tACC	Access time	-	120	ns
E	tEW	Enable pulse width	220	-	ns



10-2. AC electrical characteristics



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11. INSTRUCTION SETS

Class	Command	Code												Hex	Description
		/RD	/WR	A0	D7	D6	D5	D4	D3	D2	D1	D0			
System Control	SYSTEMSET	1	0	1	0	1	0	0	0	0	0	0	0	40	Initialize device and display.
	SLEEP IN	1	0	1	0	1	0	1	0	0	1	1	53	Enter standby mode.	
Display Control	DISP ON/OFF	1	0	1	0	1	0	1	1	0	0	D	58 59	Enable and disable display and display flashing.	
	SCROLL	1	0	1	0	1	0	0	0	1	0	0	44	Set display start address and display regions.	
	CSRFORM	1	0	1	0	1	0	1	1	1	0	1	5D	Set cursor type.	
	CGRAM ADR	1	0	1	0	1	0	1	1	1	0	0	5C	Set start address of character generator RAM.	
	CSRDIR	1	0	1	0	1	0	0	1	1	C D 1	C D 0	4C to 4F	Set direction of cursor movement.	
	HDOT SCR	1	0	1	0	1	0	1	1	0	1	0	5A	Set horizontal scroll position.	
	OVLAY	1	0	1	0	1	0	1	1	0	1	1	5B	Set display overlay format.	
Drawing Control	CSRW	1	0	1	0	1	0	0	0	1	1	0	46	Set cursor address.	
	CSRR	1	0	1	0	1	0	0	0	1	1	1	47	Read cursor address.	
Memory Control	MWRITE	1	0	1	0	1	0	0	0	0	1	0	42	Write to display memory.	
	MREAD	1	0	1	0	1	0	0	0	0	1	1	43	Read from display memory.	

11-1. SYSTEM CONTROL COMMANDS

11-1-1. SYSTEM SET

Initializes the device, sets the window sizes and selects the LCD interface format. Since this command sets the basic operating parameters of the E-1330, an incorrect SYSTEM SET command may cause other commands to operate incorrectly.

	MSB	D7	D6	D5	D4	D3	D2	D1	LSB	D0
C		0	1	0	0	0	0	0	0	0
P1		0	0	IV	1	W/S	M2	M1	M0	
P2		WF	0	0	0	←		FX	→	
P3		0	0	0	0	←		FY	→	
P4		←						C/R		→
P5		←						TC/R		→
P6		←						L/F		→
P7		←						APL		→
P8		←						APH		→

11-1-1-1. C

This control byte performs the following.

1. Resets the internal timing generator.
2. Disables the display.
3. Cancels sleep mode...

The parameters following P1 are not needed to cancel sleep mode.

11-1-1-2. M0

Selects the internal or external character generator ROM. The internal character generator ROM contains 160, 5×7-pixel characters as shown in character font. These characters are fixed at fabrication by the metalization mask. The external character generator ROM, on the other hand, can contain up to 256 user-defined characters.

M0 = 0 : Internal CG ROM

M0 = 1 : External CG ROM

Note that if the CG ROM address space overlaps the display memory address space, that portion of the display memory cannot be written to.

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11-1-1-3. M1

Selects the memory configuration for user-definable characters. The CG RAM codes select one of the 64 codes.

M1 = 0 : No D6 correction

The CG RAM1 and CG RAM2 address spaces are contiguous. The CG RAM1 address space is treated as character generator RAM and the CG RAM2 address space is treated as character generator ROM.

M1 = 1 : D6 correction

The CG RAM1 and CG RAM2 address spaces are contiguous and both treated as character generator RAM.

11-1-1-4. M2

Selects the height of the character bitmaps. Characters more than 16 pixels high can be displayed by creating a bitmap for each portion of each character and using the E-1330's graphics mode to reposition them.

M2 = 0 : 8 pixel character height.

M2 = 1 : 16-pixel character height.

11-1-1-5. W/S

Selects the LCD drive method.

W/S = 0 : Single-panel drive

W/S = 1 : Two-panel drive

11-1-1-6. IV

Screen origin compensation for inverse display. IV is usually set to 1. The best way of displaying inverted characters is to Exclusive-OR the text layer with the graphics background layer. However, inverted characters at the top or left of the screen are difficult to read as the character origin is at the top-left of its bitmap and there are no background pixels either above or to the left of these character.

The IV flag causes the E-1330 to offset the text screen against the graphics back layer by one vertical pixel.

Use the horizontal pixel scroll function (HDOT SCR) to shift the text screen 1 to 7 pixels to the right. All characters will then have the necessary surrounding background pixels that ensure easy reading of the inverted characters.

IV = 0 : Screen top-line correction

IV = 1 : No screen top-line correction

11-1-1-7. FX

hex	FX				[FX] character width
	D3	D2	D1	D0	(pixels)
00	0	0	0	0	1
01	0	0	0	1	2
↓	↓	↓	↓	↓	↓
07	0	1	1	1	8

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11-1-1-8. WF

Selects the AC frame drive waveform period, WF is usually set to 1.

WF = 0 : 16-line AC drive

WF = 1 : two-frame AC drive

In two-frame AC drive, the WF period is twice the frame period.

In 16-line AC drive, WF inverts every 16 lines.

Although 16-line AC drive gives a more readable display, horizontal lines may appear when using high LCD drive voltages or at high viewing angles.

11-1-1-9. FY

FY					(FY) character height (pixels)
HEX	D3	D2	D1	D0	
00	0	0	0	0	1
01	0	0	0	1	2
↓	↓	↓	↓	↓	↓
07	1	1	1	1	8
↓	↓	↓	↓	↓	↓
0E	1	1	1	0	15
0F	1	1	1	1	16

11-1-1-10. C/R

C/R									[C/R] bytes per display line
HEX	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
4F	0	1	0	0	1	1	1	1	80
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
EE	1	1	1	0	1	1	1	0	239
EF	1	1	1	0	1	1	1	1	240

11-1-1-11. TC/R

TC/R									[TC/R] line length(bytes)
HEX	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
52	0	1	0	1	0	0	1	0	80
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

-1-1-12. L/F

HEX	L/F								[L/F]
	D7	D6	D5	D4	D3	D2	D1	D0	lines per frame
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
7F	0	1	1	1	1	1	1	1	128
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

If W/S is set to 1, thus selecting two-screen display, the number of lines must be even and L/F must, therefore, be an odd number.

1-1-13. AP

Defines the horizontal address range of the virtual screen as shown in the following table. APL is the least significant byte of the address.

APL	AP7	AP6	AP5	AP4	AP3	AP2	AP1	AP0
-----	-----	-----	-----	-----	-----	-----	-----	-----

APH	AP15	AP14	AP13	AP12	AP11	AP10	AP9	AP8
-----	------	------	------	------	------	------	-----	-----

-- AP parameters --

Hex code				[AP]
APH		APL		address per line
0	0	0	0	0
0	0	0	1	1
↓	↓	↓	↓	↓
0	0	5	0	80
↓	↓	↓	↓	↓
F	F	F	E	$2^{10} - 2$
F	F	F	F	$2^{16} - 1$

11-1-2. SLEEP IN

Puts the device into the sleep state. This command has no parameter bytes. At least one blank frame after receiving this command, the E-1330 halts all internal operations, including the oscillator, and enters the sleep state. Blank data is sent to the X-drivers, and the Y-drivers have their bias supplies turned off by the YDIS signal. Using the YDIS signal to disable the Y-drivers guards against any spurious displays.

The internal registers of the E-1330 maintain their values during the sleep state. The display memory control pins maintain their logic levels to ensure that the display memory is not corrupted.

The E-1330 can be removed from the sleep state by sending the SYSTEM SET command with only the PI parameter. The DISP ON command should be sent next to enable the display.

MSB		LSB
C	0 1 0 1 0 0 1 1	

-- SLEEP IN command --

1. The YDIS signal goes LOW between one and two frames after the SLEEP IN command is received. Since YDIS forces all display driver output voltage, YDIS can be used as a power-down signal for the LCD unit. This can be done by having YDIS turn off the relatively high-power LCD drive supplies at the same time as it blanks the display.
2. Since all internal clocks in the E-1330 are halted while in the sleep state, a DC voltage will be applied to the LCD panel if the LCD drive supplies remain on. If reliability is a prime consideration, turn off the LCD drive supplies before issuing the SLEEP IN command.
3. Note that, although the bus lines become high impedance in the sleep state, pull-up or pull-down resistors on the bus will force these lines to a known state.

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11-2. DISPLAY CONTROL COMMANDS

11-2-1. DISP ON/OFF

Turns the whole display on or off. The single-byte parameter enables and disables the cursor and layered screens, and sets the cursor and screen flash rates. The cursor can be set to flash over one character or over a whole line.

	MSB							LSB
C	0	1	0	1	1	0	0	0
P1	FP5	FP4	FP3	FP2	FP1	FP0	FC1	FC0

-- DISP ON/OFF command --

11-2-1-1. D

Turns the display ON or OFF. The D bit takes precedence over the FP bits in the parameter.

D = 0 : Display OFF

D = 1 : Display ON

11-2-1-2. FC

Enables/disables the cursor and sets the flash rate as shown in the following table. The cursor flashes with a 70% duty cycle (ON/OFF).

FC1	FC0	Cursor display	
0	0	OFF (blank)	
0	1	ON	No flashing
1	0		Flash at $f_{FR}/32$ Hz (approx. 2 Hz)
1	1		Flash at $f_{FR}/64$ Hz (approx. 1 Hz)

11-2-1-3. FP

Each pair of bits in FP sets the attributes of one screen block as shown in the following table.

FP1	FP0	First screen block (SAD1)	
FP3	FP2	Second screen block (SAD2, DAD4). See note.	
FP5	FP4	Third screen block (SAD3)	
0	0	OFF (blank)	
0	1	ON	No flashing
1	0		Flash at $f_{FR}/32$ Hz (approx. 2 Hz)
1	1		Flash at $f_{FR}/4$ Hz (approx. 17 Hz)

Note

If SAD4 is enabled by setting W/S to 1, FP3 and FP2 control both SAD2 and SAD4.

The attributes of SAD2 and SAD4 cannot be set independently.

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11-2-2. SCROLL

11-2-2-1. C

Sets the scroll start address and the number of lines per scroll block as shown in the following table. Parameters P1 to P10 can be omitted if not required.

	MSB								LSB	
C	0	1	0	0	0	1	0	0		
P1	A7	A6	A5	A4	A3	A2	A1	A0	(SAD 1 L)	
P2	A15	A14	A13	A12	A11	A10	A9	A8	(SAD 1 H)	
P3	L7	L6	L5	L4	L3	L2	L1	L0	(SL 1)	
P4	A7	A6	A5	A4	A3	A2	A1	A0	(SAD 2 L)	
P5	A15	A14	A13	A12	A11	A10	A9	A8	(SAD 2 H)	
P6	L7	L6	L5	L4	L3	L2	L1	L0	(SL 2)	
P7	A7	A6	A5	A4	A3	A2	A1	A0	(SAD 3 L)	
P8	A15	A14	A13	A12	A11	A10	A9	A8	(SAD 3 H)	
P9	A7	A6	A5	A4	A3	A2	A1	A0	(SAD 4 L)	
P10	A15	A14	A13	A12	A11	A10	A9	A8	(SAD 4 H)	

(SCROLL COMMAND)

Note

Set the parameter P9 and P10 only if both two-screen drive(W/S=1) and two-layer configuration are selected. SAD4 is the fourth screen block display start address.

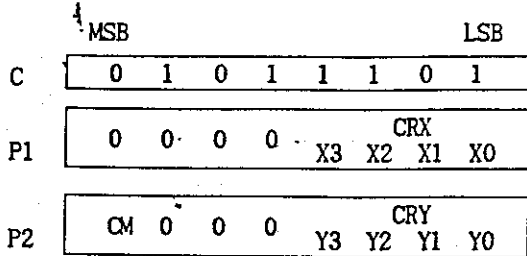
11-2-2-2. SL1, SL2

SL1 and SL2 set the number of lines per scrolling screen. the number of lines is SL1 or SL2, plus one.

HEX	SL1,SL2								(SL)Screen lines
	L7	L6	L5	L4	L3	L2	L1	L0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
7F	0	1	1	1	1	1	1	1	128
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

11-2-3. CSRFORM

Sets the cursor size and shape. Although the cursor is normally used only in text displays, it can also be used in graphics display when displaying special characters.



11-2-3-1. CRX

Sets the horizontal size of the cursor from the character origin as shown in the following table. CRX is equal to the cursor size less one. CRX must be less than or equal to FX.

HEX	CRX				(CRX) cursor width (pixels)
	X3	X2	X1	X0	
0	0	0	0	0	1
1	0	0	0	1	2
↓	↓	↓	↓	↓	↓
4	0	1	0	0	9
↓	↓	↓	↓	↓	↓
E	1	1	1	0	15
F	1	1	1	1	16

11-2-3-2. CRY

Sets the location of an underscored cursor, in lines, from the character origin as shown in the following table. When using a block cursor, CRY sets the vertical size of the cursor from the character origin. CRY is equal to the number of lines less one.

HEX	CRY				(CRY) cursor width (pixels)
	Y3	Y2	Y1	Y0	
0	0	0	0	0	Illegal
1	0	0	0	1	2
↓	↓	↓	↓	↓	↓
8	1	0	0	0	9
↓	↓	↓	↓	↓	↓
E	1	1	1	0	15
F	1	1	1	1	16

11-2-3-3. CM

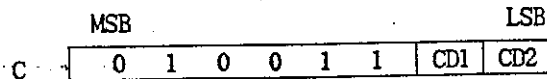
Sets the cursor shape. Always set CM to 1 when in graphics mode.

CM = 0 : Underscore cursor

CM = 1 : Block cursor

11-2-4. CSDIR

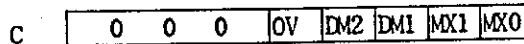
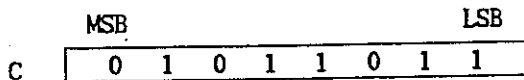
Sets the direction of automatic cursor increment as shown in the following table. The cursor can move left or right one character, or up or down by the number or bytes specified by the address pitch, AP.



C	CD1	CD2	Shift direction
4CH	0	0	Right
4DH	0	1	Left
4EH	1	0	Up
4FH	1	1	Down

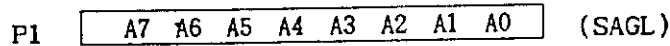
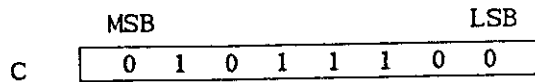
11-2-5. OVLAY

Selects layered screen composition and screen text/graphics mode.



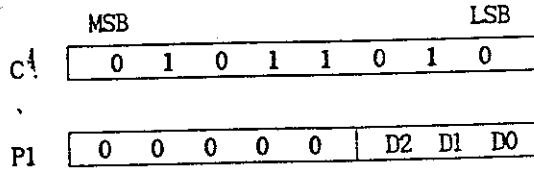
11-2-6. CGRAM ADR

Specifies the CG RAM start address.



11-2-7. HDOT SCR

While the SCROLL command only allows scrolling by characters, HDOT SCR allows the screen to be scrolled horizontally by pixels. HDOT SCR cannot be used on individual layers.



11-2-7-1. D0 to D2

Specifies the number of pixels to scroll as shown in the following table. The C/R parameter has to be set to the number of horizontal characters plus one before using HDOT SCR.

HEX	P1			Number of pixels to scroll
	D2	D1	D0	
00	0	0	0	0
01	0	0	1	1
02	0	1	0	2
↓	↓	↓	↓	↓
06	1	1	0	6
07	1	1	1	7

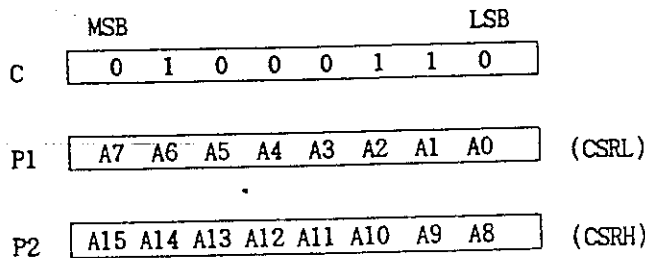
11-3. DRAWING CONTROL COMMANDS

11-3-1. CSRW

The 16bit cursor address register contains the display memory address of the data at the cursor position.

Note that the microprocessor cannot directly access the display memory.

The MREAD and MWRITE commands use the address in the register.

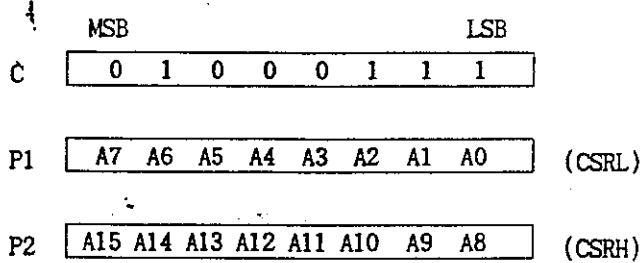


The cursor address register can only be modified by the CSRW command and by the automatic increment after an MREAD or MWRITE command. It is not affected by display scrolling.

If a new address is not set, display memory accesses will be from the last set address or address after previous automatic increments.

11-3-2. CSRR

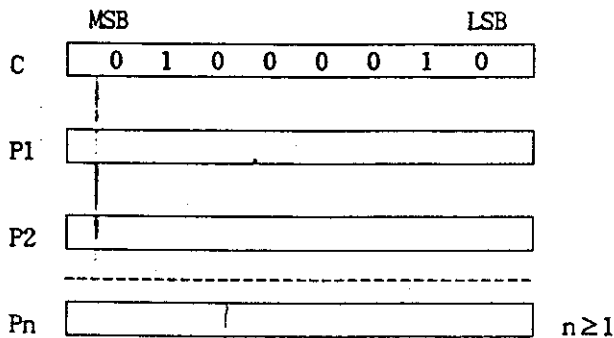
Read from the cursor address register. After issuing the command, the data read address is read twice, for the low byte and then the high byte of the register.



11-4. MEMORY CONTROL COMMANDS

11-4-1. MWRITE

The microprocessor may write a sequence of data bytes to display memory by issuing the MREAD command and then writing the bytes to the E-1330. There is no need for further MWRITE commands for the microprocessor to update the cursor address register after each byte as the cursor address is automatically incremented by the amount set with CSRDIR, in preparation for the next data write.



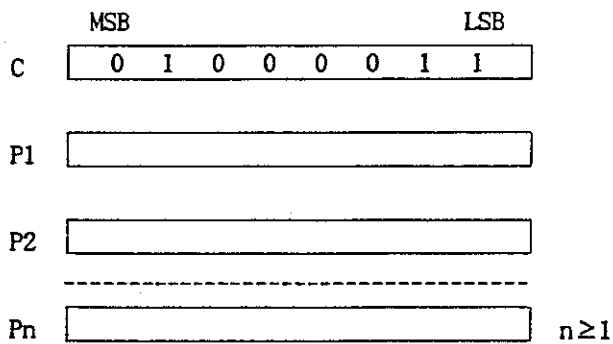
Note

P1, P2, ..., Pn : Display data

11-4-2. MREAD

Puts the E-1330 into the data output state. On the MREAD command, the display memory data at the cursor address is read into a buffer in the E-1330. Each time the microprocessor reads the buffer the cursor address is incremented by the amount set by CSRDIR and the next data byte fetched from memory, so a sequence of data bytes can be read without further MREAD commands or by updating the cursor address register.

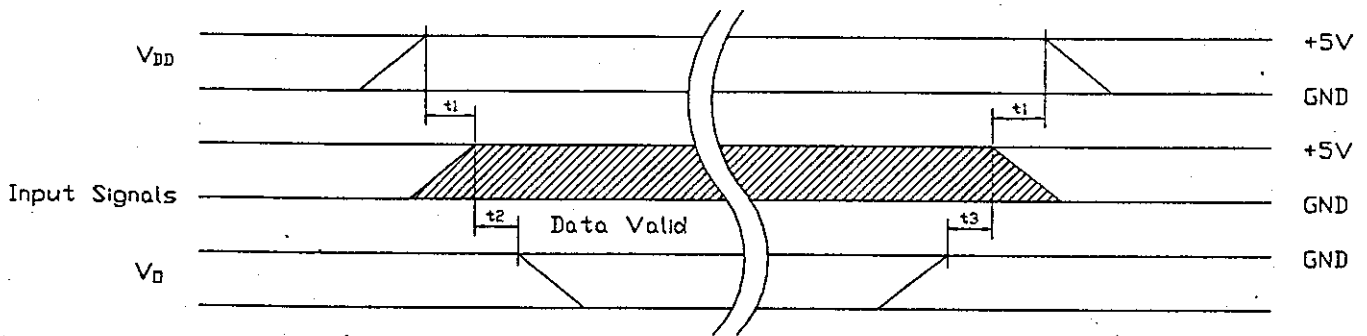
If the cursor is displayed, the read data will be from two positions ahead of the cursor.



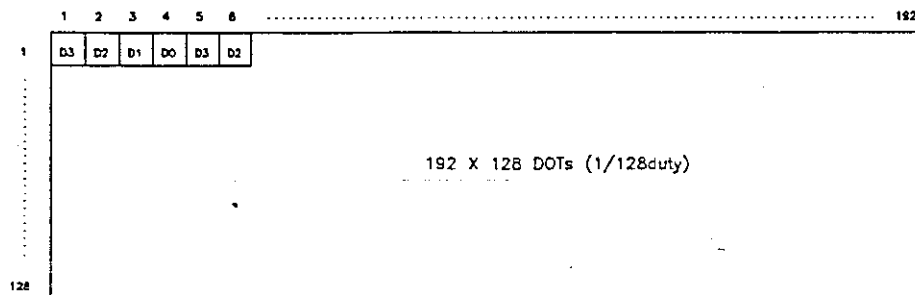
12. Power ON/OFF and signal input timing

Power ON/OFF and signal input should be performed according to the timing shown in the figure below in order not to damage the LCD driving circuit and the LCD panel.

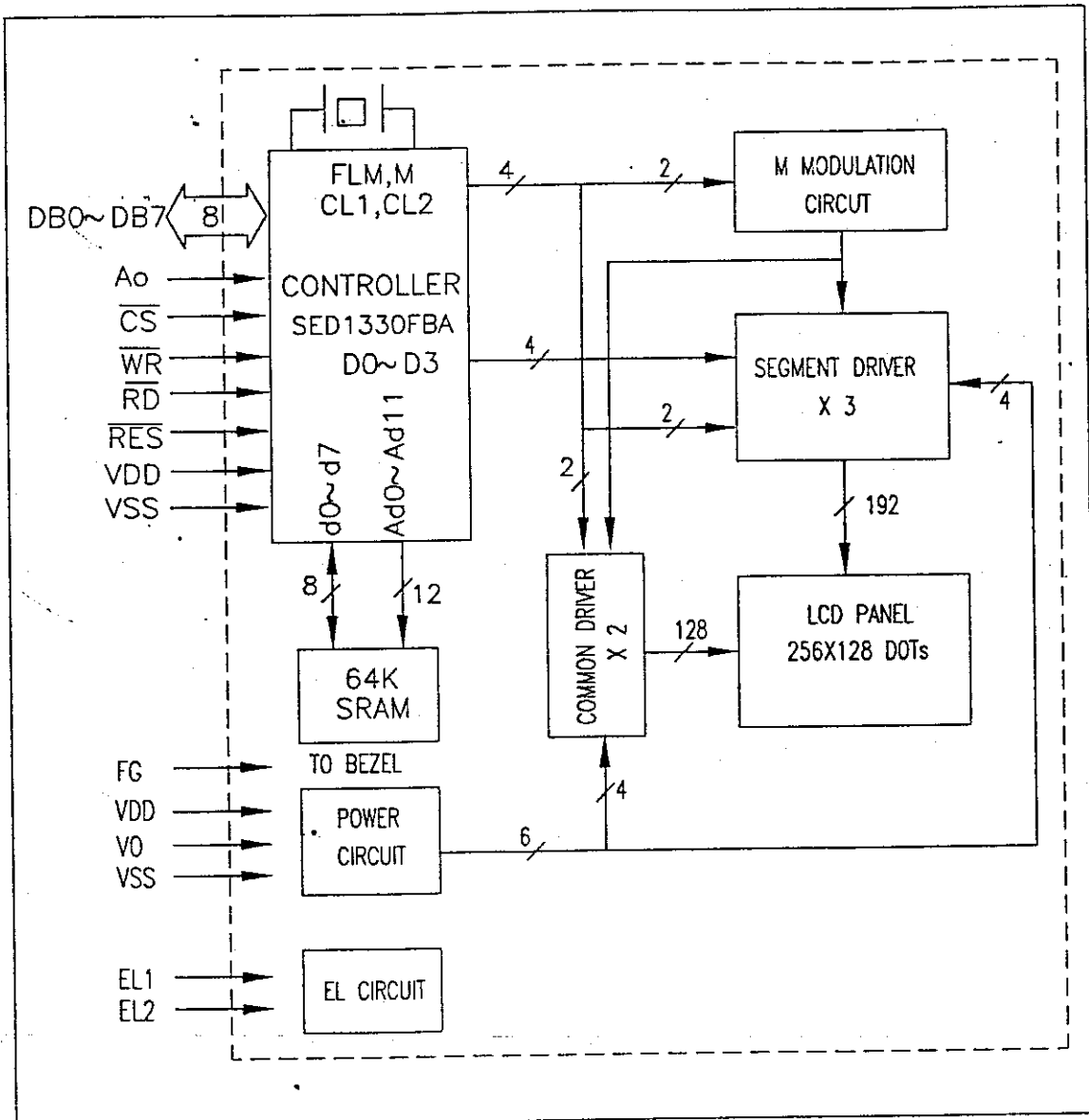
Item	Min.	Max.	Unit
t1	0	20	ms
t2	20	-	ms
t3	0	-	ms



13. RELATION BETWEEN DATA AND DISPLAY



14. BLOCK DIAGRAM



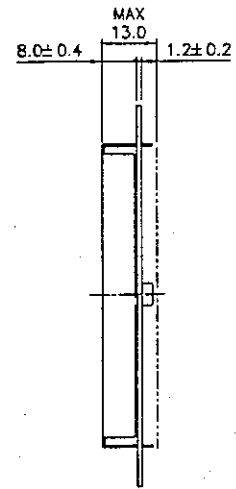
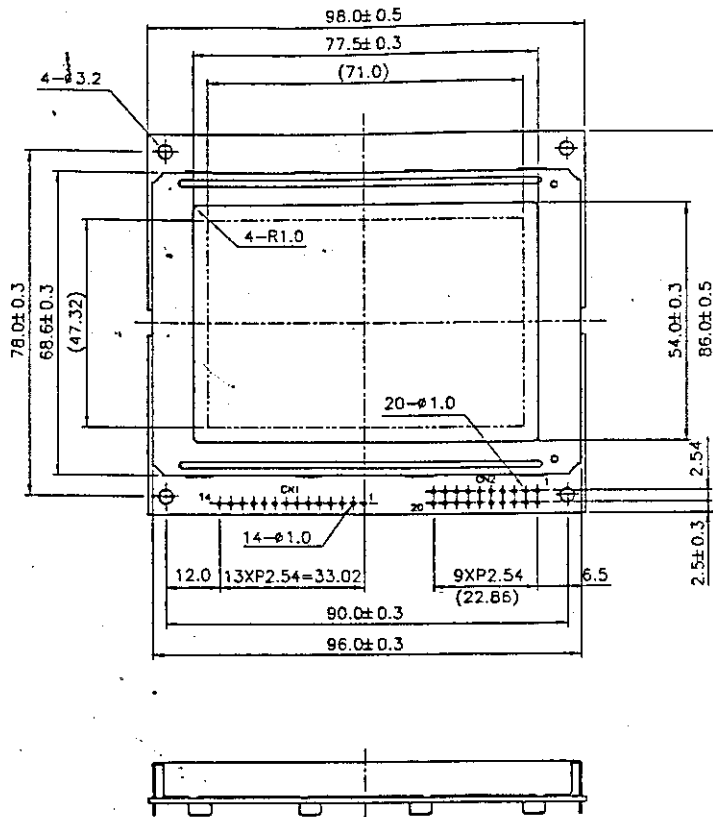
15. CHARACTER FONT MAP

		Character code bits 0 to 3															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Character code bits 4 to 7	2		1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	3	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	4	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	5	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	6	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	7	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	A	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	B	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	C	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	D	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

15. EXTERNAL DIMENSION

Unit : mm

Tolerance : ± 0.1 mm



PIN ASSIGNMENT

Pin No.	Signal (CN1)	Signal (CN2)
1	DB3	FG
2	DB2	V _{SS}
3	FLM	V _{DD}
4	M	V _O
5	CL1	/RES
6	CL2	/RD
7	DB1	/WR
8	DB0	/CS
9	V _{DD}	A0
10	V _{SS}	-DB0
11	V _O	DB1
12	FG	DB2
13	EL1	DB3
14	EL2	DB4
15	-	DB5
16	-	DB6
17	-	DB7
18	-	NC
19	-	EL1
20	-	EL2

DOTS DETAIL

