(주)엘엠솔루션

Brief Data sheet

LMS200

Ver1.0
April 7, 2009

LMSOLUTION Co.,Ltd

Revision History

Date	Rev. Num	Descriptions

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目　　录

1 概要

LMS200是为了进行影像讯号的处理、编辑与存储操作而开发的SoC产品。将输入的BT.656或BT.601 数据接收并处理后显示到 LCD 屏(也可同时透过CVBS输出），或者运行 Full Hardware JPEG Encoding ，将影像数据保存到 SDRAM、Nand Flash Memory 或 SD/MMC Card 里。也可透过读取已保存的影像数据，经由 Full Hardware JPEG Decoding 显示到 LCD 屏。IC 内部的 OSD block 里设置了 Hardware 的高性能绘图核心 (Graphic Engine) 藉由 Nand Flash Memory 或 SD/MMC Card 上的影像数据 (Image Data) 来实现多样化的图像画面。

2 Features

2.1 Video Data Receiver / Transceiver

- 支持 BT.656, BT.601 digital video input
- 支持 BT.656 digital video output 及 CVBS analog output
- 支持 Contrast, Brightness, Saturation, Hue Control
- 可用 External Sync 或 Internal Sync Gen.

2.2 JPEG En/Decoder

- 可支持 NTSC / PAL 制式, 最大为 1024 x 512 resolution
- 对实时输入视频的 MJPEG 支持 (NTSC 时最大可支持 30 fp/s)

2.3 JPEG OSD

- 支持 JPEG 的 OSD
- 支持 16 / 12 / 8 bit per pixel
- 支持 Alpha blending, Chroma-key

2.4 Display OSD

- 支持 Video Output 的 OSD
- 支持 layer, 5 window
- 支持 16 / 12 / 8 bit per pixel
- 支持 Alpha blending, Chroma-key, Blinking

2.5 Scaler

- 对输入及输出视频的自由灵活摆设 active window 功能
- 支持垂直, 水平方向的多样化 scaling factor 功能
- 为了防止 Scaling 时的 image 过热现象,在输入端上适用了 LPF

2.6 Nand Flash Controller

- IIB (Initial Invalid Block) Check / 8bit bus
- 支持 Up to 32Gb
- 支持 ECC (1 bit Error Correction, 2 bit Error Detection)
- Block read to SDRAM / program from SDRAM operation
- Support Nand Flash Direct Access Operation for MCU

2.7 SDRAM Controller

- 16bit Data bus
- Up to 512Mb

2.8 SD / MMC Card Interface

- 支持 SD Card (ver 2.0) / MMC Card (ver 3.31)
- 支持 1 bit Data line
- Single / Multi Block Read / Write

2.9 Internal MCU (Turbo 8051)

- Two clocks per machine cycle
- 支持 UISP / Nand Boot 功能
- 4Kbyte External Data Memory / 256byte Internal Data Memory
- 4Kbyte Boot Program Memory / 64Kbyte Program Memory

2.10 RTC

- Programmable YEAR / MONTH / DAY / HOUR / MINUTE / SECOND
- 支持 Calibration 功能

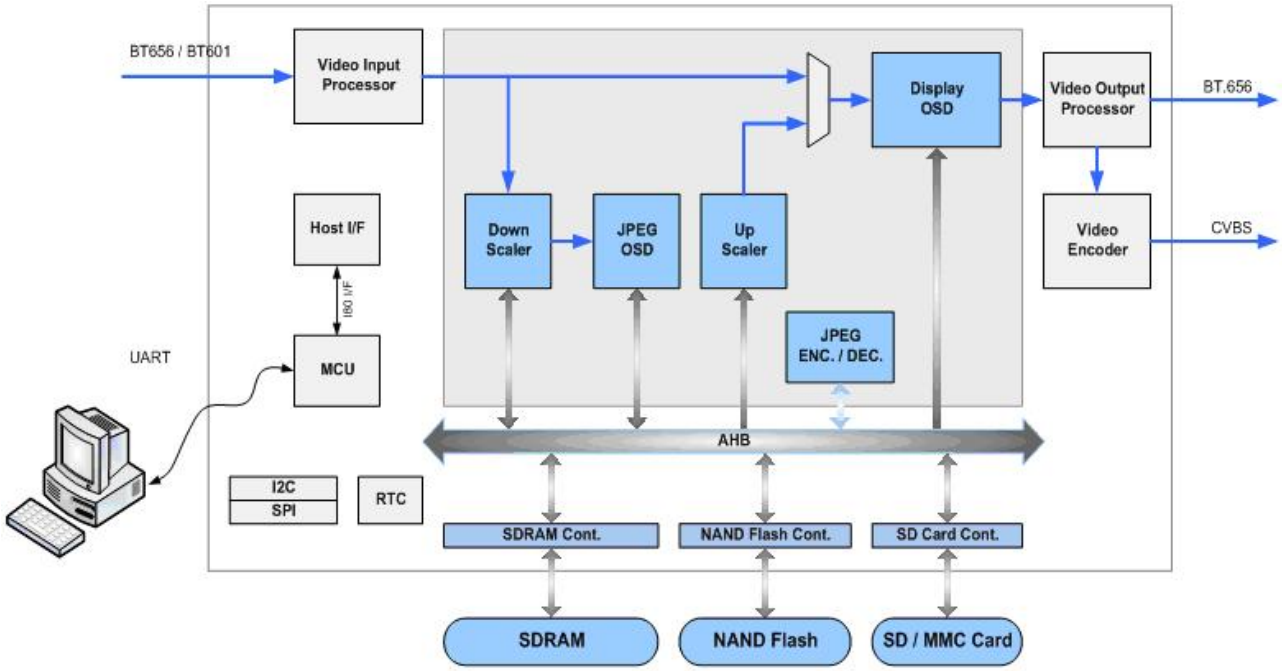
2.11 Peripheral

- I80 bus interface
- SPI
- I2C
- UART
- GPIO

2.12 Clock and Power Management

- Internal PLL
- 支持 Power Down Mode (RTC power 除外)

3 Block Diagram



4 Package & Pin Description

4.1 Pin Description

Pin No.	Pin Name	I/O	Description
System Interface			
102	RESETx	I	System Reset (Active Low)
103	P_DOWN	I	Power Down (Active High)
106	S_IMCU	I	Select Internal MCU (Active High)
104	XCLK_I	I	External Crystal Input (System Clock)
105	XCLK_O	O	External Crystal Output
125	XRTC_I	I	External Crystal Input (RTC Clock)
126	XRTC_O	O	External Crystal Output
MCU Interface			
115	MCU_ALE	I	Address Latch Enable
114	MCU_WEx	I	Write Enable
113	MCU_REx	I	Read Enable
123	MCU_DATA[0]	I/O	Address / Data Bus
122	MCU_DATA[1]	I/O	Address / Data Bus
121	MCU_DATA[2]	I/O	Address / Data Bus
120	MCU_DATA[3]	I/O	Address / Data Bus
119	MCU_DATA[4]	I/O	Address / Data Bus
118	MCU_DATA[5]	I/O	Address / Data Bus
117	MCU_DATA[6]	I/O	Address / Data Bus
116	MCU_DATA[7]	I/O	Address / Data Bus
124	MCU_INT	O	Interrupt (Active High)
Video Interface			
41	VI_CLK	I	Video Input Clock
30	FIELD_IN	I	Field Signal
31	VSYNC_IN	I	Vertical Sync
32	HSYNC_IN	I	Horizontal Sync
33	VDATA_IN[0]	I	Video Input Data
34	VDATA_IN[1]	I	Video Input Data
35	VDATA_IN[2]	I	Video Input Data
36	VDATA_IN[3]	I	Video Input Data

37	VDATA_IN[4]	I	Video Input Data
38	VDATA_IN[5]	I	Video Input Data
39	VDATA_IN[6]	I	Video Input Data
40	VDATA_IN[7]	I	Video Input Data
99	VO_CLK	O	Video Output Clock
91	VDATA_OUT[0]	O	Video Output Data
92	VDATA_OUT[1]	O	Video Output Data
93	VDATA_OUT[2]	O	Video Output Data
94	VDATA_OUT[3]	O	Video Output Data
95	VDATA_OUT[4]	O	Video Output Data
96	VDATA_OUT[5]	O	Video Output Data
97	VDATA_OUT[6]	O	Video Output Data
98	VDATA_OUT[7]	O	Video Output Data
SDRAM Interface			
164	SDCLKOUT	O	SDRAM Clock
156	SDCSx	O	Chip Select
157	SDRASx	O	Row Address Strobe
158	SDCASx	O	Column Address Strobe
159	SDWEx	O	Write Enable
160	SDDQM[0]	O	Data Input/Output Masking Enable
161	SDDQM[1]	O	Data Input/Output Masking Enable
162	SDBA[0]	O	Bank Select Address
163	SDBA[1]	O	Bank Select Address
5	SDADDR[0]	O	Address Bus
4	SDADDR[1]	O	Address Bus
3	SDADDR[2]	O	Address Bus
2	SDADDR[3]	O	Address Bus
1	SDADDR[4]	O	Address Bus
176	SDADDR[5]	O	Address Bus
175	SDADDR[6]	O	Address Bus
174	SDADDR[7]	O	Address Bus
173	SDADDR[8]	O	Address Bus
172	SDADDR[9]	O	Address Bus
167	SDADDR[10]	O	Address Bus
166	SDADDR[11]	O	Address Bus

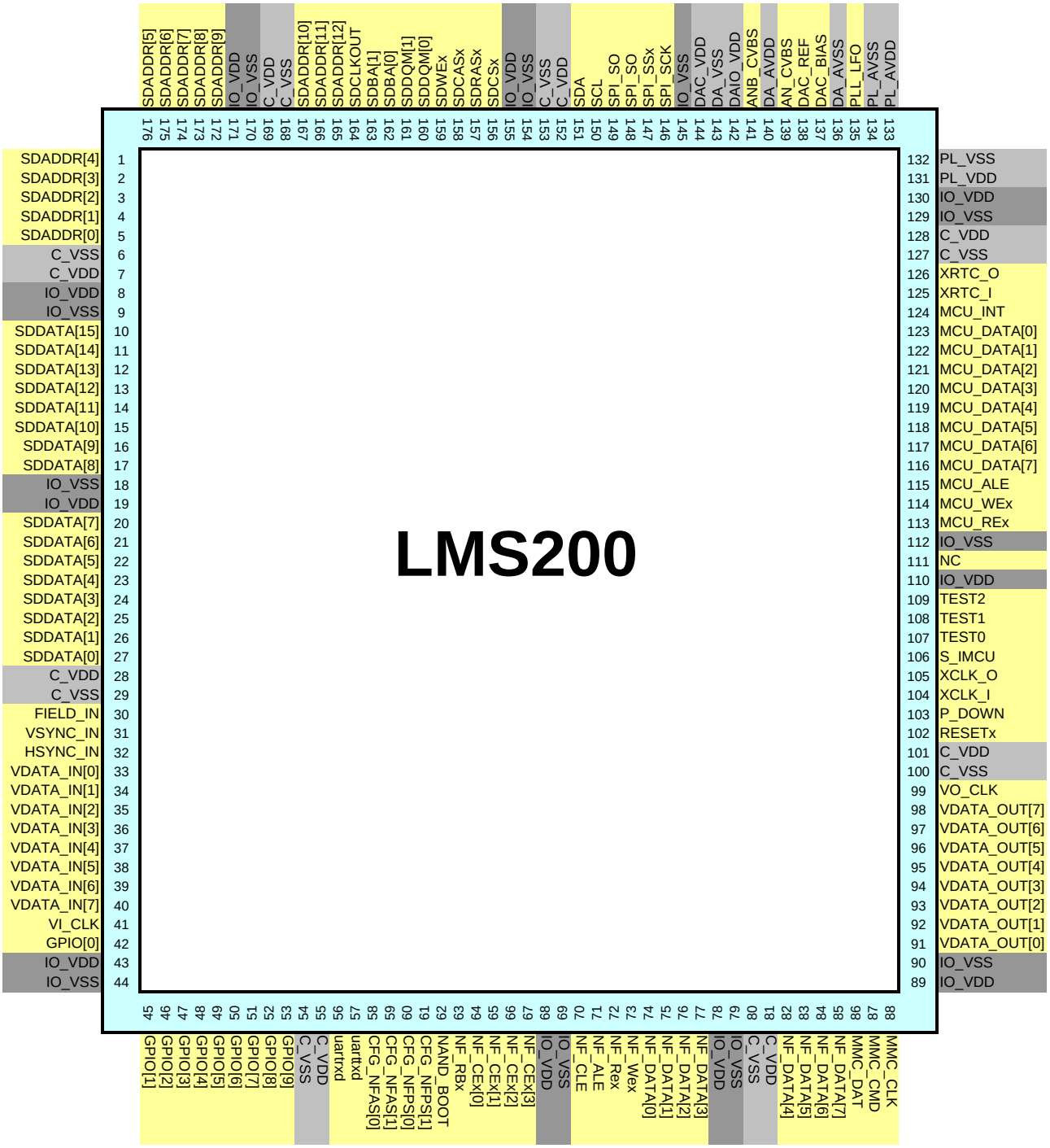
165	SDADDR[12]	O	Address Bus
27	SDDATA[0]	I/O	Data Bus
26	SDDATA[1]	I/O	Data Bus
25	SDDATA[2]	I/O	Data Bus
24	SDDATA[3]	I/O	Data Bus
23	SDDATA[4]	I/O	Data Bus
22	SDDATA[5]	I/O	Data Bus
21	SDDATA[6]	I/O	Data Bus
20	SDDATA[7]	I/O	Data Bus
17	SDDATA[8]	I/O	Data Bus
16	SDDATA[9]	I/O	Data Bus
15	SDDATA[10]	I/O	Data Bus
14	SDDATA[11]	I/O	Data Bus
13	SDDATA[12]	I/O	Data Bus
12	SDDATA[13]	I/O	Data Bus
11	SDDATA[14]	I/O	Data Bus
10	SDDATA[15]	I/O	Data Bus
NAND Flash Memory Interface			
58	CFG_NFAS[0]	I	Address Size Configuration Pin “00” : 3 Cycle “01” : 4 Cycle “10” : 5 Cycle
59	CFG_NFAS[1]	I	
60	CFG_NFPS[0]	I	Page Size Configuration Pin “00” : 512 + 16 Byte “01” : 2K + 64 Byte “10” : 4K + 128 Byte
61	CFG_NFPS[1]	I	
62	NAND_BOOT	I	Nand Boot Enable “S_IMCU” pin 为 high 时 internal mcu 是从 nand flash memory 里读取 program data, 为 low 时以 UISP mode 工作并通过 UART 通信来读取 program data.
64	NF_CEx[0]	O	Chip Enable
65	NF_CEx[1]	O	Chip Enable
66	NF_CEx[2]	O	Chip Enable
67	NF_CEx[3]	O	Chip Enable
63	NF_RBx	I	Ready / Busy

70	NF_CLE	O	Command Latch Enable
71	NF_ALE	O	Address Latch Enable
72	NF_REx	O	Read Enable
73	NF_WEx	O	Write Enable
74	NF_DATA[0]	I/O	Address / Data Bus
75	NF_DATA[1]	I/O	Address / Data Bus
76	NF_DATA[2]	I/O	Address / Data Bus
77	NF_DATA[3]	I/O	Address / Data Bus
82	NF_DATA[4]	I/O	Address / Data Bus
83	NF_DATA[5]	I/O	Address / Data Bus
84	NF_DATA[6]	I/O	Address / Data Bus
85	NF_DATA[7]	I/O	Address / Data Bus
SD / MMC Card Interface			
88	MMC_CLK	O	Clock Line
87	MMC_CMD	I/O	Command Line
86	MMC_DATA	I/O	Data Line
UART			
56	UART_RXD	I	Rx Data Line
57	UART_TXD	O	Tx Data Line
SPI			
147	SPI_SSx	I	Chip Select
146	SPI_SCK	I	Clock Line
149	SPI_SI	I	Input Data Line
148	SPI_SO	O	Output Data Line
I2C			
150	SCL	I	Clock Line
151	SDA	I/O	Data Line
Video Encoder Interface			
137	DAC_BIAS	I	Voltage Reference Input
138	DAC_REF	I	Full-scale Adjust Control
139	AN_CVBS	O	Analog Output
141	ANB_CVBS	O	Complementary Analog Output
其它			
42	GPIO[0]	I/O	General Purpose I/O
45	GPIO[1]	I/O	General Purpose I/O

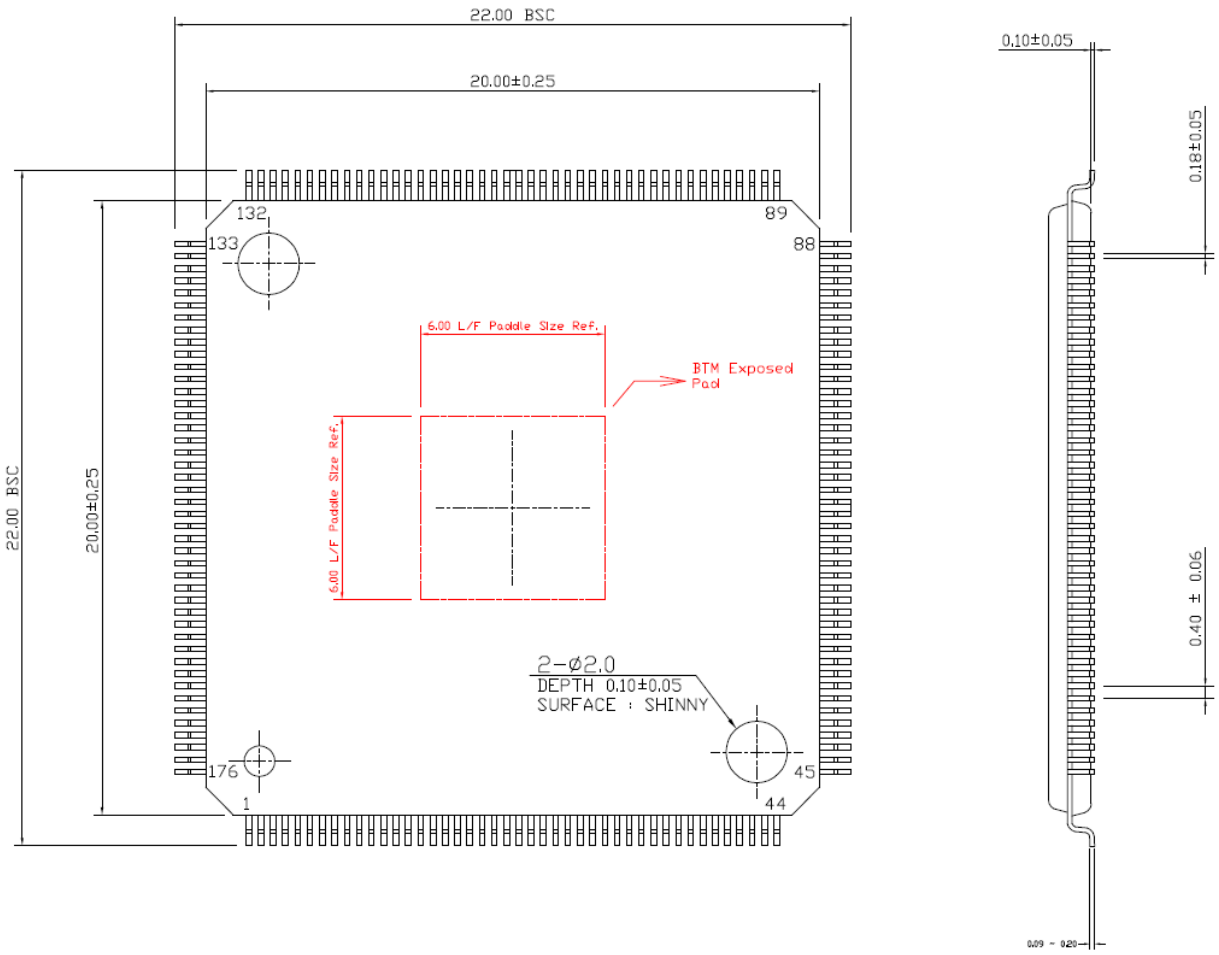
46	GPIO[2]	I/O	General Purpose I/O
47	GPIO[3]	I/O	General Purpose I/O
48	GPIO[4]	I/O	General Purpose I/O
49	GPIO[5]	I/O	General Purpose I/O
50	GPIO[6]	I/O	General Purpose I/O
51	GPIO[7]	I/O	General Purpose I/O
52	GPIO[8]	I/O	General Purpose I/O
53	GPIO[9]	I/O	General Purpose I/O
135	PLL_LFO	O	External loop filter for PLL
107	TEST0	I	Test Pin
108	TEST1	I	Test Pin
109	TEST2	I	Test Pin
6	C_VSS	I	Digital Core Ground
29	C_VSS	I	Digital Core Ground
54	C_VSS	I	Digital Core Ground
80	C_VSS	I	Digital Core Ground
100	C_VSS	I	Digital Core Ground
153	C_VSS	I	Digital Core Ground
168	C_VSS	I	Digital Core Ground
9	IO_VSS	I	Digital I/O Ground
18	IO_VSS	I	Digital I/O Ground
44	IO_VSS	I	Digital I/O Ground
69	IO_VSS	I	Digital I/O Ground
79	IO_VSS	I	Digital I/O Ground
90	IO_VSS	I	Digital I/O Ground
112	IO_VSS	I	Digital I/O Ground
145	IO_VSS	I	Digital I/O Ground
154	IO_VSS	I	Digital I/O Ground
170	IO_VSS	I	Digital I/O Ground
7	C_VDD	I	2.5V Core Power
28	C_VDD	I	2.5V Core Power
55	C_VDD	I	2.5V Core Power
81	C_VDD	I	2.5V Core Power
101	C_VDD	I	2.5V Core Power
152	C_VDD	I	2.5V Core Power

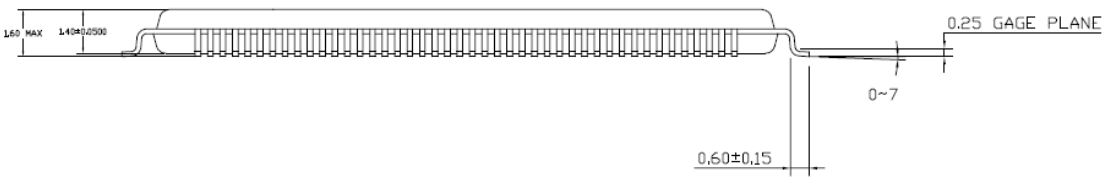
169	C_VDD	I	2.5V Core Power
8	IO_VDD	I	3.3V I/O Power
19	IO_VDD	I	3.3V I/O Power
43	IO_VDD	I	3.3V I/O Power
68	IO_VDD	I	3.3V I/O Power
78	IO_VDD	I	3.3V I/O Power
89	IO_VDD	I	3.3V I/O Power
110	IO_VDD	I	3.3V I/O Power
155	IO_VDD	I	3.3V I/O Power
171	IO_VDD	I	3.3V I/O Power
127	C_VSS	I	RTC Core Ground
129	IO_VSS	I	RTC I/O Ground
128	C_VDD	I	2.5V RTC Core Power
130	IO_VDD	I	3.3V RTC I/O Power
132	PL_VSS	I	PLL Digital Ground
143	DA_VSS	I	DAC Digital Ground
131	PL_VDD	I	2.5V Core Power
144	DAC_VDD	I	2.5V Core Power
142	DAIO_VDD	I	3.3V Core Power
134	PL_AVSS	I	PLL Analog Ground
136	DA_AVSS	I	DAC Analog Ground
133	PL_AVDD	I	2.5V PLL Analog Power
140	DA_AVDD	I	3.3V DAC Analog Power

4.2 Pin Information



4.3 Package Description





5 Electrical Characteristics

5.1 Recommended Operating Condition

Symbol	Parameter	Min	TYP	Max	Unit
V_{DD}	DC Supply Voltage 3.3V Supply 2.5V Supply	 3.0 2.3		 3.6 2.7	V
V_{IN}	Input Voltage Normal 3.3V Input 5V tolerant Input	 0 0		 3.6 5.5	V
V_{OUT}	Output voltage outputs active	0		V_{DD}	V
V_{OUT}	Output voltage outputs disabled	0		5.5	V
T_A	Operating temperature	0		70	℃
V_{IH}	Input High Voltage	2.0			V
V_{IL}	Input Low Voltage			0.8	V
I_{IH}	Input High Current	-10		10	μA
I_{IL}	Input Low Current Input with pull-up	-10 -19	 -36	10 -56	μA
I_{OZ}	3-State Output Leakage Current	-10		10	μA

The I/O pad is LVTTL/LVCMOS compatible.

5.2 Power Consumption

Active Mode	Status	VDD 3.3V	VDD 2.5V	AVDD 3.3V	AVDD 2.5V
Power Down Mode	All Clock Disable	14.6mA	6.8mA	0.27mA	0.1 μA
	MCU Clock Enable	15.4mA	8.1mA	0.27mA	0.1 μA
	SDRAM Clock Enable	15.5mA	18.0mA	0.27mA	0.1 μA
	MCU & SDRAM Clock Enable	15.6mA	19.2mA	0.27mA	0.1 μA
Maximum Operation Mode	50MHz SDRAM Clock	28.0mA	119mA	[1)]28.0mA	1.9mA
	60MHz SDRAM Clock	29.6mA	128mA	[1)]28.0mA	2.3mA
	70MHz SDRAM Clock	29.8mA	141mA	[1)]28.0mA	2.6mA
	80MHz SDRAM Clock	31.0mA	157mA	[1)]28.0mA	3.0mA

1)使用 Internal Video Encoder

6 Register Summary

Address	Name	7	6	5	4	3	2	1	0
0x000	SYSID	CHIP_ID							
0x001	SYSCK	S_SD			NU	S_VI		N_VO	N_VI
0x002		S_JP		S_VO			S_MCU		
0x003	SDCK	SDRCK				SDWCK			
0x004	MMCCK	CKEN	CKRATIO						
0x005	SWRST	R_MMC	R_SD	R_JP	R_VO	R_VI	R_HOST	NU	R_SW
0x006		NU					R_PLL	R_MCU	R_NFC
0x007	MCU_CONT	PLL_LK	NU					M_WAIT	
0x008	AN_CONT	PL_TDM	PL_LFM			PL_BP	PV_PD	PL_PD	DA_PD
0x009	PLL_CONT	PL_M[7:0]							
0x00A		PL_TINIT	PL_M[13:8]						
0x00B		PL_N[7:0]							
0x00C		PL_ICP				PL_VC		PL_P	
0x00D	PAGESEL	NU							PS
0x00E	XBUF_CON	NU	SD_SEL			ID		R/W	EN
0x00F	HOSTRW_DAT	RW_DATA							
0x010	RTCCON	NU					RDEN	WREN	RTCEN
0x011	CALIB	SIGN	CALIB						
0x012	WSEC	NU		WSEC					
0x013	WMIN	NU		WMIN					
0x014	WHOUR	NU			WHOUR				
0x015	WDATE	NU			WDATE				
0x016	WMON	NU				WMON			
0x017	WYEAR	NU	WYEAR						
0x018	RSEC	NU		RSEC					
0x019	RMIN	NU		RMIN					
0x01A	RHOUR	NU			RHOUR				
0x01B	RDATE	NU			RDATE				
0x01C	RMON	NU				RMON			
0x01D	RYEAR	NU	RYEAR						
0x01E	RYEAR	WR_CODE							
0x020	VICON	NU	SELVOS	FPOL	VPOL	HPOL	SELIN	INOD	
0x021	VOCON	NU		EN_VE	SELOD			OTOD	
0x022		NU				FPOL	VPOL	HPOL	NU
0x024	VIPOPC	NU			JOEN	DSEN	VIEN	UP_JOSD	UP_DS
0x025		JOOM	JOMO	DMASM	DMAEN	DSMO	DSFM	DSOM	
0x026	VIPOCNT	NU	STTCNT			NU	SKCNT		
0x027	VIPIE	NU		JOSIE	JODIE	DSSIE	DSDIE	FMSIE	FLSIE
0x028	VIPI	NU		JOSI	JODI	DSSI	DSDI	FMSI	FLSI
0x029	VOPOPC	USFM	SELUSB		USEN	GFTEN	VOEN	UP_DO	UP_US
0x02A		NU			DOEN				
0x02B		NU		JDECEN	JPPS	SELJEB		JDEN	JEEN
0x02C	VOPOCNT	NU	STTCNT			NU	SKCNT		
0x02D	JPCNT	JPCNT[7:0]							
0x02E		JPCNT[15:8]							
0x02F	JPDCNT	JPDCNT[7:0]							
0x030		JPDCNT[15:8]							
0x031	JPECNT	JPECNT[7:0]							
0x032	VOPIE	JPSIE	JPDIE	DOSIE	DODIE	USSIE	USDIE	FMSIE	FLSIE
0x034	VOPI	JPSI	JPDI	DOSI	DODI	USSI	USDI	FMSI	FLSI
0x038	GenFTC	NU				SGVF	STIS	ISEN	SVO
0x039	MAXSZ	MAXVS[7:0]							
0x03A		MAXHS[7:0]							
0x03B		NU				MAXHS[9:8]		MAXVS[9:8]	
0x03C	FH	FH[7:0]							
0x03D		NU						FH[9:8]	
0x03E	VSP	VL0[7:0]							
0x03F		VH0[7:0]							
0x040		VL1[7:0]							
0x041		VH1[7:0]							
0x042		VH1[9:8]		VL1[9:8]		VH0[9:8]		VL0[9:8]	
0x043	HSP	HL[7:0]							
0x044		HH[7:0]							
0x045		DL[7:0]							
0x046		DH[7:0]							
0x047		DH[9:8]		DL[9:8]		HH[9:8]		HL[9:8]	
0x048	DSLPFC	NU						VLEN	HLEN
0x049	DSSR	DSVR[7:0]							

Address	Name	7	6	5	4	3	2	1	0
0x04A		DSHR[7:0]							
0x04B	DSSIZE	DSVMS[7:0]							
0x04C		DSHMS[7:0]							
0x04D		DSVAS[7:0]							
0x04E		DSHAS[7:0]							
0x04F		DSHAS[9:8]		DSVAS[9:8]		DSHMS[9:8]		DSVMS[9:8]	
0x050	USSR	NU			USVR[4:0]				
0x051		NU			USHR[4:0]				
0x052	USSIZE	USVMS[7:0]							
0x053		USHMS[7:0]							
0x054		USVAS[7:0]							
0x055		USHAS[7:0]							
0x056		USHAS[9:8]		USVAS[9:8]		USHMS[9:8]		USVMS[9:8]	
0x057	USMAC	MSK_Y[7:0]							
0x058		MSK_CB[7:0]							
0x059		MSK_MR[7:0]							
0x060	JOCON	NU		SELIN	ALPHA[4:0]				
0x061		NU					CHEN	CFD[1:0]	
0x062	JOCHf	NU		CH_CB					
0x063		NU		CH_CR					
0x064	JOPOS	JOYS[7:0]							
0x065		JOYE[7:0]							
0x066		JOXS[7:0]							
0x067		JOXE[7:0]							
0x068		JOXE[9:8]		JOXS[9:8]		JOYE[9:8]		JOYS[9:8]	
0x069	DOCH	NU		CH_CB					
0x06A		NU		CH_CR					
0x06B	DOBBC	BLN_Y[7:0]							
0x06C		BLN_CB[7:0]							
0x06D		BLN_CR[7:0]							
0x06E	DOBS	BLN_S0[7:0]							
0x06F		BLN_S1[7:0]							
0x070	DOB0C	NU					CHEN	CFD[1:0]	
0x071		BSSEL	BBCEN	BEN	ALPHA				
0x072	DOB10C	NU					CHEN	CFD[1:0]	
0x073		BSSEL	BBCEN	BEN	BSSEL				
0x074	DOB11C	NU					CHEN	CFD[1:0]	
0x075		BSSEL	BBCEN	BEN	BSSEL				
0x076	DOB12C	NU					CHEN	CFD[1:0]	
0x077		BSSEL	BBCEN	BEN	BSSEL				
0x078	DOB13C	NU					CHEN	CFD[1:0]	
0x079		BSSEL	BBCEN	BEN	BSSEL				
0x07A	DOPOSW0	DOXS[7:0]							
0x07B		NU						DOXS[9:8]	
0x07C		DOYS[7:0]							
0x07D		NU						DOYS[9:8]	
0x07E		DOXE[7:0]							
0x07F		NU						DOXE[9:8]	
0x080		DOYE[7:0]							
0x081		NU						DOYE[9:8]	
0x082	DOPOSW10	DOXS[7:0]							
0x083		NU						DOXS[9:8]	
0x084		DOYS[7:0]							
0x085		NU						DOYS[9:8]	
0x086		DOXE[7:0]							
0x087		NU						DOXE[9:8]	
0x088		DOYE[7:0]							
0x089		NU						DOYE[9:8]	
0x08A	DOPOSW11	DOXS[7:0]							
0x08B		NU						DOXS[9:8]	
0x08C		DOYS[7:0]							
0x08D		NU						DOYS[9:8]	
0x08E		DOXE[7:0]							
0x08F		NU						DOXE[9:8]	
0x090		DOYE[7:0]							
0x091		NU						DOYE[9:8]	
0x092	DOPOSW12	DOXS[7:0]							
0x093		NU						DOXS[9:8]	
0x094		DOYS[7:0]							
0x095		NU						DOYS[9:8]	
0x096		DOXE[7:0]							
0x097		NU						DOXE[9:8]	
0x098		DOYE[7:0]							
0x099		NU						DOYE[9:8]	
0x09A	DOPOSW13	DOXS[7:0]							

Address	Name	7	6	5	4	3	2	1	0
0x09B		NU						DOXS[9:8]	
0x09C		DOYS[7:0]							
0x09D		NU						DOYS[9:8]	
0x09E		DOXE[7:0]							
0x09F		NU						DOXE[9:8]	
0x0A0		DOYE[7:0]							
0x0A1		NU						DOYE[9:8]	
0x0B0	ENC_Q	ENC_Q[7:0]							
0x0B1	ENC_SIZE	ENC_VSIZE[7:0]							
0x0B2		NU						ENC_VSIZE[9:8]	
0x0B3		ENC_HSIZE[7:0]							
0x0B4		NU						ENC_HSIZE[9:8]	
0x0B5	DEC_DLY	DEC_DLY[7:0]							
0x0B6	JPCON	NU				TOES	ORES	SSMODE	CFF
0x0B7	BUF_SIZE	BUF_SIZE[7:0]							
0x0B8		BUF_SIZE[15:8]							
0x0B9		BUF_SIZE[23:16]							
0x0BA	SB_ADDR	SB_ADDR[7:0]							
0x0BB		SB_ADDR[15:8]							
0x0BC		SB_ADDR[23:16]							
0x0BD		SB_ADDR[31:24]							
0x0BE	SE_ADDR	SE_ADDR[7:0]							
0x0BF		SE_ADDR[15:8]							
0x0C0		SE_ADDR[23:16]							
0x0C1		SE_ADDR[31:24]							
0x0C2	STR_SIZE	STR_SIZE[7:0]							
0x0C3		STR_SIZE[15:8]							
0x0C4		STR_SIZE[23:16]							
0x0C5	ENC_BADDR	ENC_BADDR[7:0]							
0x0C6		ENC_BADDR[15:8]							
0x0C7		ENC_BADDR[23:16]							
0x0C8		ENC_BADDR[31:24]							
0x0C9	DEC_BADDR	DEC_BADDR[7:0]							
0x0CA		DEC_BADDR[15:8]							
0x0CB		DEC_BADDR[23:16]							
0x0CC		DEC_BADDR[31:24]							
0x0CD	DEC_SIZE	DEC_VSIZE[7:0]							
0x0CE		NU						DEC_VSIZE[9:8]	
0x0CF		DEC_HSIZE[7:0]							
0x0D0		NU						DEC_HSIZE[9:8]	
0x0D1	UPSB	NU					UPDBA	UPEBA	NU
0x0D8	CP_REG	SAT[8]	NU	BRIGHT					
0x0D9		SAT[7:0]							
0x0DA		CONTRAST[7:0]							
0x0DB		HUE_COS[7:0]							
0x0DC		HUE_SIN[7:0]							
0x0E0	VECON	NU	DISBST	CBSEL	CBEN	Y_DLY	OUTSEL		VTYPE
0x0E1	VEPH	PHASE[7:0]							
0x0E2	VESF	SUB_FQ[7:0]							
0x0E3		SUB_FQ[15:8]							
0x0E4		SUB_FQ[23:16]							
0x0E5		SUB_FQ[31:24]							
0x0E6	VECFSEL	NU					COFF	CFSEL	
0x0E7	VEDOFF	COF_C[7:0]							
0x0E8		COF_Y[7:0]							
0x120	SDCCON	NU		DEVSEL		CASL		APC	XBW
0x121	SDCTC	TRC				TRCD		TRP	
0x122		NU				TRAS			
0x123	SDCCON	NU				BUSY	WBEN	IM	
0x124	SDCREF	REFCYC[7:0]							
0x125		REFCYC[15:8]							
0x126	SDCWBT	WBTCYC[7:0]							
0x127		WBTCYC[15:8]							
0x130	SDA0	SDA_BA[7:0]							
0x131		SDA_BA[15:8]							
0x132		SDA_BA[23:16]							
0x133		NU	SDA_BA[29:24]						
0x134		SDA_VS[7:0]							
0x135		SDA_HS[7:0]							
0x136		SDA_OF[7:0]							
0x137		SDA_OF[10:8]			SDA_HS[10:8]			SDA_VS[9:8]	
0x138	SDA1	SDA_BA[7:0]							
0x139		SDA_BA[15:8]							
0x13A		SDA_BA[23:16]							
0x13B		NU	SDA_BA[29:24]						

Address	Name	7	6	5	4	3	2	1	0
0x13C		SDA_VS[7:0]							
0x13D		SDA_HS[7:0]							
0x13E		SDA_OF[7:0]							
0x13F		SDA_OF[10:8]			SDA_HS[10:8]			SDA_VS[9:8]	
0x140	SDA2	SDA_BA[7:0]							
0x141		SDA_BA[15:8]							
0x142		SDA_BA[23:16]							
0x143		NU		SDA_BA[29:24]					
0x144		SDA_VS[7:0]							
0x145		SDA_HS[7:0]							
0x146		SDA_OF[7:0]							
0x147		SDA_OF[10:8]			SDA_HS[10:8]			SDA_VS[9:8]	
0x148	SDA3	SDA_BA[7:0]							
0x149		SDA_BA[15:8]							
0x14A		SDA_BA[23:16]							
0x14B		NU		SDA_BA[29:24]					
0x14C		SDA_VS[7:0]							
0x14D		SDA_HS[7:0]							
0x14E		SDA_OF[7:0]							
0x14F		SDA_OF[10:8]			SDA_HS[10:8]			SDA_VS[9:8]	
0x150	SDA4	SDA_BA[7:0]							
0x151		SDA_BA[15:8]							
0x152		SDA_BA[23:16]							
0x153		NU		SDA_BA[29:24]					
0x154		SDA_VS[7:0]							
0x155		SDA_HS[7:0]							
0x156		SDA_OF[7:0]							
0x157		SDA_OF[10:8]			SDA_HS[10:8]			SDA_VS[9:8]	
0x158	SDA5	SDA_BA[7:0]							
0x159		SDA_BA[15:8]							
0x15A		SDA_BA[23:16]							
0x15B		NU		SDA_BA[29:24]					
0x15C		SDA_VS[7:0]							
0x15D		SDA_HS[7:0]							
0x15E		SDA_OF[7:0]							
0x15F		SDA_OF[10:8]			SDA_HS[10:8]			SDA_VS[9:8]	
0x160	SDA6	SDA_BA[7:0]							
0x161		SDA_BA[15:8]							
0x162		SDA_BA[23:16]							
0x163		NU		SDA_BA[29:24]					
0x164		SDA_VS[7:0]							
0x165		SDA_HS[7:0]							
0x166		SDA_OF[7:0]							
0x167		SDA_OF[10:8]			SDA_HS[10:8]			SDA_VS[9:8]	
0x168	SDA7	SDA_BA[7:0]							
0x169		SDA_BA[15:8]							
0x16A		SDA_BA[23:16]							
0x16B		NU		SDA_BA[29:24]					
0x16C		SDA_VS[7:0]							
0x16D		SDA_HS[7:0]							
0x16E		SDA_OF[7:0]							
0x16F		SDA_OF[10:8]			SDA_HS[10:8]			SDA_VS[9:8]	
0x170	SDASEL	NU	WDSB1			NU	WDSB0		
0x171		NU	RDSB1			NU	RDSB0		
0x172		NU					RJOB		
0x173		NU	WJOB1			NU	WJOB0		
0x174		NU	RUSB1			NU	RUSB0		
0x175		NU					DOB0		
0x176		NU	DOB11			NU	DOB10		
0x177		NU	DOB13			NU	DOB12		
0x178		NU	JPB1			NU	JPB0		
0x179		NU	WDB			NU	RDB		
0x17A	DISPTI	NU	DPTI						
0x17B	DMACON	NU					XBRST	DBSEN	DSTT
0x17C	XBUFIE	DREIE	DWEIE	DDIE	DSIE	XREIE	XWEIE	XDIE	XSIE
0x17D	XBUFI	DREI	DWEI	DDI	DSI	XREI	XWEI	XDI	XSI
0x180	NFCIE	NU	ECCEIE	RBnIE	SOVIE	NAOIE	NCDIE	SEIE	BDAIE
0x181	NFCI	NU	ECCEI	RBnI	SOVI	NAOI	NCDI	SEI	BDAI
0x182	NFCADDR	NFCADDR[7:0]							
0x183		NFCADDR[15:8]							
0x184		NU	NFCADDR[22:16]						
0x185	ECCS	ECCST3[1:0]		ECCST2[1:0]		ECCST1[1:0]		ECCST0[1:0]	
0x186		ECCST7[1:0]		ECCST6[1:0]		ECCST5[1:0]		ECCST4[1:0]	
0x187	ECCSEG	NU					ECCSEG[2:0]		
0x188	ECCPTR	ECCPRT[7:0]							

Address	Name	7	6	5	4	3	2	1	0
0x189		NU				ECCPTR[11:8]			
0x190	ECCTT	NU					NFCTT[2:0]		
0x191	NFCPA	NFCPA[7:0]							
0x192		NFCPA[15:8]							
0x193		NU			NFCPA[20:16]				
0x194	NFCSA	NFCSA[7:0]							
0x195		NFCSA[15:8]							
0x196		NU							NFCSA[16]
0x197	NFCTS	NFCTS[7:0]							
0x198		NFCTS[15:8]							
0x199		NU			NFCTS[20:16]				
0x19A	NFCGO	NFCGO[7:0]							
0x19B	NFCSPR	NU							NFCSPR
0x1A0	NFCRST	NU							NFCRST
0x1A1	NFCDAC	NU			NFDA	NU		NFCS	
0x1A2	NFCR	NFCR							
0x1A3	NFAR	NFAR							
0x1A4	NFWD	NFWD							
0x1A5	NFRD	NFRD							
0x1A6	NFRDB	NU							NFRDB
0x1A7	NFSIZE	NU		NFPS		NU		NFAS	
0x1A8		NU		NFBS		NU	NFMS		
0x1A9	NFTIM	NU	NFST			NU	NFWT		
0x1AA		NU					NFHT		
0x1AB		NU	NFTIT			NU		NFRST	
0x1AC	NFCECC	NU		ECCSTOP	ECCDIS	ECCPOS			
0x1AD	NFCNMODE	NU						NB_ST	N_MODE
0x1B0	SMCCON	CTS	BSEN	REST		WRSEL	DTEN	DSRST	CSRST
0x1B1	SMCTC	NU			SCTS	TWR			
0x1B2	SMCDS	BLK_NUM[7:0]							
0x1B3		BLK_LNG[7:0]							
0x1B4		BLK_NUM[11:8]				BLK_LNG[11:8]			
0x1B5	SMCCMD	COMMAND[15:8]							
0x1B6		COMMAND[23:16]							
0x1B7		COMMAND[31:24]							
0x1B8		COMMAND[39:32]							
0x1B9		COMMAND[47:40]							
0x1BA	SMCCST	NU				CRCST			
0x1BB	SMCRES	RESPONSE[135:128]							
0x1BC		RESPONSE[127:120]							
0x1BD		RESPONSE[119:112]							
0x1BE		RESPONSE[111:104]							
0x1BF		RESPONSE[103:96]							
0x1C0		RESPONSE[95:88]							
0x1C1		RESPONSE[87:80]							
0x1C2		RESPONSE[79:72]							
0x1C3		RESPONSE[71:64]							
0x1C4		RESPONSE[63:56]							
0x1C5		RESPONSE[55:48]							
0x1C6		RESPONSE[47:40]							
0x1C7		RESPONSE[39:32]							
0x1C8		RESPONSE[31:24]							
0x1C9		RESPONSE[23:16]							
0x1CA		RESPONSE[15:8]							
0x1CB		RESPONSE[7:0]							
0x1CD	SMCTRCNT	BLK_CNT[7:0]							
0x1CE		DAT_CNT[7:0]							
0x1CF		BLK_CNT[11:8]				DAT_CNT[11:8]			
0x1D0	SMCIE	NU	CTSIE	CSTIE	DCIE	CCIE	DDIE	RDIE	CDIE
0x1D1	SMCI	NU	CTSI	CSTI	DCI	CCI	DDI	RDI	CDI
0x1E0	SPICON	NU					DORD	CPHA	CPOL
0x1E1	SPITD	TxDATA[7:0]							
0x1E2	SPII	NU		RDI	TDI	NU		RDIE	TDIE
0x1E3	SPIRD	RxDATA[7:0]							
0x1E8	I2CSADDR	NU	SADDR						
0x1E9	I2CTD	TxDATA[7:0]							
0x1EA	I2CI	NU	TDI	RDI	ACKI	NU	TDIE	RDIE	ACKIE
0x1EB	I2CRD	RxDATA[7:0]							
0x1EC	I2CDCNT	DAT_CNT[7:0]							
0x1F0	GPIODATA	GPIO_DT[7:0]							
0x1F1		GPIO_DT[15:8]							
0x1F2	GPIODIR	GPIO_DIR[7:0]							
0x1F3		GPIO_DIR[15:8]							
0x1F4	GPIOSEL	NU							GPIOSEL