深圳市拓普微科技开发有限公司
SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

LMT028DHHFWL-NEA

LCD Module User Manual

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Date: 2019-05-09	Date:	Date:

Rev.	Descriptions	Release Date
0.1	Preliminary new release	2019-05-09

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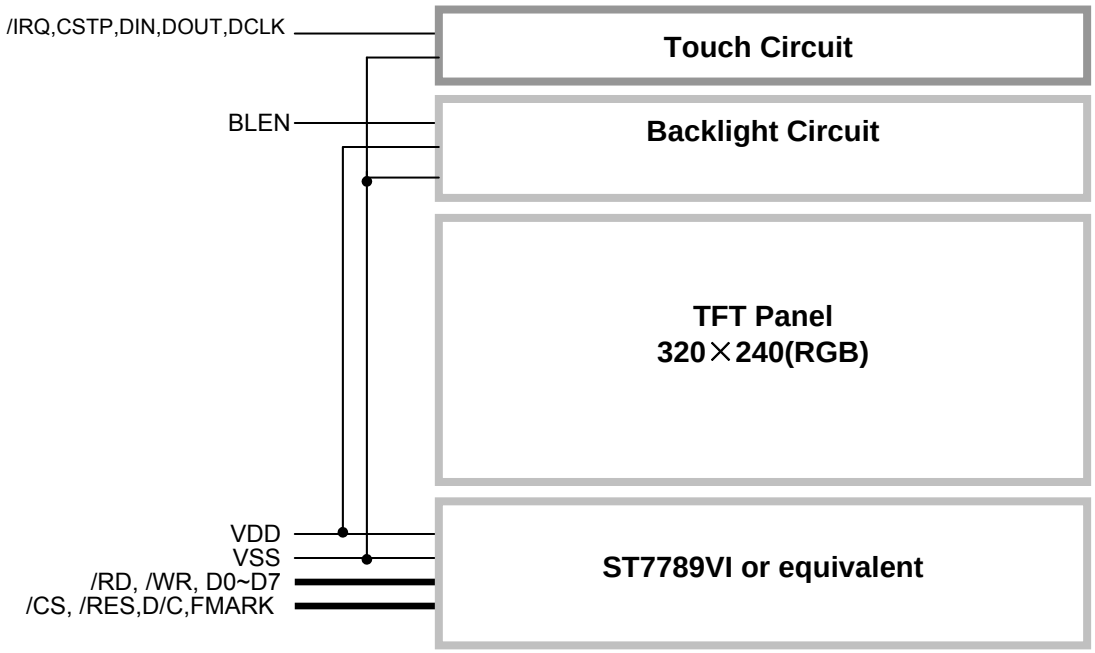
1. Basic Specifications

Screen Size(Diagonal) :	2.8”
Color Depth:	65k colors
Number of dots :	320 x 240(RGB)
Active Area :	57.6x43.2 mm
Dot Pitch :	0.18x0.18 mm
Display Technology :	a-Si TFT active matrix
Display Mode :	Transmissive / Positive
Pixel Configuration :	RGB Stripe
Viewing Direction :	3H (*1) (gray scale inverse) 9H (*2)
Polarizer Surface Treatment:	Glare
Backlight Type:	LEDs
Outline Dimension :	79.3 x 49.1 x 8.0(Max) mm (see dwg for details)
Operating Temperature :	-20 ~ +70°C
Storage Temperature :	-30 ~ +80°C

Note:
*1. For saturated color display content (eg. pure-red, pure-green, pure-blue, or pure-colors-combinations).
*2. For “color scales” display content.
*3. Color tone may slightly change by Temperature and Driving Condition.

1.1 Block Diagram



1.2 Terminal Functions

Pin No. (K1)	Pin Name	I/O	Descriptions
1	VSS	P	Negative power supply,0V
2	VSS		
3	BLEN	I	Backlight control Program dimming levels by driving pin with digital pulses.
4	VDD	P	Positive power supply
5	VDD		
6	/RD	I	Read enable input, active low
7	/WR	I	Write enable input, active low
8	D/C	I	Register Select D/C=H, Transferring the Display Data D/C = L, Transferring the Control Data
9	/CS	I	Chip Select /CS=L, enable access to the LCD module /CS=H, disable access to the LCD module
10	D0	I/O	Data Input
:	:	:	:
17	D7	I/O	Data Input
18	/RES	I	Reset signal /RES = L, Initialization is executed /RES = H, Normal running.
19	FMARK	O	Displaying Timing Frame Signal
20	NC	-	No Connection
21	VSS	P	Negative power supply,0V
22	/IRQ	O	Pen Interrupt. Open anode output (requires 10kΩ to 100kΩ pull-up resistor externally).
23	CSTP	O	Chip Select Input. Controls conversion timing and enables the serial input/output register.
24	DIN	I	Serial Data Input. If CS is LOW, data is latched on rising edge of DCLK.
25	DOUT	O	Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when CS is HIGH.
26	DCLK	O	External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O.

Pin No. (K2)	Pin Name	I/O	Descriptions
1	VSS	P	Negative power supply,0V
2	/IRQ	O	Pen Interrupt. Open anode output (requires 10kΩ to 100kΩ pull-up resistor externally).
3	CSTP	O	Chip Select Input. Controls conversion timing and enables the serial input/output register.
4	DIN	I	Serial Data Input. If CS is LOW, data is latched on rising edge of DCLK.
5	DOUT	O	Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when CS is HIGH.
6	DCLK	O	External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O.
7	VSS	P	Negative power supply,0V
8	VSS		
9	BLEN	I	Backlight control Program dimming levels by driving pin with digital pulses.
10	VDD	P	Positive power supply
11	VDD		
12	/RD	I	Read enable input, active low
13	/WR	I	Write enable input, active low
14	D/C	I	Register Select D/C=H, Transferring the Display Data D/C = L, Transferring the Control Data
15	/CS	I	Chip Select /CS=L, enable access to the LCD module /CS=H, disable access to the LCD module
16	D0	I/O	Data Input
:	:	:	:
23	D7	I/O	Data Input
24	/RES	I	Reset signal /RES = L, Initialization is executed /RES = H, Normal running.
25	FMARK	O	Displaying Timing Frame Signal
26	NC	-	No Connection

2. Absolute Maximum Ratings

VDD =5V, VSS=0V, T_{OP}=25°C

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	VDD	-0.3	+5.5	V	VSS= 0V
Input Voltage	V_{IN}	-0.3	+4.6	V	VSS = 0V
Operating Temperature	T_{OP}	-20	+70	°C	No Condensation
Storage Temperature	T_{ST}	-30	+80	°C	No Condensation

Cautions:
Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

3. Electrical Characteristics

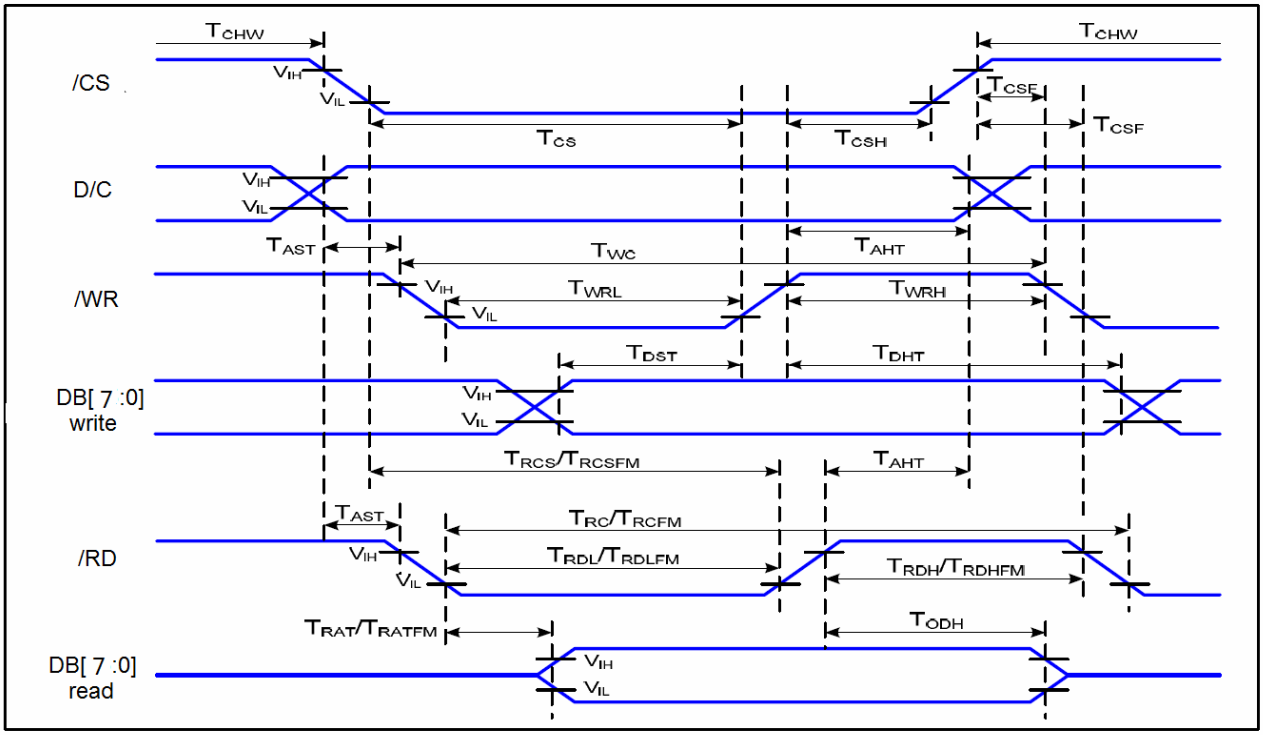
3.1 DC Characteristics

VDD=5V, VSS=0V, T_{OP}=25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition / Application Pin
Operating Voltage	VDD	4.8	5.0	5.2	V	VDD
	IOVDD	2.7	3.0	3.6	V	IOVDD
Input High Voltage	V_{IH}	0.7* IOVDD	-	IOVDD	V	/RES,D0~D7,/CS,/RD,/WR,BLEN,D/C, /IRQ,CSTP,DIN,DOUT,DCLK
Input Low Voltage	V_{IL}	0	-	0.3* IOVDD	V	
Output High Voltage	V_{OH}	0.7* IOVDD	-	IOVDD	V	D0~D7, /IRQ,CSTP,DIN,DOUT, DCLK
Output Low Voltage	V_{OL}	0	-	0.3* IOVDD	V	D0~D7
		0	-	0.4* IOVDD	V	/IRQ,CSTP,DIN,DOUT, DCLK
Operating Current	I_{DD}	-	74.5	86	mA	Backlight are ON
	I_{DD}	-	6.25	16	mA	Backlight are OFF

3.2 AC Characteristics

8080 Mode System Bus Timing



VDD =5V, VSS=0V, T_{OP}=25°C

Signal	Symbol	Parameter	Spec.		Unit	Description
			Min.	Max.		
D/C	T_{AST}	Address setup time	5	-	ns	-
	T_{AHT}	Address hole time(Write/Read)	13	-		
/CS	T_{CHW}	Chip select “H” pulse width	5	-	ns	-
	T_{CS}	Chip select setup time(Write)	20	-		
	T_{RCS}	Chip select setup time(Read ID)	60	-		
	T_{RCSFM}	Chip select setup time(Read FM)	460			
	T_{CSF}	Chip select wait time(Write/Read)	13			
	T_{CSH}	Chip select hold time	13			
/WR	T_{WC}	Write cycle	86	-	ns	-
	T_{WRH}	Control pulse “H” duration	20	-		
	T_{WRL}	Control pulse “L” duration	20	-		
DB[7:0]	T_{DST}	Data setup time	13	-	ns	For maximum CL=30pF For minimum CL=8pF
	T_{DHT}	Data hold time	13	-		
	T_{RAT}	Read access time(ID)	-	52		
	T_{RATFM}	Read access time(FM)	-	442		
	T_{ODH}	Ouput disable time	14	104		
/RD(ID)	T_{RC}	Read cycle(ID)	208		ns	When read ID data
	T_{RDH}	Control pulse “H” duration(ID)	120			
	T_{RDL}	Control pulse “H” duration(ID)	60			
/RD(FM)	T_{RCFM}	Read cycle(FM)	585			When read from frame memory
	T_{RDHFM}	Control pulse “H” duration(FM)	120			
	T_{RDLFM}	Control pulse “H” duration(FM)	460			

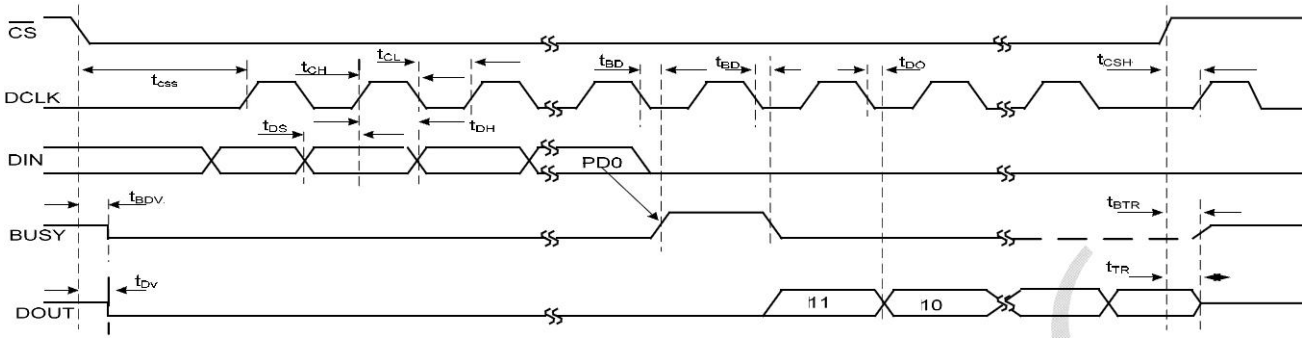
Note:
*1. Input signal rise/fall time should be less than 15ns .
*2. All timing is using 20% and 80% of VDD as the reference.
*3. Please refer to ST7789VI datasheet for details

3.3 Touch Panel controller Timing Characteristics

VDD=5V, VSS=0V, T_{OP}=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
Acquisition time(*1)	t_{ACQ}	1.5	-	-	us
DIN Valid Prior to DCLK Rising	t_{DS}	100	-	-	ns
DIN Hold After DCLK HIGH	t_{DH}	50	-	-	ns
DCLK Falling to DOUT Valid	t_{DO}	-	-	200	ns
CSTP Falling to DOUT Enabled	t_{DV}	-	-	200	ns
CSTP Rising to DOUT Disabled	t_{TR}	-	-	200	ns
CSTP Falling to First DCLK Rising	t_{CSS}	100	-	-	ns
CSTP Rising to DCLK Ignored	t_{CSH}	10	-	-	ns
DCLK high pulse width	t_{CH}	200	-	-	ns
DCLK low pulse width	t_{CL}	200	-	-	ns
DCLK Falling to BUSY Rising	t_{BD}	-	-	200	ns
CSTP Falling to BUSY Enabled	t_{BDV}	-	-	200	ns
CSTP Rising to BUSY Disabled	t_{BTR}	-	-	200	ns

NOTE:
*1 See Serial Data Sequence Diagram.
*2 The BUSY signal is not connected to Terminal (K3,K4),after one control byte send via DIN, some delay is needed to read the conversation result through DOUT.
*3 Please see the XPT2046 datasheet for details.



Timing diagram

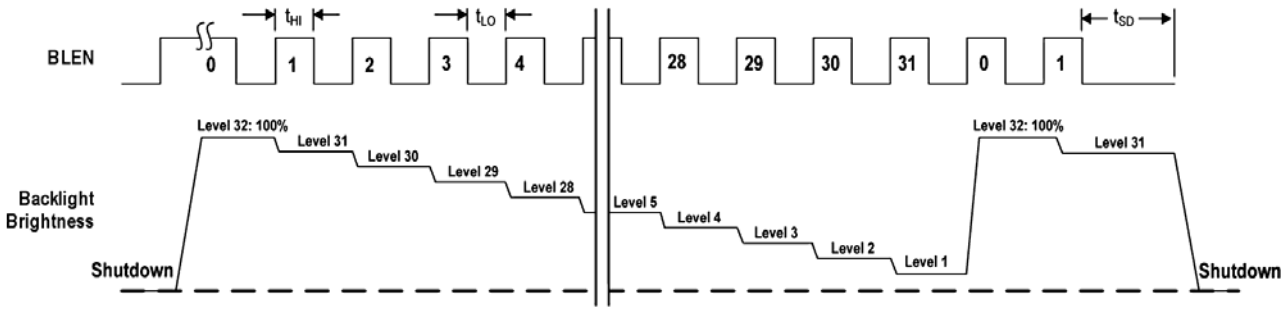
3.4 Backlight control Timing

VDD=5V, VSS=0V, T_{OP} =25°C

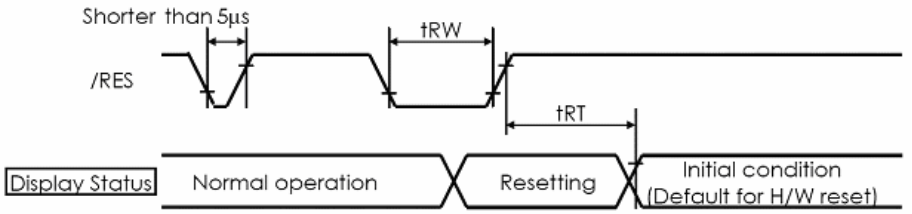
Signal	Symbol	Parameter	Spec.			Unit	Description
			Min.	Typ	Max.		
BLEN	t_{HI}	Time Delay between Steps	2	-	-	us	H: 3.3V
	t_{LO}	CTRL LOW Time for Dimming	1	-	250	us	L: 0V
	t_{SD}	CTRL LOW ,shutdown Pulse Whidth	2	-	-	ms	

Note: For basic ON/OFF function, please beware of minimum pulse width.

Register BLEN timing



3.5 Reset Timing



VDD =5V, VSS=0V, T_{OP}=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
Reset LOW pulse width	t_{RW}	10	-	-	us
Reset time	T_{RT}	-	-	170	ms

4. Functions

4.1 Display Commands

Instruction	D/C	/WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NOP	0	↑	-	0	0	0	0	0	0	0	0	(00h)	No operation
SWRESET	0	↑	-	0	0	0	0	0	0	0	1	(01h)	Software reset
RDDID	0	↑	-	0	0	0	0	0	1	0	0	(04h)	Read display ID
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 read
	1	1	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 read
	1	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		ID3 read
RDDST	0	↑	-	0	0	0	0	1	0	0	1	(09h)	Read display status
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24		-
	1	1	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON		-
	1	1	-	ST15	ST14	INVON	ST12	ST11	DISON	TEON	GCS2		-
	1	1	-	GCS1	GCS0	TEM	ST4	ST3	ST2	ST1	ST0		-
RDDPM	0	↑	-	0	0	0	0	1	0	1	0	(0Ah)	Read display power
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	0	0		
RDD MADCTL	0	↑	-	0	0	0	0	1	0	1	1	(0Bh)	Read display
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	MY	MX	MV	ML	RGB	MH	0	0		-
RDD COLMOD	0	↑	-	0	0	0	0	1	1	0	0	(0Ch)	Read display pixel
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	0	D6	D5	D4	0	D2	D1	D0		-
RDDIM	0	↑	-	0	0	0	0	1	1	0	1	(0Dh)	Read display image
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	VSSON	0	INVON	0	0	GC2	GC1	GC0		-
RDDSM	0	↑	-	0	0	0	0	1	1	1	0	(0Eh)	Read display signal
	1	1	-	-	-	-	-	-	-	-	-		Dummy read

Instruction	D/C	/WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	1	-	TEON	TEM	0	0	0	0	0	0		-
RDDSDR	0	↑	-	0	0	0	0	1	1	1	1	(0Fh)	Read display self-diagnostic result
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	D7	D6	0	0	0	0	0	0		-
SLPIN	0	↑	-	0	0	0	1	0	0	0	0	(10h)	Sleep in
SLPOUT	0	↑	-	0	0	0	1	0	0	0	1	(11h)	Sleep out
PTLON	0	↑	-	0	0	0	1	0	0	1	0	(12h)	Partial mode on
NORON	0	↑	-	0	0	0	1	0	0	1	1	(13h)	Partial off (Normal)
INVOFF	0	↑	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off
INVON	0	↑	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
GAMSET	0	↑	-	0	0	1	0	0	0	0	1	(26h)	Display inversion on
	1	↑	-	0	0	0	0	GC3	GC2	GC1	GC0		
DISPOFF	0	↑	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	0	↑	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET	0	↑	-	0	0	1	0	1	0	1	0	(2Ah)	Column address set
	1	↑	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X address start: 0≦XS≦X
	1	↑		XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
	1	↑		XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X address start: S≦XE≦X
	1	↑		XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
RASET	0	↑	-	0	0	1	0	1	0	1	1	(2Bh)	Row address set
	1	↑	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y address start: 0≦YS≦Y
	1	↑		YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
	1	↑		YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y address start: S≦YE≦Y
	1	↑		YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
RAMWR	0	↑	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
	1	↑	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	↑	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
RAMRD	0	↑	-	0	0	1	0	1	1	1	0	(2Eh)	Memory read

Instruction	D/C	/WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Read data
	1	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
PTLAR	0	↑	-	0	0	1	1	0	0	0	0	(30h)	Partial sart/end address set
	1	↑	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8		Partial start address: (0, 1,2, ..P)
	1	↑	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		
	1	↑	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		Partial end address (0, 1,2, 3, , P)
	1	↑	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		
VSCRDEF	0	↑	-	0	0	1	1	0	0	1	1	(33h)	Vertical scrolling definition
	1	↑	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8		
	1	↑	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0		
	1	↑	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8		
	1	↑	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		
	1	↑	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8		
	1	↑	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0		
TEOFF	0	↑	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	0	↑	-	0	0	1	1	0	1	0	1	(35h)	Tearing effect line on
	1	↑	-	-	-	-	-	-	-	-	TEM		
MADCTL	0	↑	-	0	0	1	1	0	1	1	0	(36h)	Memory data access control
	1	↑	-	MY	MX	MV	ML	RGB	0	0	0		-
VSCRSADD	0	↑	-	0	0	1	1	0	1	1	1	(37h)	Vertical scrolling start address
	1	↑	-	VSP15	VSP14	VSP13	VSP12	VSP11	VSP10	VSP9	VSP8		
	1	↑	-	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0		
IDMOFF	0	↑	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off
IDMON	0	↑	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on
COLMOD	0	↑	-	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format

Instruction	D/C	/WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	↑	-	0	D6	D5	D4	0	D2	D1	D0		Interface format
RAMWRC	0	↑	-	0	0	1	1	1	1	0	0	(3Ch)	Memory write continue
	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
	1	↑	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	↑	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
RAMRDC	0	↑	-	0	0	1	1	1	1	1	0	(3Eh)	Memory read continue
	1	1	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		
	1	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
TESCAN	0	↑	-	0	1	0	0	0	1	0	0	(44h)	Set tear scanline
	1	↑	-	N15	N14	N13	N12	N11	N10	N9	N8		
	1	↑	-	N7	N6	N5	N4	N3	N2	N1	N0		
RDTESCAN	0	↑	-	0	1	0	0	0	1	0	1	(45h)	Get scanline
	1	1	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	-	-	-	-	-	-	-	N9	N8		
	1	1	-	N7	N6	N5	N4	N3	N2	N1	N0		
WRDISBV	0	↑	-	0	1	0	1	0	0	0	1	(51h)	Write display brightness
	1	↑	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		
RDDISBV	0	↑	-	0	1	0	1	0	0	1	0	(52h)	Read display brightness value
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		
WRCTRLD	0	↑	-	0	1	0	1	0	0	1	1	(53h)	Write CTRL display
	1	↑	-	0	0	BCTRL	0	DD	BL	0	0		
RDCTRLD	0	↑	-	0	1	0	1	0	1	0	0	(54h)	Read CTRL value dsiplay
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	0	0	BCTRL	0	DD	BL	0	0		

Instruction	D/C	/WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
WRCACE	0	↑	-	0	1	0	1	0	1	0	1	(55h)	Write content adaptive brightness control and Color enhancemnet
	1	↑	-	CECTRL	0	CE1	CE0	0	0	C1	C0		
RDCABC	0	↑	-	0	1	0	1	0	1	1	0	(56h)	Read content adaptive brightness control
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	0	CECTRL	0	0	0	0	C1	C0		
WRCABCMB	0	↑	-	0	1	0	1	1	1	1	0	(5Eh)	Write CABC minimum brightness
	1	↑	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0		
RDCABCMB	0	↑	-	0	1	0	1	1	1	1	1	(5Fh)	Read CABC minimum brightness
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0		
RDID1	0	↑	-	1	1	0	1	1	0	1	0	(Dah)	Read ID1
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read parameter
RDID2	0	↑	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read parameter
RDID3	0	↑	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1		ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read parameter

Notes:
1. There will be no abnormal visible effects on the display when S/W or H/W Reset are applied.
2. Please refer to ST7789VI datasheet for details

4.2 Power off the LCD Module

It recommends that enter Sleep Mode before power off the LCD module.

4.3 Refreshing The LCD Module

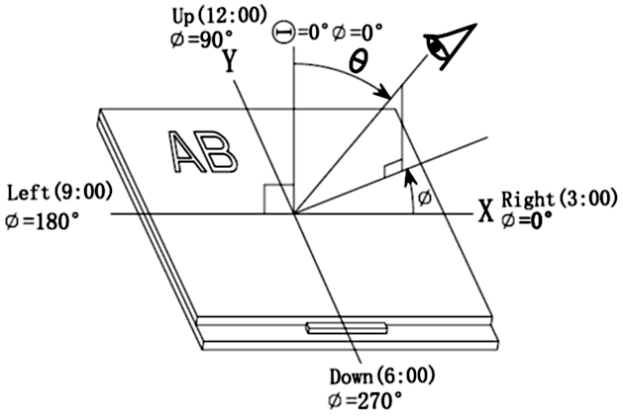
It recommends that the operating modes and display contents be refreshed periodically to prevent the effect of unexpected noise.

5. Optical Characteristics

Item		Symbol	Condition	MIN.	TYP.	MAX.	UNIT	Note.
Viewing angle		Φ=90°	(CR≥10)	50	60	-	degree	Note 1,6
		Φ=270°		50	60	-		
		Φ=180°		40	50	-		
		Φ=0°		50	60	-		
Contrast ratio		CR	Φ=0° θ=0°	300	500	-	-	Note 3
Response Time		T_{on}	Φ=0° θ=0°	-	30	50	msec	Note 4
		T_{off}					msec	
Chromaticlty	Red	X	Backlight is on Φ=0° θ=0°	0.55	0.60	0.65		Note 1,5
		Y		0.30	0.35	0.40		
	Green	X		0.27	0.32	0.37		
		Y		0.56	0.61	0.66		
	Blue	X		0.09	0.14	0.19		
		Y		0.05	0.09	0.15		
	White	X		0.26	0.29	0.32		
		Y		0.28	0.31	0.34		
NTSC Ratio	S			45	65	-	%	
Luminance		L	Φ=0° θ=0°	160	200	-	cd/m^2	Note 1,6
Luminance uniformity		U		80	-	-	%	Note 1,6

Note 1:
The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment PR-705
Measuring condition:
- Measuring surroundings: Dark room
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.

Note 2:
The definition of viewing angle:
Refer to the graph below marked by θ and Φ

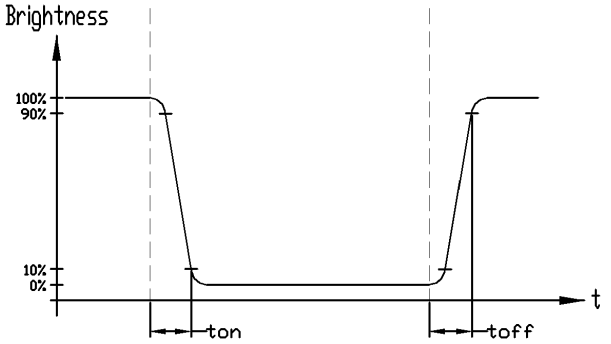


Note 3:
The definition of contrast ratio (Test LCM using PR-705):

$$\text{Contrast Ratio(CR)} = \frac{\text{Luminance When LCD is at "White" state}}{\text{Luminance When LCD is at "Black" state}}$$

(Contrast Ratio is measured in optimum common electrode voltage)

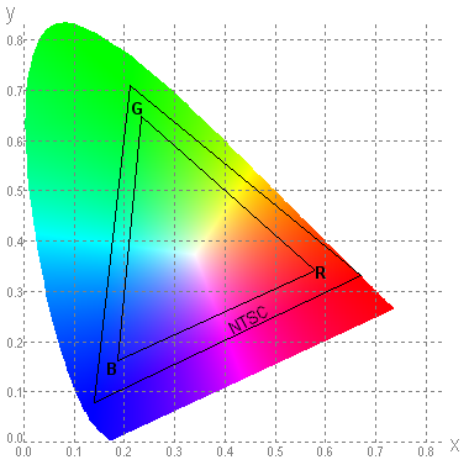
Note 4:
Definition of Response time. (Test LCD using DMS501):
The output signals of photo detector are measured when the input signals are changed from "black" to "white"(falling time) and from "white" to "black"(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.Refer to figure as below.



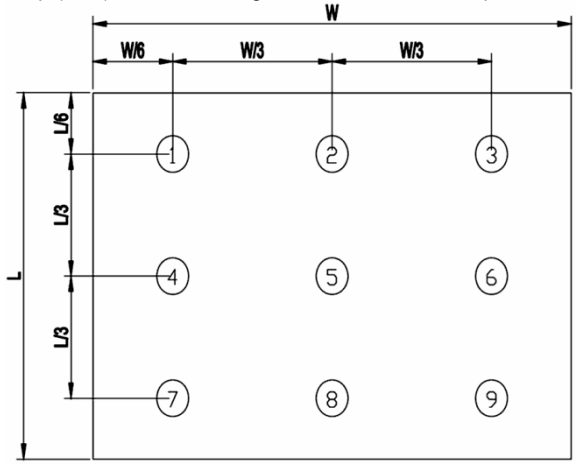
Note 5:
Definition of Color of CIE1931 Coordinate and NTSC Ratio.

Color gamut:

$$S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$



Note 6:
The luminance uniformity is calculated by using following formula.
△Bp = Bp (Min.) / Bp (Max.)×100 (%)
Bp (Max.) = Maximum brightness in 9 measured spots
Bp (Min.) = Minimum brightness in 9 measured spots.



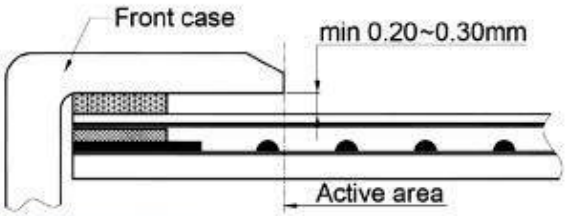
Note 7:
Measured the luminance of white state at center point

6. Design and Handling Precaution

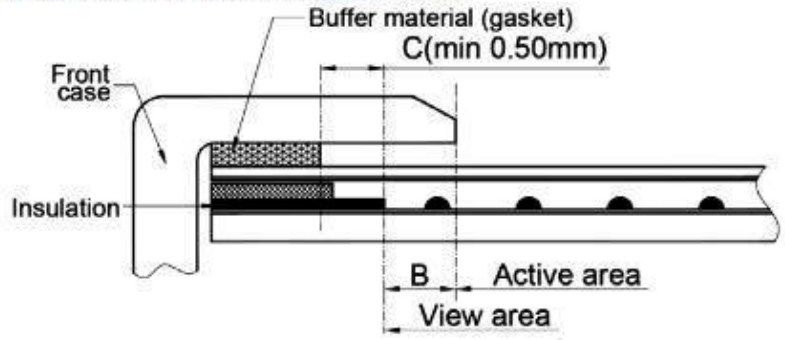
1. The LCD panel is made by glass. Any mechanical shock (eg. dropping form high place) will damage the LCD module.
2. Do not add excessive force on the surface of the display, which may cause the Display color change abnormally.
3. The polarizer on the LCD is easily get scratched. If possible, do not remove the LCD protective film until the last step of installation.
4. Never attempt to disassemble or rework the LCD module.
5. Only Clean the LCD with Isopropyl Alcohol or Ethyl Alcohol. Other solvents (eg. water) may damage the LCD.
6. When mounting the LCD module, make sure that it is free form twisting, warping and distortion.
7. Ensure to provide enough space (with cushion) between case and LCD panel to prevent external force adding on it, or it may cause damage to the LCD or degrade the display result.
8. Only hold the LCD module by its side. Never hold LCD module by add force on the heat seal or TAB.
9. Never add force to component of the LCD module. It may cause invisible damage or degrade of the reliability.
10. LCD module could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect the LCD module.
11. When peeling off the protective film from LCD, static charge may cause abnormal display pattern. It is normal and will resume to normal in a short while.
12. Take care and prevent get hurt by the LCD panel sharp edge.
13. Never operate the LCD module exceed the absolute maximum ratings.
14. Keep the signal line as short as possible to prevent noisy signal applying to LCD module.
15. Never apply signal to the LCD module without power supply.
16. IC chip (eg. TAB or COG) is sensitive to the light. Strong lighting environment could possibly cause malfunction. Light sealing structure casing is recommend.
17. LCD module reliability may be reduced by temperature shock.
18. When storing the LCD module, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature. They may damage or degrade the LCD module

7. Touch panel Design Precautions

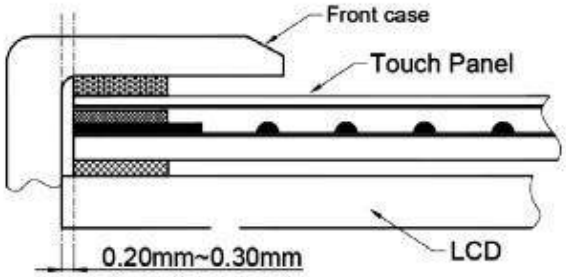
1. It should prevent front case touching the touch panel Active Area (A.A.) to prevent abnormal touch.
   It should left gab (e.g. 0.2~0.3mm) in between.



2. Outer case design should take care about the area outside the A.A.
   Those areas contain circuit wires which is having different thickness. Touching those areas could de-form the ITO film. As a result case the ITO cold be damaged and shorten its lifetime.
   It is suggested to protect those areas with gasket (between the front case and the touch panel).
   The suggested figures are B≥0.50mm; C≥0.50mm。



3. The front case side wall should keep space (e.g. 0.2 ~ 0.3mm) from the touch panel.



4. In general design,
   touch panel V.A. should be bigger than the LCD V.A.
   and touch panel A.A. should be bigger than the LCD A.A.