深圳市拓普微科技开发有限公司
SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

LMT032DNHFWD-NAN

LCD Module User Manual

Prepared by:	Checked by:	Approved by:
Lin		
Date: 2012-10-15	Date:	Date:

Rev.	Descriptions	Release Date
0.1	Preliminary	2012-10-15

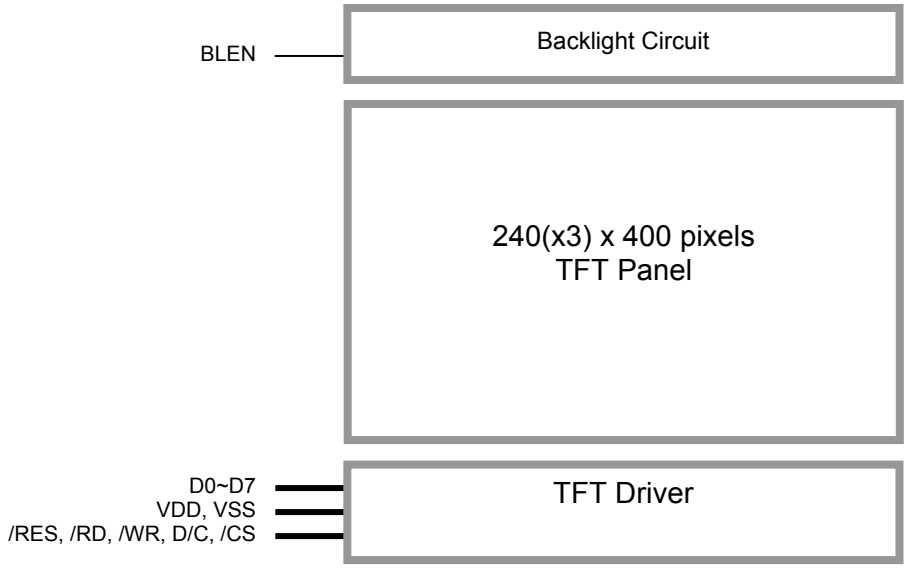
Table of Content

1. General Specification

Screen Size(Diagonal) :	3.2 inch
Resolution :	240(RGB) x 400
Signal Interface :	8-bit MCU Interface
Color Depth :	65k color
Pixel Pitch :	0.174 x 0.174 (mm)
Pixel Configuration :	RGB Stripe
Display Mode :	Transmissive / normal white
Surface Treatment :	Clare Type
Viewing Direction :	9 o'clock
Outline Dimension :	92.6 x 51.0 x 5.7 (mm) (exclude FPC, see attached drawing for details)
Active Area :	69.6 x 41.76 (mm)
Backlight :	4 LEDs
Operating Temperature :	-20 ~ +70°C
Storage Temperature :	-30 ~ +80°C

Note:
*1 Color tune may slightly changed by temperature and driving voltage.

2. Block Diagram



3. Terminal Functions

3.1 Interface

Pin No.	Pin Name	I/O	Descriptions
1	VSS	P	Power Ground (0V)
2	VSS		
3	BLEN	I	BLEN=L, backlight Off BLEN=H, backlight On
4	VDD	P	Positive Power Supply
5	VDD		
6	/RD	I	/WR=H, /RD=L; Data or Status read form the LCD module
7	/WR	I	/WR=L→H, RD=H; Data or Instruction latch into the LCD module
8	D/C	I	Register Select D/C = H, Transferring the Display Data D/C = L, Transferring the Control Data
9	/CS	I	Chip Select /CS=L, enable access to the LCD interface /CS=H, disable access to the LCD interface
10	D0	I	Data Input
:	:	:	:
17	D7	I	Data Input
18	/RES	I	Reset signal /RES = L, Initialization is executed /RES = H, Normal running.
19	NC	-	-
20	NC	-	-
21	NC	-	-
22	NC	-	-

4. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	V_{DD}	-0.3	+4.0	V	GND = 0V
Operating Temperature	T_{OP}	-20	+70	°C	No Condensation
Storage Temperature	T_{ST}	-30	+80	°C	No Condensation

Cautions:
Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

5. Electrical Characteristics

5.1 DC Characteristics (MCU terminal)

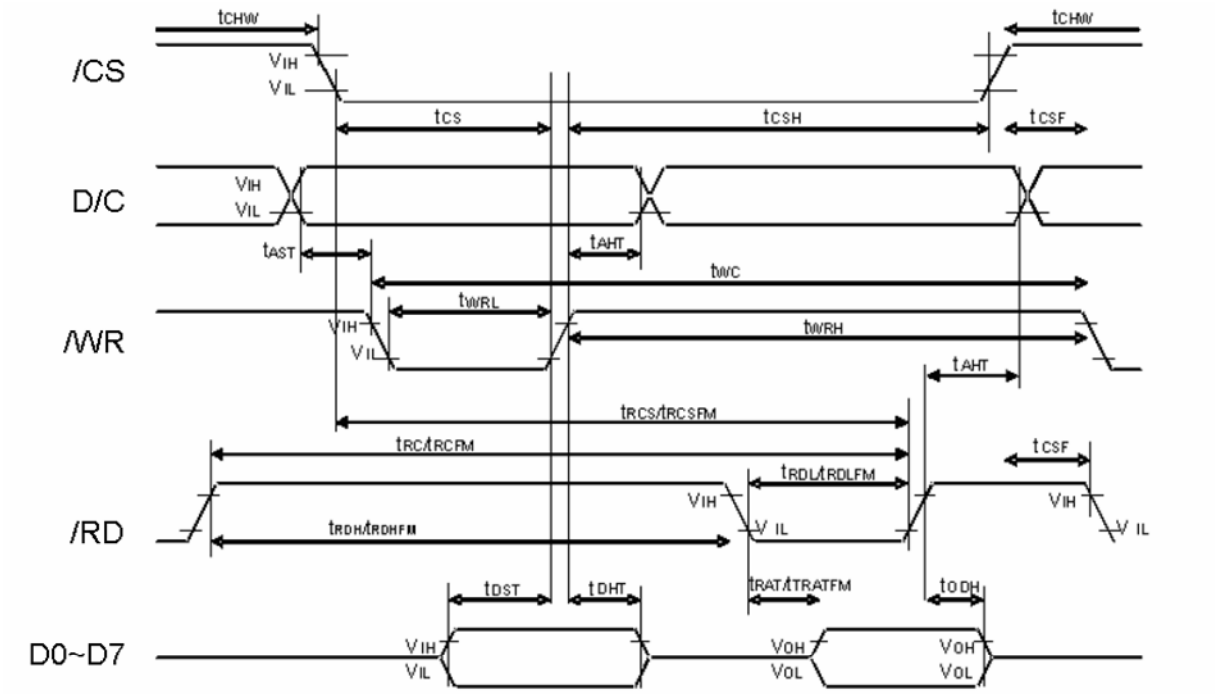
VSS=0V, T_{OP} =25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Operating Voltage	VDD	2.7	3.0	3.3	V	VDD
Input High Voltage	V_{IH}	0.8VDD	-	VDD	V	Input pins
Input Low Voltage	V_{IL}	VSS	-	0.2VDD	V	Input pins
Output Signal High Voltage	V_{OH}	0.7VDD	-	VDD	V	
Output Signal Low Voltage	V_{OL}	0	-	0.3xVDD	V	
Operating Current	I_{DD}	-	105	-	mA	All black, Backlight ON (BLEN=H)
		-	11	-	mA	All black, Backlight OFF (BLEN=L)

5.2 AC Characteristics

Signal	Symbol	Parameter	Spec.			Unit	Description
			Min.	Typ	Max.		
D/C	tAST	Address setup time	10	-	-	ns	
	tAHT	Address hole time(Write/Read)	10	-	-		
/CS	tCHW	Chip select “H” pulse width	0	-	-	ns	
	tCS	Chip select setup time(Write)	35	-	-		
	tRCSFM	Chip select setup time(Read FM)	355	-	-		
	tCSF	Chip select wait time(Write/Read)	10	-	-		
	tCSH	Chip select hold time	10	-	-		
/WR	tWC	Write cycle	33	-	-	ns	
	tWRH	Control pulse “H” duration	15	-	-		
	tWRL	Control pulse “L” duration	15	-	-		
/RD (FM)	tRCFM	Read cycle(FM)	450	-	-	ns	When read from frame memory
	tRDHFM	Control pulse “H” duration(FM)	90	-	-		
	tRDLFM	Control pulse “L” duration(FM)	355	-	-		
D[7:0]	tDST	Data setup time	15	-	-	ns	For maximum CL=30pF For minimum CL=8pF
	tDHT	Data hold time	10	-	-		
	tRATFM	Read access time(FM)	-	-	340		
	tODH	Output disable time	20	-	80		

Note:
*1. The input signal rise time and fall time(tr , tf)is specified at 15 ns or less
*2. Logic high and low levels are specified as 30% and 70% of VDD for input signals.
*3 .Refer to the HX8352-B datasheet for more details.

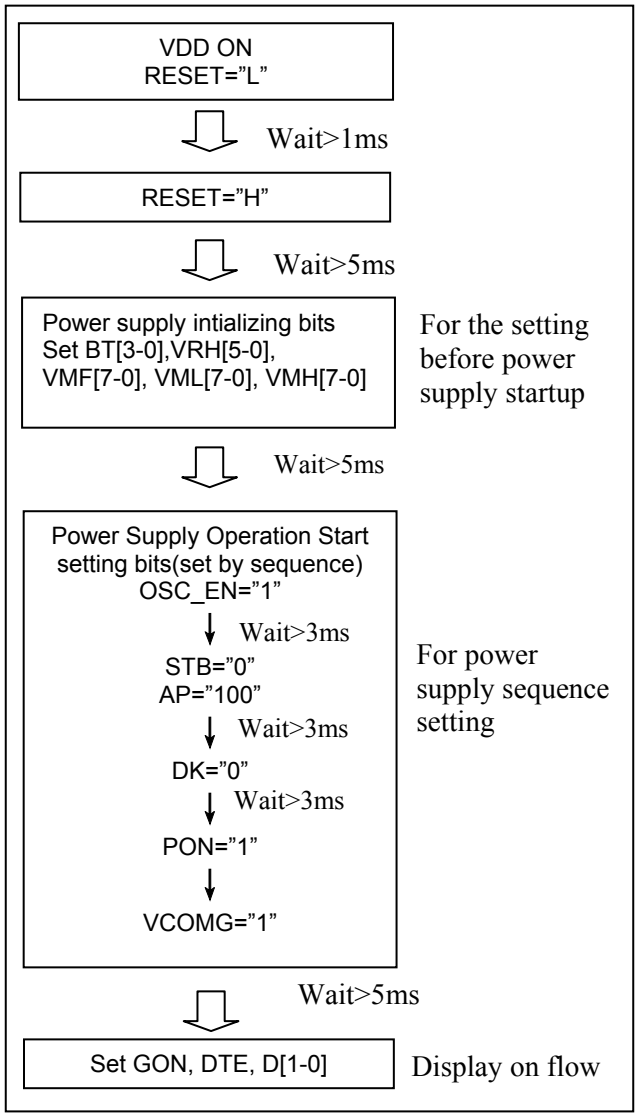


Register Write/Read timing (for CPU 8 Bit)

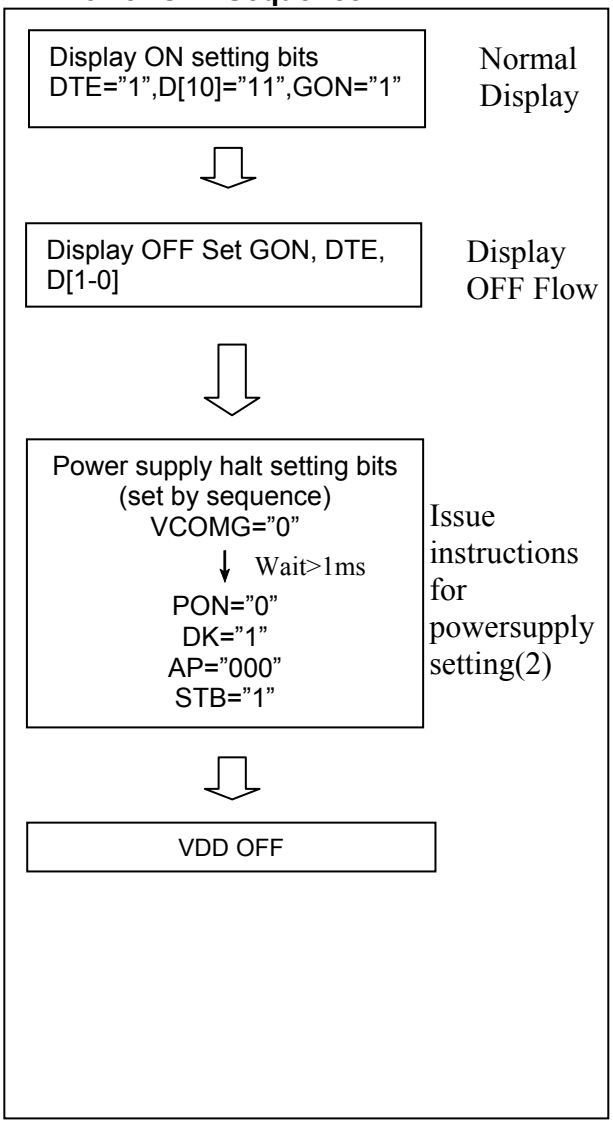
6. Function specifications

6.1 Power ON/OFF Sequence

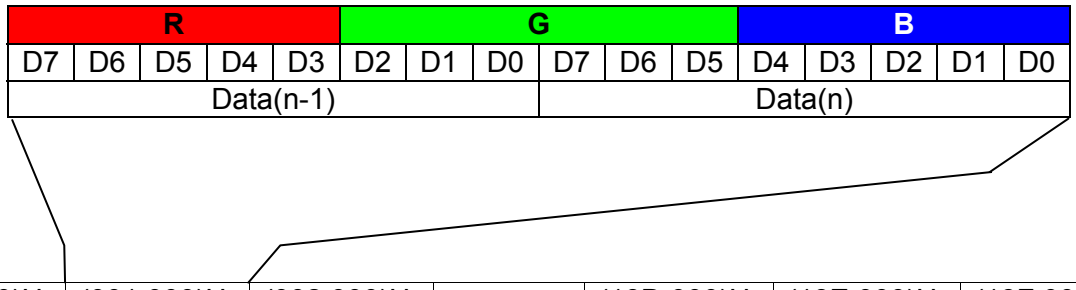
Power ON Sequence



Power OFF Sequence



6.2 Display Memory Map



(000,000)H	(001,000)H	(002,000)H	- - -	(18D,000)H	(18E,000)H	(18F,000)H
(000,001)H	(001,001)H	(002,001)H	- - -	(18D,001)H	(18E,001)H	(18F,001)H
(000,002)H	(001,002)H	(002,002)H	- - -	(18D,002)H	(18E,002)H	(18F,002)H
⋮	⋮	⋮	⋮	⋮	⋮	⋮
(000,0ED)H	(001,0ED)H	(002,0ED)H	- - -	(18D,0ED)H	(18E,0ED)H	(18F,0ED)H
(000,0EE)H	(001,0EE)H	(002,0EE)H	- - -	(18D,0EE)H	(18E,0EE)H	(18F,0EE)H
(000,0EF)H	(001,0EF)H	(002,0EF)H	- - -	(18D,0EF)H	(1AE,0EF)H	(18F,0EF)H

Note:
1. Based on the top view of the LCD module.
2. The above is memory map based on:
   MX=1
   MY=0
   MV=1
   BGR=1
   CSEL_DBI[2:0]=101

7. Commands

(Hex)	Operation Code	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
00	Himax ID	R	-	Himax ID (8'bXXXX_XXXX)								-
01	Display Mode control	W/R	-		DP_STBY (0)	-	-	SCROL(0)	IDMON(0)	INVON(0)	PTLON(0)	-
02	Column address start 2	W/R	-	SC[15:8] (8'b0)								-
03	Column address start 1	W/R	-	SC[7:0] (8'b0)								-
04	Column address end 2	W/R	-	EC[15:8] (8'b0)								-
05	Column address end 1	W/R	-	EC[7:0] (8'b1110_1111)								-
06	Row address start 2	W/R	-	SP[15:8] (8'b0)								-
07	Row address start 1	W/R	-	SP[7:0] (8'b0)								-
08	Row address end 2	W/R	-	EP[15:8] (8'b0000_0001)								-
09	Row address end 1	W/R	-	EP[7:0] (8'b1010_1111)								-
0A	Partial area start row 2	W/R	-	PSL[15:8] (8'b0)								-
0B	Partial area start row 1	W/R	-	PSL[7:0] (8'b0)								-
0C	Partial area end row 2	W/R	-	PEL[15:8] (8'b0000_0001)								-
0D	Partial area end row 1	W/R	-	PEL[7:0] (8'b1010_1111)								-
0E	Vertical Scroll Top fixed area 2	W/R	-	TFA[15:8](8'b0)								-
0F	Vertical Scroll Top fixed area 1	W/R	-	TFA[7:0](8'b0)								-
10	Vertical Scroll height area 2	W/R	-	VSA[15:8](8'b0000_0001)								-
11	Vertical Scroll height area 1	W/R	-	VSA[7:0](8'b1011_0000)								-
12	Vertical Scroll Button area 2	W/R	-	BFA[15:8](8'b0)								-
13	Vertical Scroll Button area 1	W/R	-	BFA[7:0](8'b0)								-
14	Vertical Scroll Start address 2	W/R	-	VSP[15:8](8'b0)								-
15	Vertical Scroll Start address 1	W/R	-	VSP[7:0](8'b0)								-
16	Memory Access control	W/R	-	MY (0)	MX (0)	MV (0)	-	BGR (0)	SM(0)	SS (0)	GS (0)	-
17	COLMOD	W/R	-	CSEL_RGB[2:0](110)				-	CSEL_DBI[2:0](110)			-
18	OSC Control 1	W/R	-	-	I/P RADJ[3:0](1000)			-	N/P RADJ[3:0](1000)			*
19	OSC Control 2	W/R	-	-	-	-	-	-	RNG_EN(0)	OSC_TURBO(0)	OSC_EN (0)	-
1A	Power Control	W/R	-	-	-	-	DCCLK_DISBALE (0)	BT[3:0] (0000)				-
1B	Power Control	W/R	-	-	-	VRH[5:0](01_1000)						-
1C	Power Control	W/R	-	-	-	-	-	-	AP[2:0] (100)			-
1D	Power Control	W/R	-	-	I/PI_FS0[2:0] (010)			-	N/P_FS0[2:0] (010)			-
1E	Power Control	W/R		-	I/PI_FS1[2:0] (001)			-	N/P_FS1[2:0] (001)			-
1F	Power Control 1	W/R	-	GASEN(1)	VCOMG (0)	VPNL_EN(0)	PON (0)	DK (1)	XDK (1)	DDVDH_TRI(0)	STB (1)	-

Commands(continue)

(Hex)	Operation Code	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
22	SRAM Control	W/R	SRAM Write/Read									-
23	VCOM Control 1	W/R	-	VMF[7:0] ((8'b1000_0000)								-
24	VCOM Control 2	W/R	-	VMH[7:0] ((8'b0110_0100)								-
25	VCOM Control 3	W/R	-	VML[7:0] ((8'b0110_0100)								-
26	Display Control 1	W/R	-	I/P_ISC[3:0] (0011)				N/P_ISC[3:0] (0011)				-
27	Display Control 2	W/R	-	PT[1:0] (10)		PTV[1:0](01)		-	(0)	PTG(1)	REF(1)	-
28	Display Control 3	W/R	-	-	-	GON(1)	DTE(0)	D[1:0] (00)		-	-	-
29	Frame Rate control 1	W/R	-	I/PI_RTN[3:0](0000)				N/P_RTN[3:0](0000)				-
2A	Frame Rate Control 2	W/R	-	-	-	I/P_DIV[1:0] (00)		-	-	N/P_DIV[1:0] (00)		-
2B	Frame Rate Control 3	W/R	-	N/P_DUM[7:0](8'b 0001_1110)								-
2h	Frame Rate Control 4	W/R	-	I/PI_DUM[7:0](8'b 0001_1110)								-
2D	Cycle Control 2	W/R	-	GDON[7:0] (8'b0000_0011)								-
2E	Cycle Control 3	W/R	-	GDOF[7:0] (8'b0111_1011)								-
2F	Display inversion	W/R	-	-	I/PI_NW[2:0] (000)			-	N/P_NW[2:0] (001)			-
31	RGB interface control 1	W/R	-	-	-	-	-	-	-	RCM[1:0] (00)		-
32	RGB interface control 2	W/R	-	-	-	-	-	DPL(0)	HSPL(0)	VSPL(0)	EPL(0)	-
33	RGB interface control 3	W/R	-	HBP[7:0] (0000_1000)								-
34	RGB interface control 4	W/R	-	-	VBP[6:0] (00_0010)							-
38	OTP Control 1	W/R	-	OTP_MASK[7:0] (8'b0)								-
39	OTP Control 2	W/R	-	-	OTP_INDEX[6:0] (7'b111_1111)							-
3A	OTP Control 3	W/R	-	OTP_LOAD_DISABLE (0)	OTP_TEST (0)	OTP_POR(0)	OTP_PWE (0)	OTP_PTM[1:0] (00)		VPP_SEL (0)	OTP_PROG (0)	-
3B	OTP Control 4	W/R	-	OTP_DATA[7:0] (8'h00)								-
3C	CABC Control 1	W/R	-	DBV[7:0](8'b0000_0000)								-
3D	CABC Control 2	W/R	-	-	-	BCTRL (0)	-	DD (0)	BL (0)	-	-	-
3E	CABC Control 3	W/R	-	-	-	-	-	-	-	CABC[1:0] (00)		-
3F	CABC Control 4	W/R	-	CMB[7:0](8'b0000_0000)								-
40	r1 Control (1)	W/R	-	-	-	VRP0[5:0] (6'b00_0000)						-
41	r1 Control (2)	W/R	-	-	-	VRP1[5:0] (6'b00_0000)						-
42	r1 Control (3)	W/R	-	-	-	VRP2[5:0] (6'b00_0000)						-
43	r1 Control (4)	W/R	-	-	-	VRP3[5:0] (6'b00_0000)						-
44	r1 Control (5)	W/R	-	-	-	VRP4[5:0] (6'b00_0000)						-
45	r1 Control (6)	W/R	-	-	-	VRP5[5:0] (6'b00_0000)						-
46	r1 Control (7)	W/R	-	-	PRP0[6:0] (7'b000_0000)							-
47	r1 Control (8)	W/R	-	-	PRP1[6:0] (7'b000_0000)							-
48	r1 Control (9)	W/R	-	-	-	-	PKP0[4:0] (5'b0_0000)					-
49	r1 Control (10)	W/R	-	-	-	-	PKP1[4:0] (5'b0_0000)					-
4A	r1 Control (11)	W/R	-	-	-	-	PKP2[4:0] (5'b0_0000)					-
4B	r1 Control (12)	W/R	-	-	-	-	PKP3[4:0] (5'b0_0000)					-
4C	r1 Control (13)	W/R	-	-	-	-	PKP4[4:0] (5'b0_0000)					-
50	r1 Control (18)	W/R	-	-	-	VRN0[5:0] (6'b00_0000)						-
51	r1 Control (19)	W/R	-	-	-	VRN1[5:0] (6'b00_0000)						-
52	r1 Control (20)	W/R	-	-	-	VRN2[5:0] (6'b00_0000)						-
53	r1 Control (21)	W/R	-	-	-	VRN3[5:0] (6'b00_0000)						-
54	r1 Control (22)	W/R	-	-	-	VRN4[5:0] (6'b00_0000)						-
55	r1 Control (23)	W/R	-	-	-	VRN5[5:0] (6'b00_0000)						-
56	r1 Control (24)	W/R	-	-	PRN0[6:0] (7'b000_0000)							-

Commands(continue)

(Hex)	Operation Code	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
57	r1 Control (25)	W/R	-	-	PRN1[6:0] (7'b000_0000)							-
58	r1 Control (26)	W/R	-	-	-	PKN0[4:0] (5'b0_0000)						-
59	r1 Control (27)	W/R	-	-	-	PKN1[4:0] (5'b0_0000)						-
5A	r1 Control (28)	W/R	-	-	-	PKN2[4:0] (5'b0_0000)						-
5B	r1 Control (29)	W/R	-	-	-	PKN3[4:0] (5'b0_0000)						-
5C	r1 Control (30)	W/R	-	-	-	PKN4[4:0] (5'b0_1001)						-
5D	r1 Control (35)	W/R	-	CGMN1[1:0] (2'b00)		CGMN0[1:0] (2'b00)		CGMP1[1:0] (2'b00)		CGMP0[1:0] (2'b00)		-
60	TE Control	W/R	-	-	-	-	TE_mode (0)	TEON (0)	-	-	-	-
61	ID1	W/R	-	ID1[7:0](8'b0000_0000)								-
62	ID2	W/R	-	ID2[7:0](8'b0000_0000)								-
63	ID3	W/R	-	ID3[7:0](8'b0000_0000)								-
64	ID4	W/R	-	ID4[7:0](8'b0000_0000)								-
80	Column address counter 2	W/R	-	-	-	-	-	-	-	-	CAC[8] (0)	-
81	Column address counter 1	W/R	-	CAC[7:0] (8'b0000_0000)								-
82	Row address counter 2	W/R	-	-	-	-	-	-	-	-	RAC[8] (0)	-
83	Row address counter 1	W/R	-	RAC[7:0] (8'b0000_0000)								-
84	TE Output Line2	W/R	-	TSEL15:8] (8'b0)								-
85	TE Output Line2	W/R	-	TSEL[7:0] (8'b0)								-
87	OTP Control 6	W/R	-	OTP_KEY[7:0] (8'b0)								-
E2	VREF comtrol	W/R	-	-	-	0	1	TVREF[3:0] (OTP)				
E3	VLCD control	W/R	-	-	-	0	VDHS_SEL[4:0] (5'b0_1010)					
E4	Power saving counter 1	W/R	-	EQVCI_M1[7:0] (8'b0000_0000)								-
E5	Power saving counter 2	W/R	-	EQGND_M1[7:0] (8'b0001_1000)								-
E6	Power saving counter 3	W/R	-	EQVCI_M0[7:0] (8'b0000_0000)								-
E7	Power saving counter 4	W/R	-	EQGND_M0[7:0] (8'b0001_1000)								-
EA	TRI_CTRL control	W/R	-	0	0	0	0	0	TRI_CTRL (0)	0	0	-
EC	STBA control 1	W/R	-	-	-	-	-	STBA[11:8] (4'b1000)				-
ED	STBA control 2	W/R	-	STBA[7:0] (8'b1110_1100)								-
EE	RTBA control 1	W/R	-	0	0	WL_Delay_EN	0	0	0	0	0	
EF	RTBA control 2	W/R	-	0	1	RTBA[2:0] (3'b001)			0	0	0	-
FF	Page select	W/R	-	-	-	-	-	-	-	PAGE_SEL[1:0] (00)		-

Note:
Please refer to HX8352-B data sheet for details

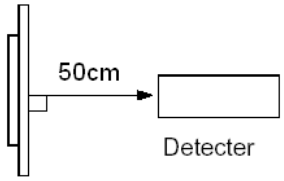
8. Optical Characteristics

Item		Symbol	Condition	MIN.	TYP.	MAX.	UNIT	Note.
Brightness		Bp	θ=0°	280	-	-	Cd/m²	Note 1
Uniformity		△Bp	Φ=0°	80%	-	-	-	Note 1,2
Viewing Angle		θ1 (Φ =90° or270°)	Cr≥10				Deg	Note 3
		θ2 Deg 3 (Φ=0° or 180°)						
Contrast ratio		CR	θ=0° Φ=0° 25℃	-	500	-	-	Note 4
Response Time		T_{on}		-	25	40	msec	Note 5
		T_{off}					msec	
Color of CIE Coordinate	White	X	θ=0° Φ=0°				-	Note 1,6
		Y					-	
	Red	X					-	
		Y					-	
	Green	X					-	
		Y					-	
	Blue	X					-	
		Y					-	
NTSC Ratio		S		-	60%			

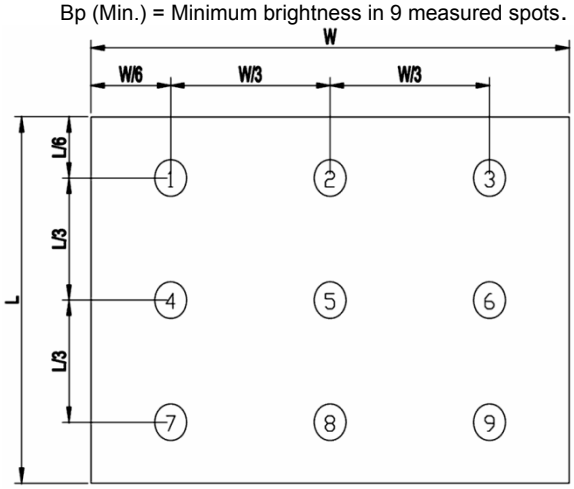
Note：The parameter is slightly changed by temperature, driving voltage and materiel.

Note 1:
The data are measured after LEDs are turned on for 5 minutes. LCM displays full white.
The brightness is the average value of 9 measured spots.
Measurement equipment PR-705 (Φ8mm)
Measuring condition:
- Measuring surroundings: Dark room
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.

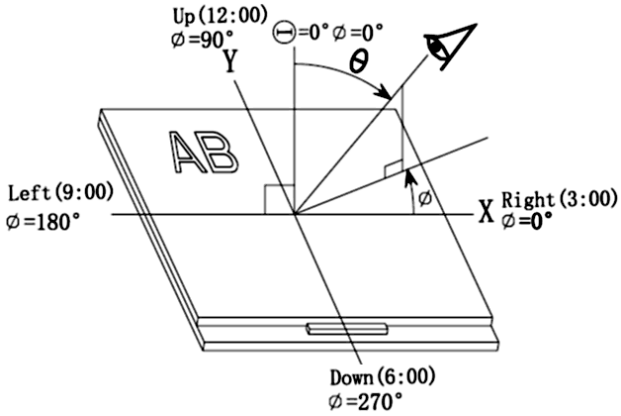
Measured value at the center point of LCD panel after more than 5 minutes while backlight turning on.



Note 2:
The luminance uniformity is calculated by using following formula.
△Bp = Bp (Min.) / Bp (Max.)×100 (%)
Bp (Max.) = Maximum brightness in 9 measured spots
Bp (Min.) = Minimum brightness in 9 measured spots.



Note 3:
The definition of viewing angle:
Refer to the graph below marked by θ and Φ

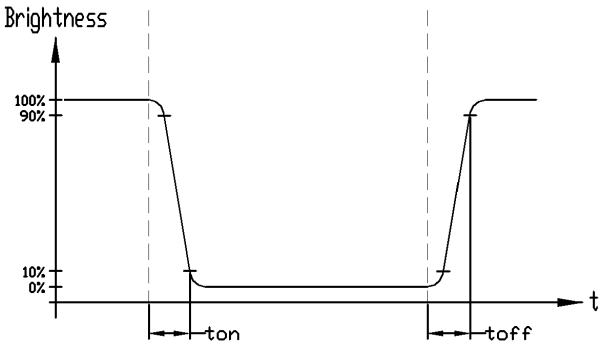


Note 4:
The definition of contrast ratio (Test LCM using PR-705):

$$\text{Contrast Ratio(CR)} = \frac{\text{Luminance When LCD is at “White” state}}{\text{Luminance When LCD is at “Black” state}}$$

(Contrast Ratio is measured in optimum common electrode voltage)

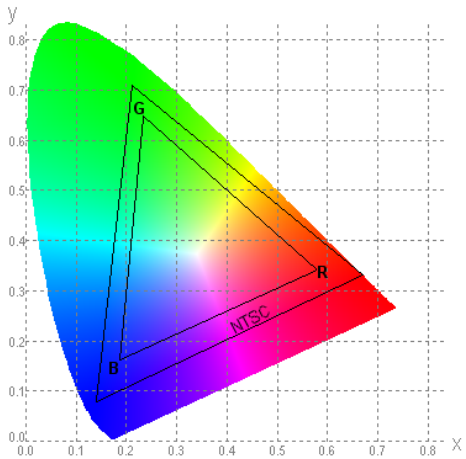
Note 5:
Definition of Response time. (Test LCD using DMS501):
The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.
The response time is defined as the time interval between the 10% and 90% of amplitudes.Refer to figure as below.



Note 6:
Definition of Color of CIE1931 Coordinate and NTSC Ratio.

Color gamut:

$$S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$



9. Precautions of using LCD Modules

Mounting

- Mounting must use holes arranged in four corners or four sides.
- The mounting structure so provide even force on to LCD module. Uneven force (ex. Twisted stress) should not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- It is suggested to attach a transparent protective plate to the surface in order to protect the polarizer. It should have sufficient strength in order to the resist external force.
- The housing should adopt radiation structure to satisfy the temperature specification.
- Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. Never rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics deteriorate the polarizer.)
- When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer

Operating

- The spike noise causes the mis-operation of circuits. It should be within the ±200mV level (Over and under shoot voltage)
- Response time depends on the temperature.(In lower temperature, it becomes longer.)
- Brightness depends on the temperature. (In lower temperature, it becomes lower.) And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
- Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- When fixed patterns are displayed for a long time, remnant image is likely to occur.
- Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference

Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

Storage

When storing modules as spares for a long time, the following precautions are necessary.

- Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

Protection Film

- When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt tore main on the polarizer. Please carefully peel off the protection film without rubbing it against the polarizer.
- When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
- You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

Transportation

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.