深圳市拓普微科技开发有限公司
SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

LMT035DNJFWD

LCD Module User Manual

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Date: 2017-05-19	Date:	Date:

Rev.	Descriptions	Release Date
0.1	Preliminary New release	2017-05-19

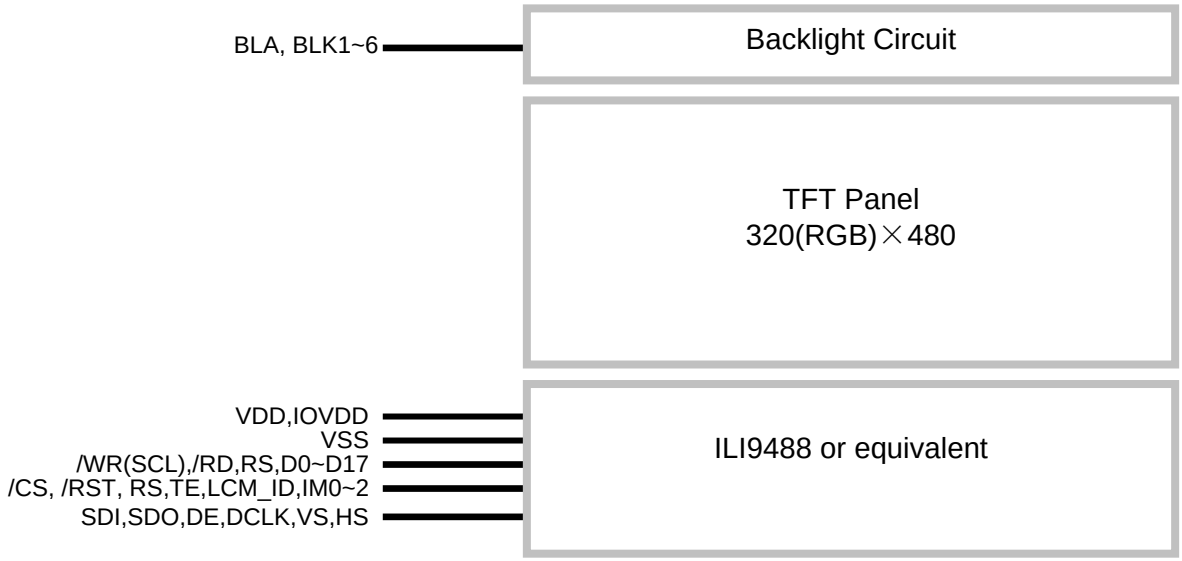
Table of Content

1. Basic Specifications

Screen Size(Diagonal) :	3.5”
Color Depth:	65K/262K Color
Number of dots :	320(RGB)x480
Active Area :	48.96x73.44
Dot Pitch :	0.153x0.153mm
Display Technology :	a-Si TFT active matrix
Display Mode :	Transmissive With Normally white
Pixel Configuration :	RGB Vertical Stripe
Viewing Direction :	12H (*1) (gray scale inverse) 6H (*2)
Polarizer Surface Treatment:	HC
Backlight Type:	LEDs
Outline Dimension :	55.26x 84.69 x 2.2 mm (exclude FPC , see dwg for details)
Operating Temperature :	-20 ~ +70°C (No Condensation)
Storage Temperature :	-30 ~ +80°C (No Condensation)

Note:
*1. For saturated color display content (eg. pure-red, pure-green, pure-blue or pure-colors-combinations).
*2. For “color scales” display content.
*3. Color tone may slightly change by temperature and driving condition.

1.1 Block Diagram



1.2 Terminal Functions

Pin No.	PIN Name	I/O	Descriptions
1	TE	Output	Output a frame head pulse signal If no used, please open this pin
2	VSS	Power	NegAtive power supply,0V
3	DE	Input	Data enable signal in RGB mode If no used, please fix this pin at VSS level
4	DCLK	Input	Pixel clock signal in RGB mode If no used, please connect this pin to VSS
5	VS	Input	Vertical sync. signal in RGB mode If no used, please connect this pin to VSS
6	VSS	Power	Ground
7	HS	Input	Horizontal sync, signal in RGB mode If no used, please connect this pin to VSS
8	IM0	Input	MPU system interface mode select
9	IM1	Input	MPU system interface mode select
10	IM2	Input	MPU system interface mode select
11	IOVDD	Power	IO Positive Power
12	VDD	Power	Positive power supply
13	SDI	I/O	Serial data in/out pin in DBI Type C 9bit mode Serial data input pin in DBI Type B 8bit mode If no used, please connect this pin to vss
14	SDO	Output	Serial data output pin If no used, leave this pin open
15	D17	I/O	Data Bus
:	:	:	
32	D0	I/O	
33	/RST	Input	Reset signal /RST = L, Initialization is executed /RST = H, Normal running.
34	/RD	Input	Read strobe signal If no used, please connect this pin to IOVDD
35	/WR(SCL)	Input	(WR) Write data enable pin in DBI Type B (SCL) Write data enable pin in DBI Type C If no used, please connect this pin to IOVDD
36	RS	Input	Data/command selection pin If no used, please connect this pin to IOVDD
37	/CS	Input	Chip select signal If no used, please connect this pin to IOVDD
38	BLK6	Power	LEDS CATHODE
:	:	:	
43	BLK1	Power	
44	BLA	Power	LED ANODE
45	LCM_ID	Output	Customer requirement：1.8V

IM2	IM1	IM0	Interface	WR/SCL	DATA Bus use	
					Command/Parament	GRAM
0	0	0	DBITYPE-B18-bit (DB_EN='0')	WR	D7~D0	D17~D0:18bits Data
0	0	1	DBI TYPE-B 9-bit	WR	D7~D0	D8 ~D0: 9bits Data
0	1	0	DBI TYPE-B 16-bit	WR	D7~D0	D15~D0:16bits Data
0	1	1	DBI TYPE-B 8-bit	WR	D7~D0	D7 ~D0:8bits Data
1	0	1	DBI TYPE-C Option 1(3 wire)	SCL	SDI/SDO	
1	1	1	DBI TYPE-C Option 3(4 wire)	SCL	SDI/SDO	

System interface select

2. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Power Voltage	VDD	-0.3	+3.3	V	V_{SS} = 0V
Input Voltage	V_{IN}	-0.3	+3.3	V	V_{SS} = 0V
Operating Temperature	T_{OP}	-20	+70	°C	No Condensation
Storage Temperature	T_{ST}	-30	+80	°C	No Condensation

Cautions:
Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

3. Electrical Characteristics

3.1 DC Characteristics

V_{SS}=0V, T_{OP}=25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition / Application Pin
Operating Voltage	VDD	2.65	3.0	3.3	V	VDD,IOVDD
Input High Voltage	V_{IH}	0.7xV_{DD}	-	V_{DD}	V	TE、DE、DCLK、VS、HS、IM0~2、SDI、SDO、D0~D17、/RST、/RD、WR(SCL)、RS、/CS、LCM_ID
Input Low Voltage	V_{IL}	-0.3	-	0.3xV_{DD}	V	
Operating Current	I_{DD}	-	TBD	-	mA	VDD (*1)

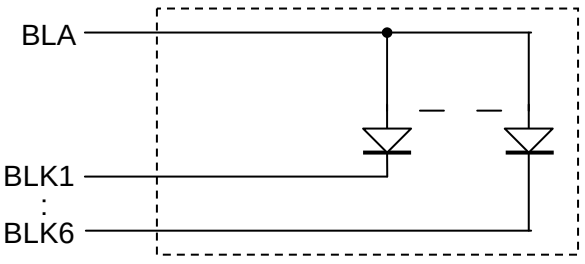
Note: *1. VDD=3.0V

3.2 LED Backlight Circuit Characteristics

BLK(1~6)=0V, I_{BLA}=120mA, T_{OP} =25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Forward Voltage	BLA	-	3.2	-	V	BLA
Forward Current	I_{BLA}	-	120	-	mA	BLA

Cautions:
Exceeding the recommended driving current could cause substantial damage to the backlight and shorten its lifetime.

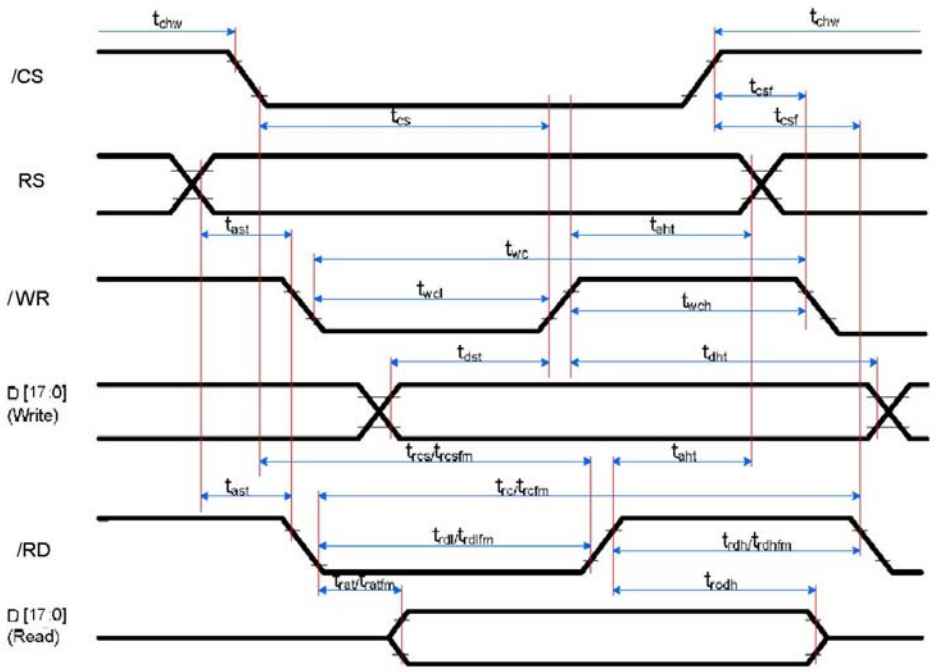


No. of LEDs = 6pcs

4. AC Characteristics

4.1 DBI Type B

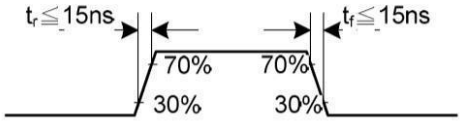
4.1.1 DBI Type B Timing Characteristic



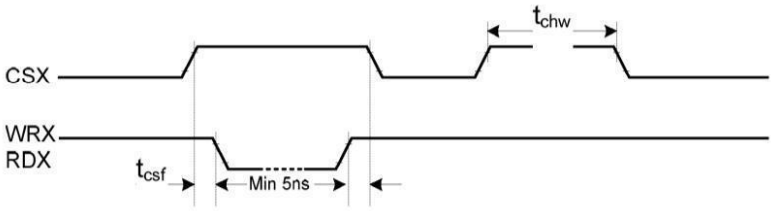
Signal	Symbol	Parameter	min	max	Unit	Description
RS	tast	Address setup time	0	-	ns	-
	that	Address hold time (Write/Read)	0	-	ns	-
/CS	tchw	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	15	-	ns	-
	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
	tcsf	Chip Select Wait time (Write/Read)	0	-	ns	-
/WR	twc	Write cycle	40	-	ns	-
	twrh	Write Control pulse H duration	15	-	ns	-
	twrl	Write Control pulse L duration	15	-	ns	-
/RD(FM)	trcfm	Read Cycle (FM)	450	-	ns	When read from Frame Memory
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
/RD(ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D [17:0], D [15:0], D [8:0], D [7:0]	tdst	Write data setup time	10	-	ns	For maximum, CL=30pF For minimum, CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Notes:

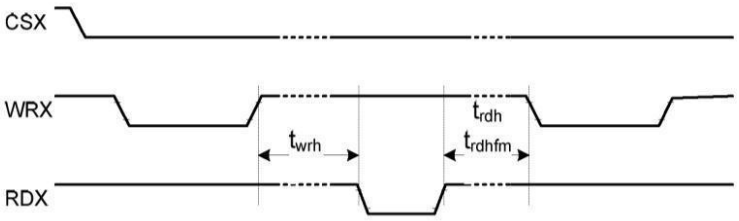
1. Ta = -30 to 70 ℃, IOVDD、VDD = 2.5V to 3.3V, VSS = 0V
2. Logic high and low levels are specified as 30% and 70% of IOVDD for input signals.
3. Input signal rising time and falling time:



4. The CSX timing:

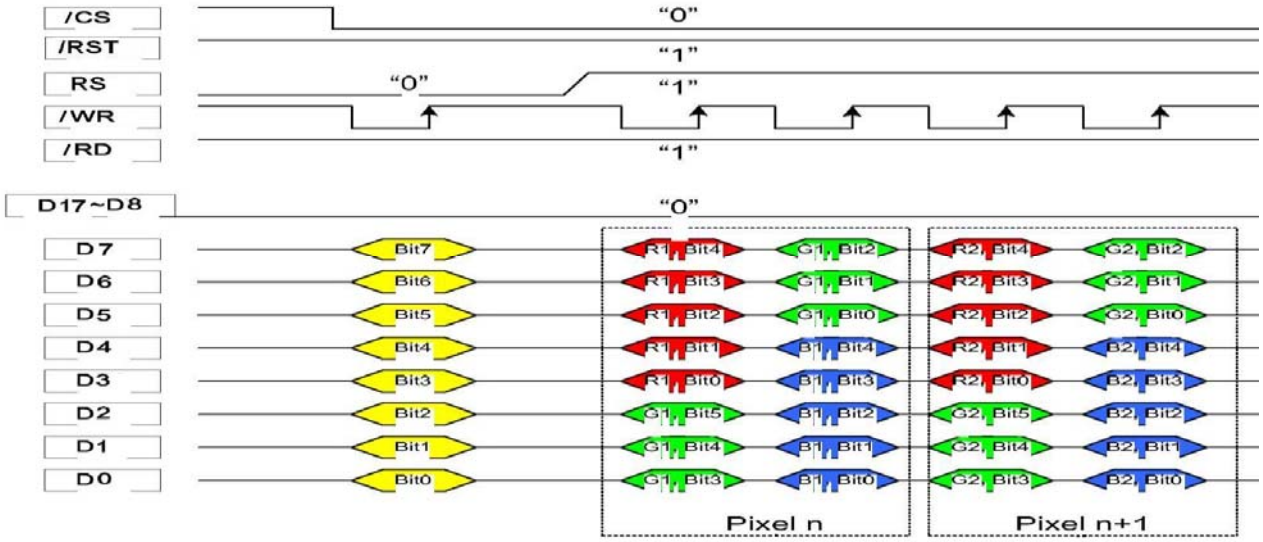


5. The Write to Read or the Read to Write timing:

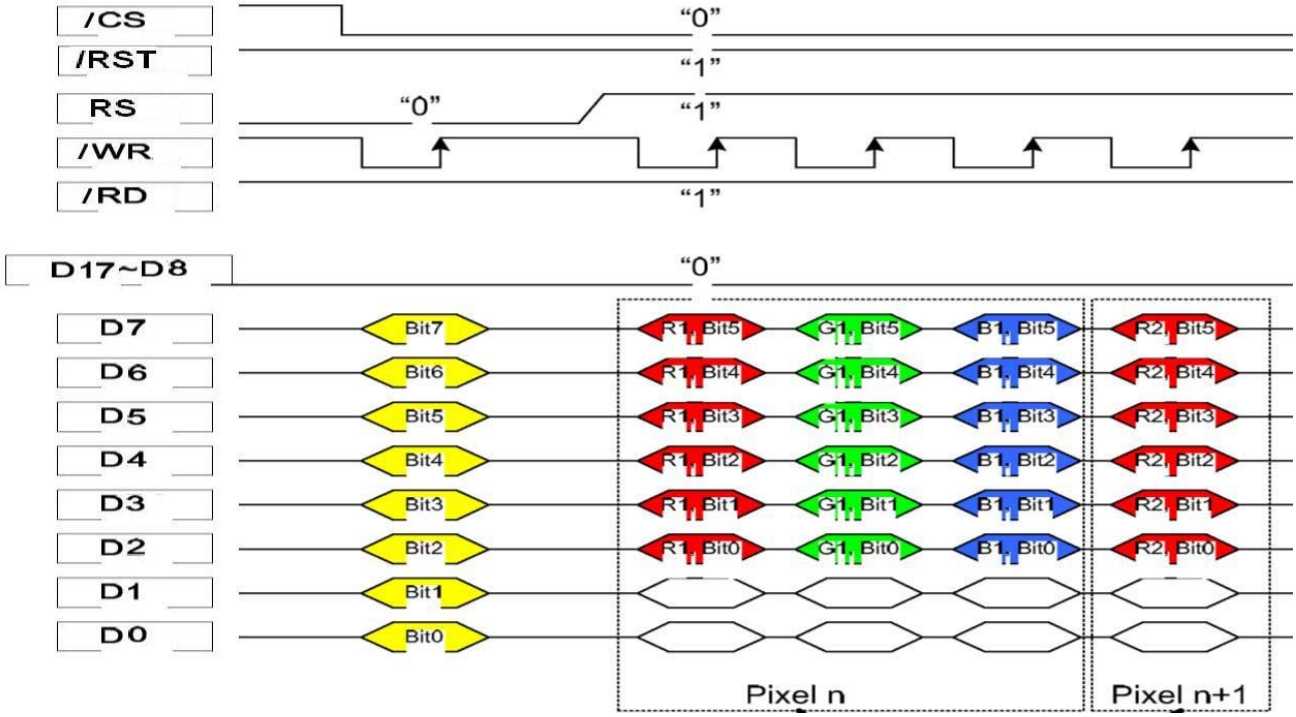


4.1.2 DBI Type B Data Bus

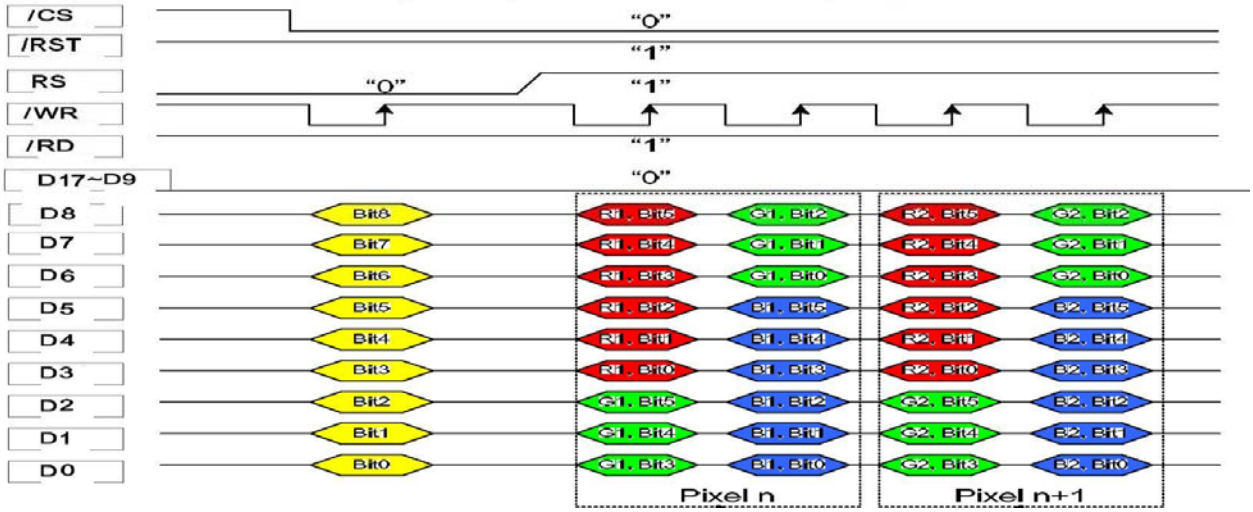
8-bit Data Bus for 16-bit/pixel (RGB 5-6-5 Bits Input), 65K-color



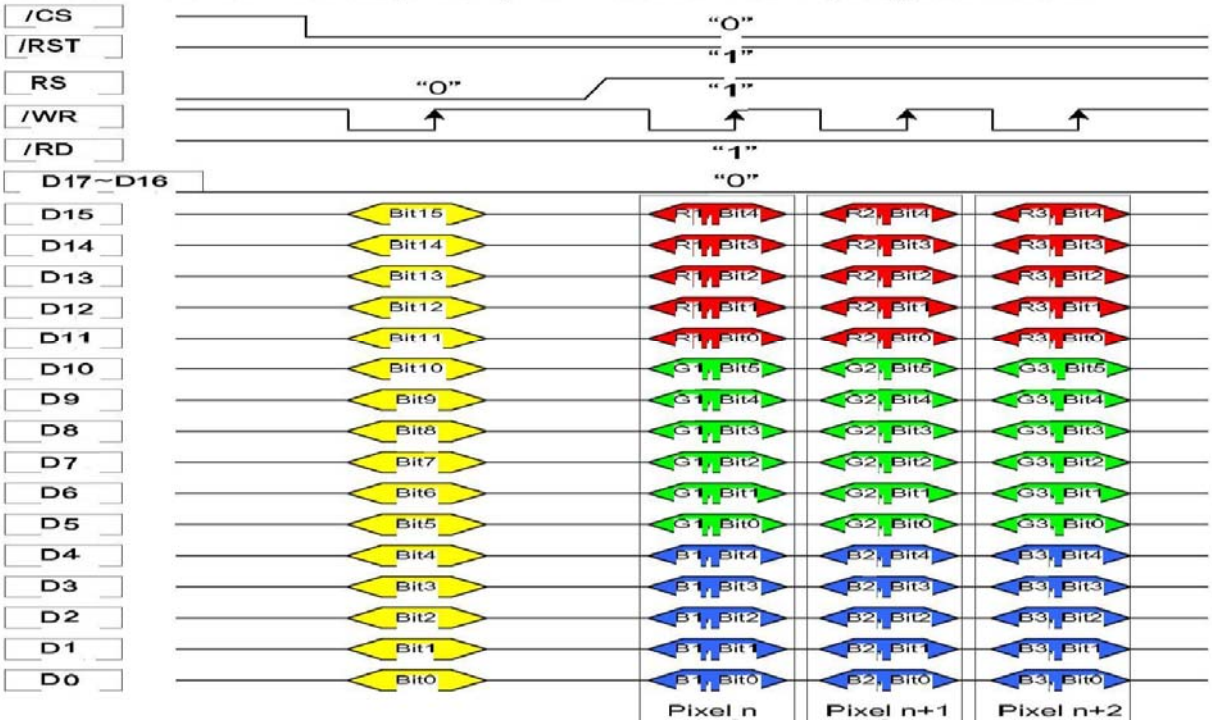
8-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color



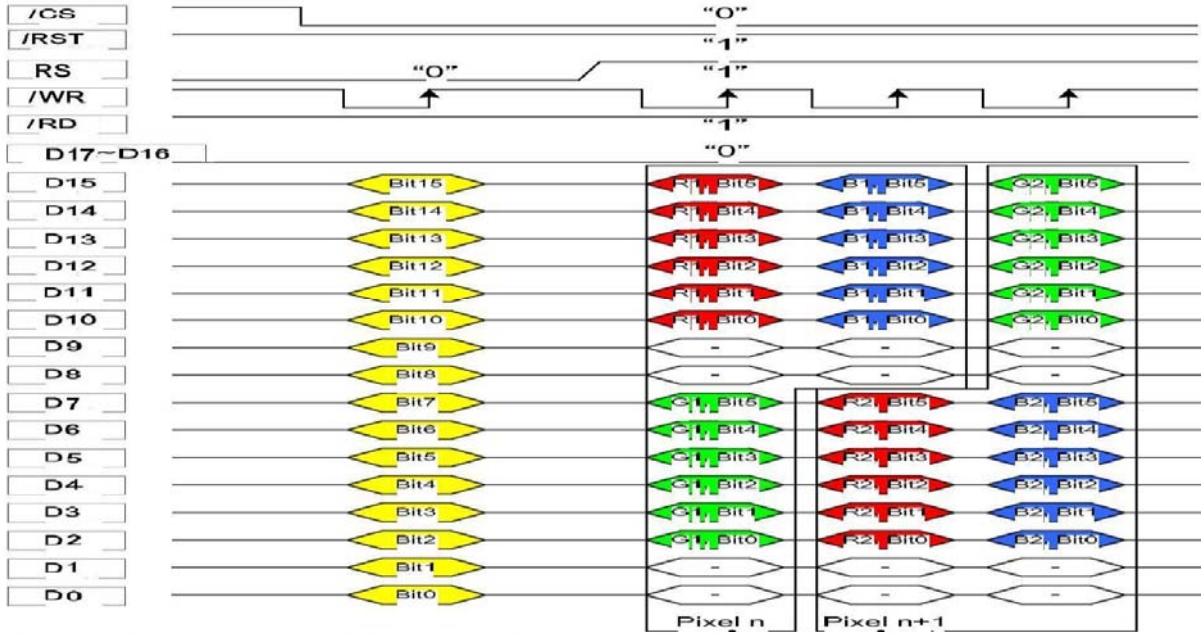
9-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color



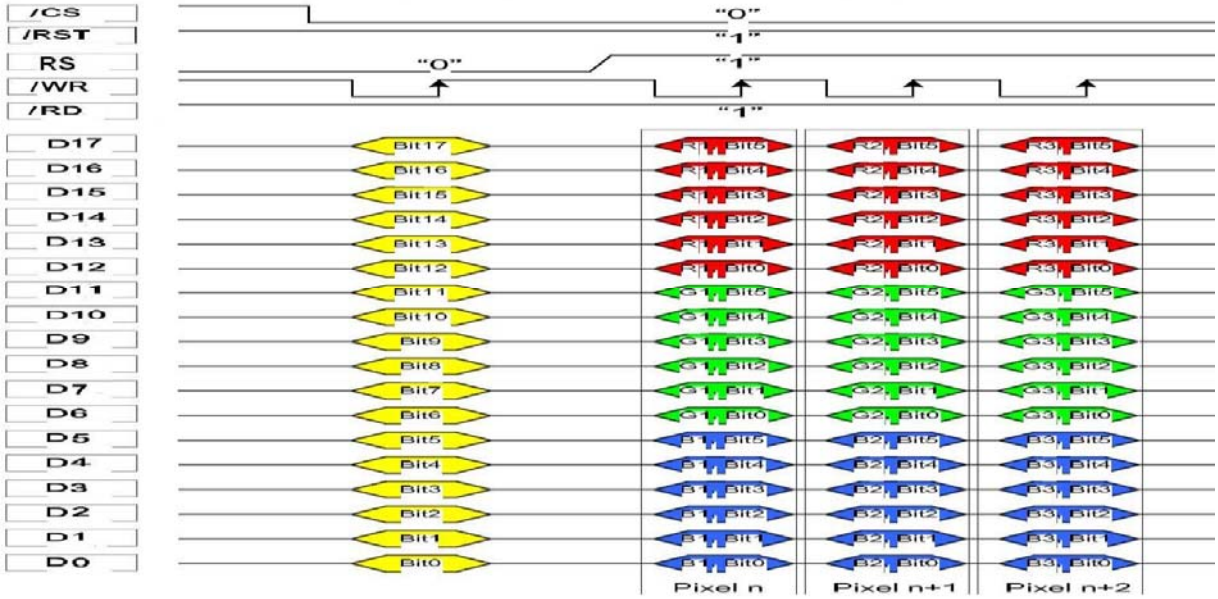
16-bit Data Bus for 16-bit/pixel (RGB 5-6-5 Bits Input), 65K-color



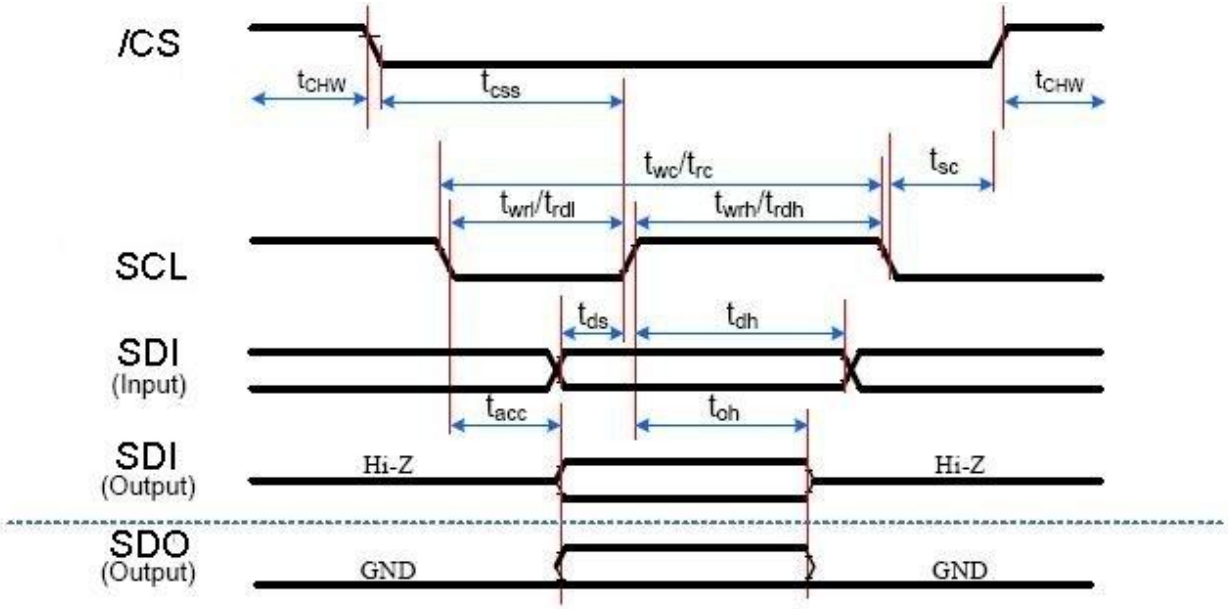
16-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color



18-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

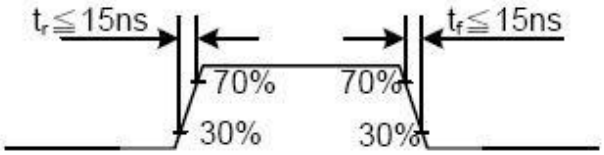


4.2 3-Line SPI Interface Timing Characteristic

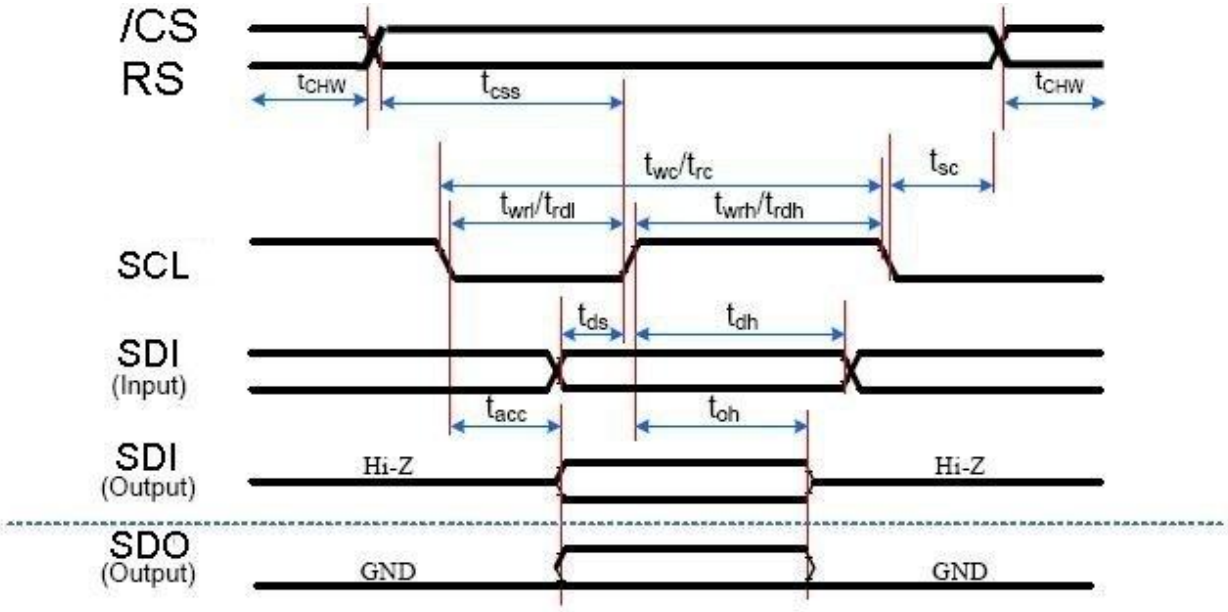


Signal	Symbol	Parameter	min	max	Unit	Description
/CS	tsc	SCL- /CS	15	-	ns	
	tchw	/CS H Pulse Width	40	-	ns	
	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	65	-	ns	
SCL	twc	Serial Clock Cycle (Write)	66	-	ns	
	twrh	SCL H Pulse Width (Write)	15	-	ns	
	twrl	SCL L Pulse Width (Write)	15	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL H Pulse Width (Read)	60	-	ns	
	trdl	SCL L Pulse Width (Read)	60	-	ns	
SDI (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDI/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: Ta = -30 to 70 °C, IOVDD、VDD= 2.5V to 3.3V, VSS = 0V, T = 10+/-0.5ns

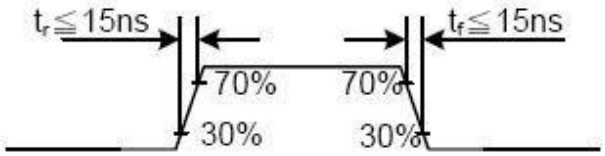


4.3 4-Line SPI Interface Timing Characteristic



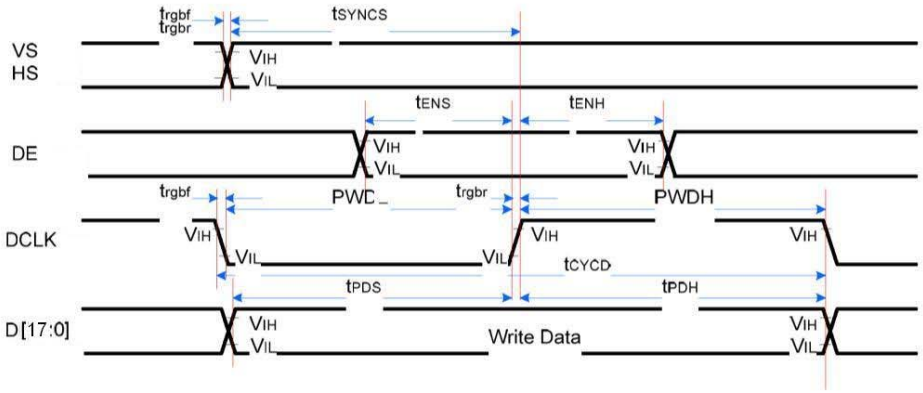
Signal	Symbol	Parameter	min	max	Unit	Description
/CS	tsc	SCL- /CS	15	-	ns	
	tchw	/CS H Pulse Width	40	-	ns	
	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	65	-	ns	
SCL	twc	Serial Clock Cycle (Write)	66	-	ns	
	twrh	SCL H Pulse Width (Write)	15	-	ns	
	twrl	SCL L Pulse Width (Write)	15	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL H Pulse Width (Read)	60	-	ns	
	trdl	SCL L Pulse Width (Read)	60	-	ns	
SDI (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDI/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: Ta = -30 to 70 °C, IOVDD、VDD= 2.5V to 3.3V, VSS = 0V, T = 10+/-0.5ns



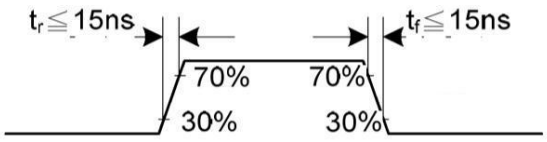
4.4 DPI Interface

4.4.1 DPI Interface Characteristic



Signal	Symbol	Parameter	min	max	Unit	Description
VS HS	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	16-/18-/24-bit bus RGB interface mode
	t_{PDH}	Data hold time	15	-	ns	
DCLK	PWDH	DCLK high-level period	20	-	ns	
	PWDL	DCLK low-level period	20	-	ns	
	t_{CYCD}	DCLK cycle time	50	-	ns	
	t_{rgbr} , t_{rgbf}	DCLK ,HSYNC,VSYNC rise/fall time	-	15	ns	

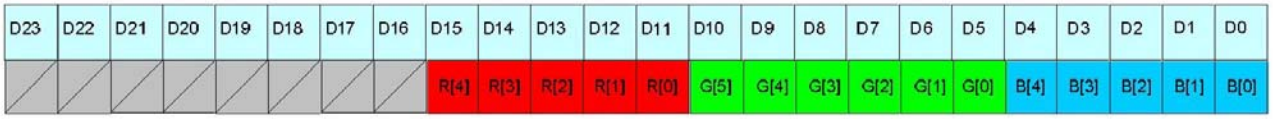
Note: Ta = -30 to 70 ℃, IOVDD、VDD = 2.5V to 3.3V, VSS = 0V



4.4.2 DPI Interface pixel format

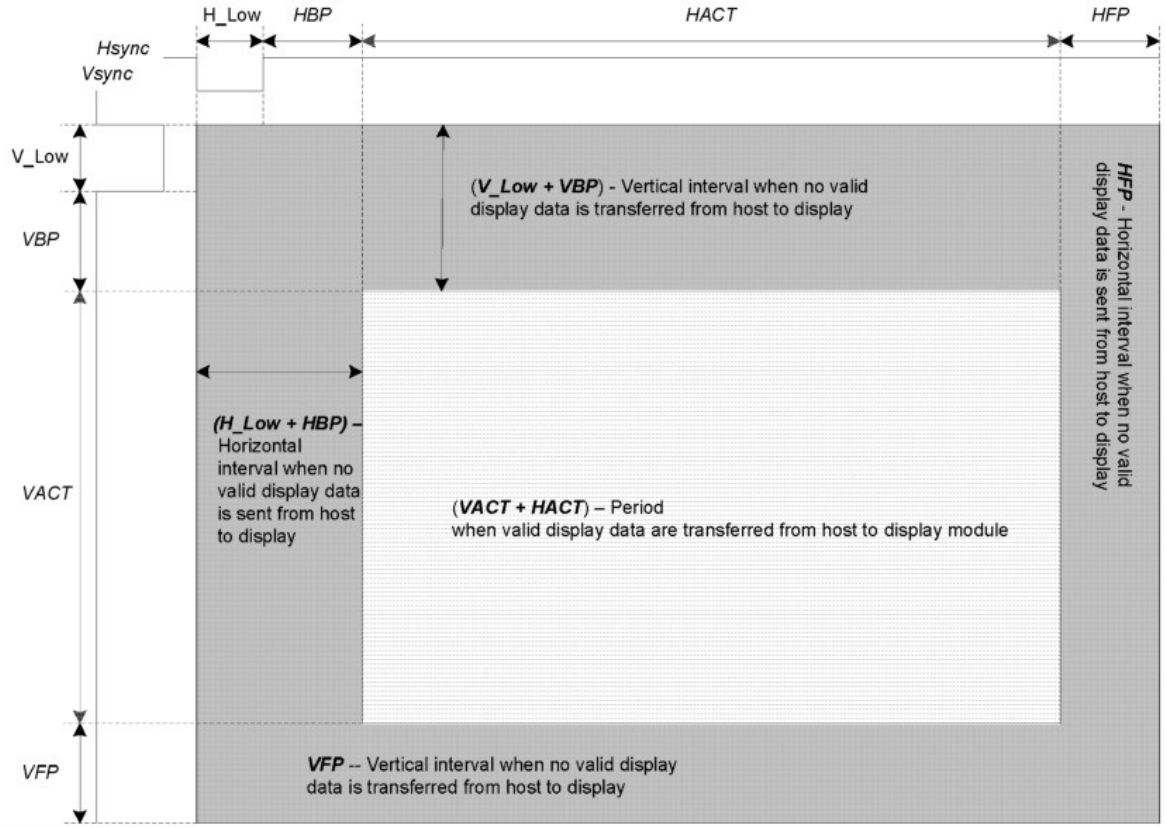
18-bit DPI interface connection (D [17:0] is used): set pixel format DPI [2:0] = 3'h6

16-bit DPI interface connection (D [15:0] is used): set pixel format DPI [2:0] = 3'h5



The Pixel clock (DCLK) runs all the time without stop. It is used to enter VS, HS, DE and D[17: 0] states when there is a rising edge of the DCLK. The DCLK cannot be used as the internal clock for other functions of the display module.
Vertical synchronization (VS) is used to indicate when a new frame of the display is received. This is low enable and its state is read to the display module by a rising edge of the DCLK signal.
Horizontal synchronization (HS) IS used to indicate when a new line of the frame is received. This is low enable and its state is read to the display module by a rising edge of the DCLK signal.
Data Enable (DE) is used to indicate when the RGB information that should be transferred in the display is received. This is a high enable, and its state is read to the display module by a rising edge of the DCLK signal.
D[17:0] is used to indicate what is the information of the image that is transferred on the display (when DE = 0 (low) and there is a rising edge of DCLK). D[17:0] can be 0(low) or 1(high). These lines are read by a rising edge of the DCLK signal. In RGB interface modes, the input display data is written to GRAM first then outputs the corresponding source voltage according to the gray data from GRAM.

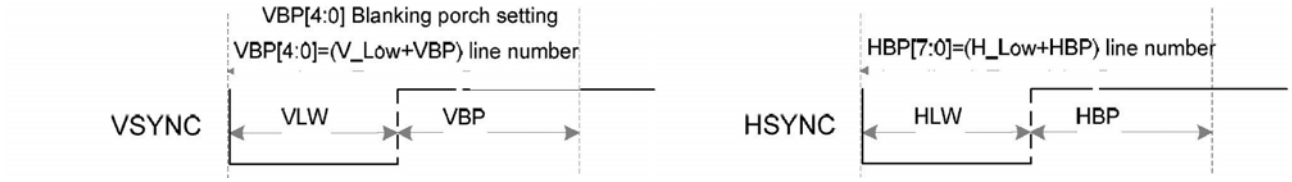
4.4.3 DPI(RGB) Interface timing

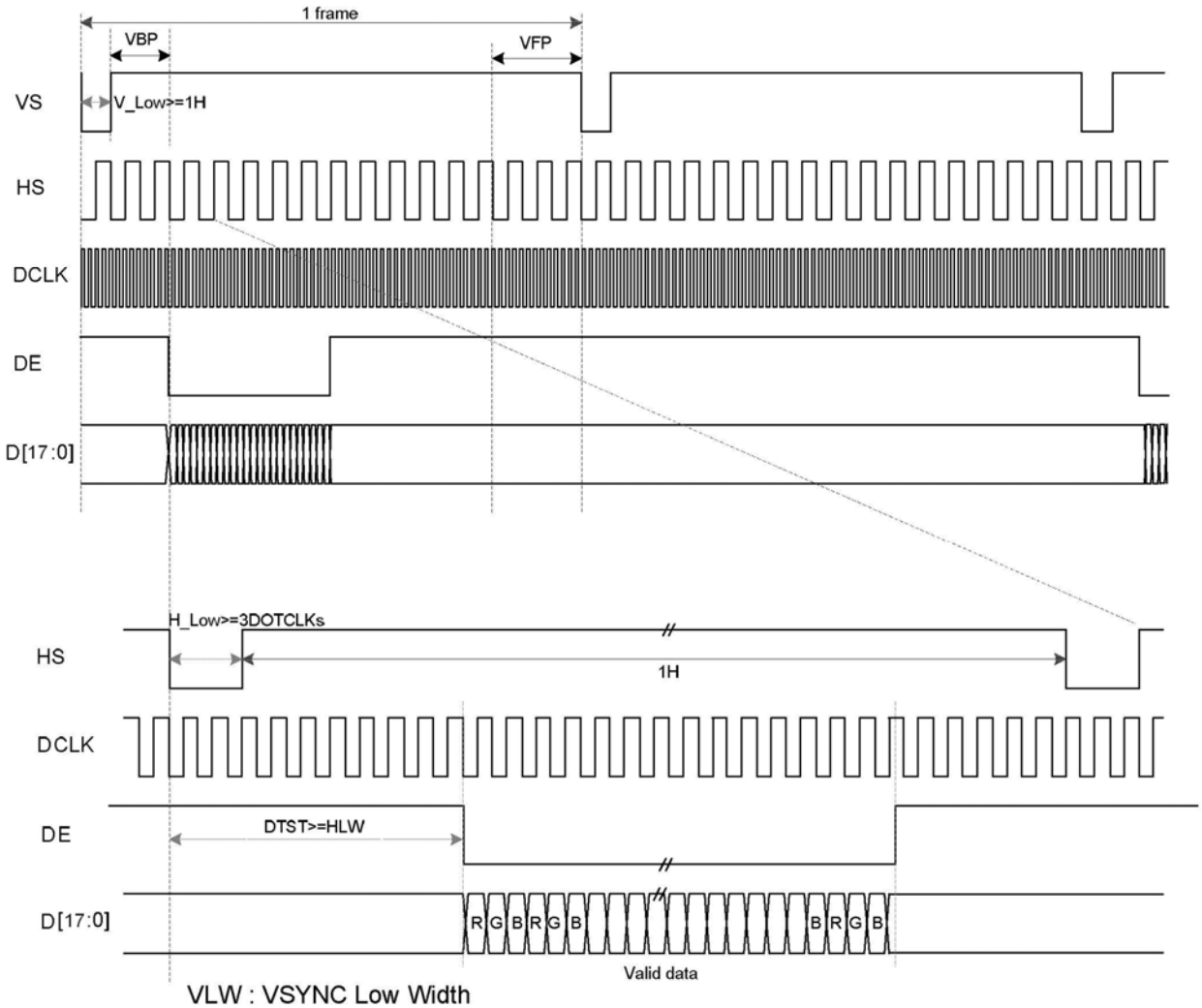


Parameters	Symbols	Min.	Typ.	Max.	Units
Horizontal Synchronization	H_Low	3	-	H_Low+HBP <192	DCLK
Horizontal Back Porch	HBP	3	-		DCLK
Horizontal Front Porch	HFP	3	-	255	DCLK
Horizontal Address	HACT	-	320	-	DCLK
Horizontal Frequency		-	-	33	KHz
Vertical Synchronization	V_Low	1	-	V_Low+VBP+VFP < 32	Line
Vertical Back Porch	VBP	2	-		Line
Vertical Front Porch	VFP	2	-		Line
Vertical Address	VACT	-	480	-	Line
Vertical Frequency		60	-	70	Hz
DCLK cycle		100	-	50	ns
DCLK Frequency		10	-	20	MHz

Example： DCLK = 20Mhz, TE=70Hz, V_Low+VBP=2, VFP=2, H_Low+HBP=100, HFP=170.

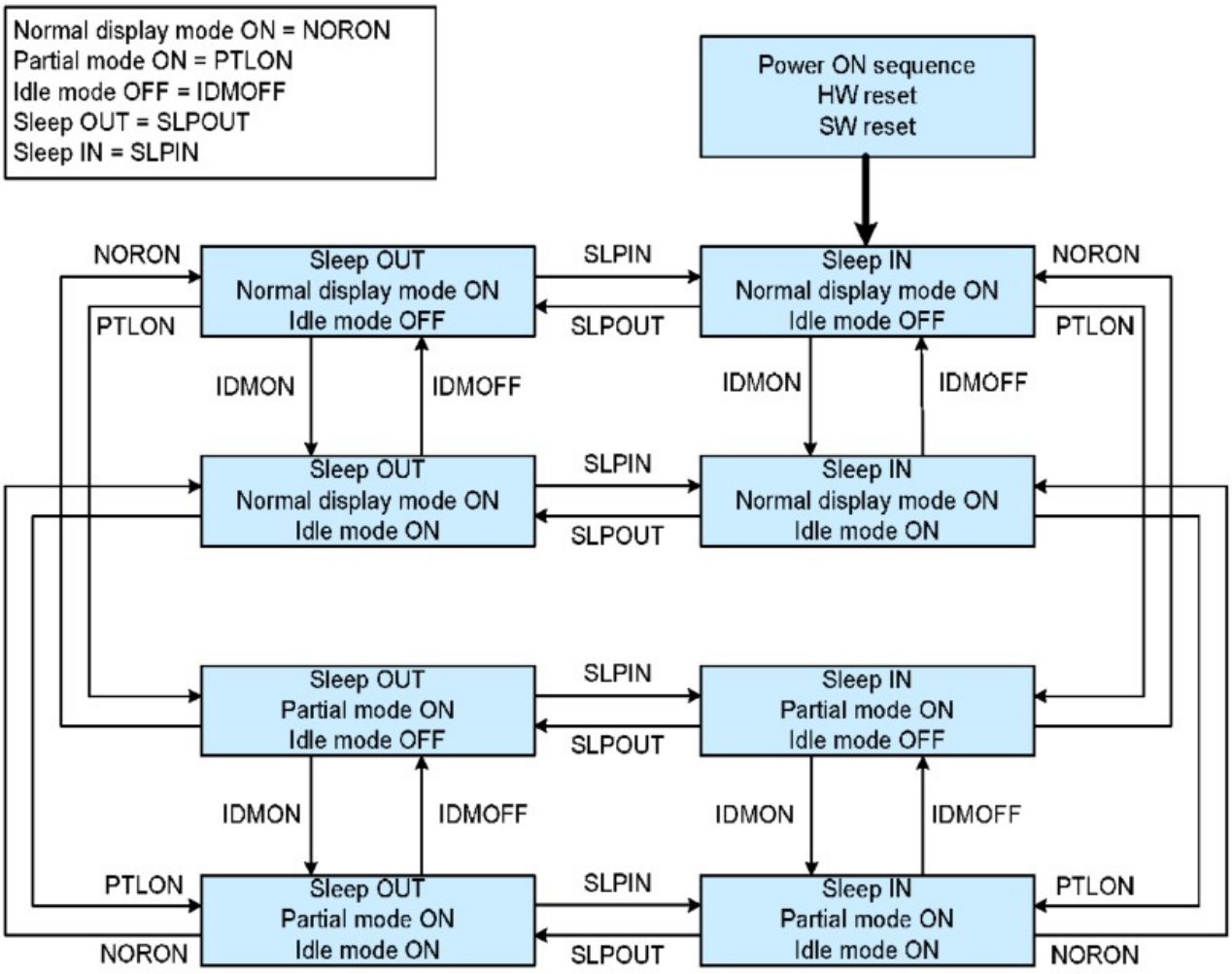
Note: VBP[4:0]/HBP[7:0] (Blanking Porch Control, RB5h) define as follows:





VLW : VSYNC Low Width
HLW : HSYNC Low Width
DTST : Data Transfer Startup Time

4.5 Power ON/OFF Sequence



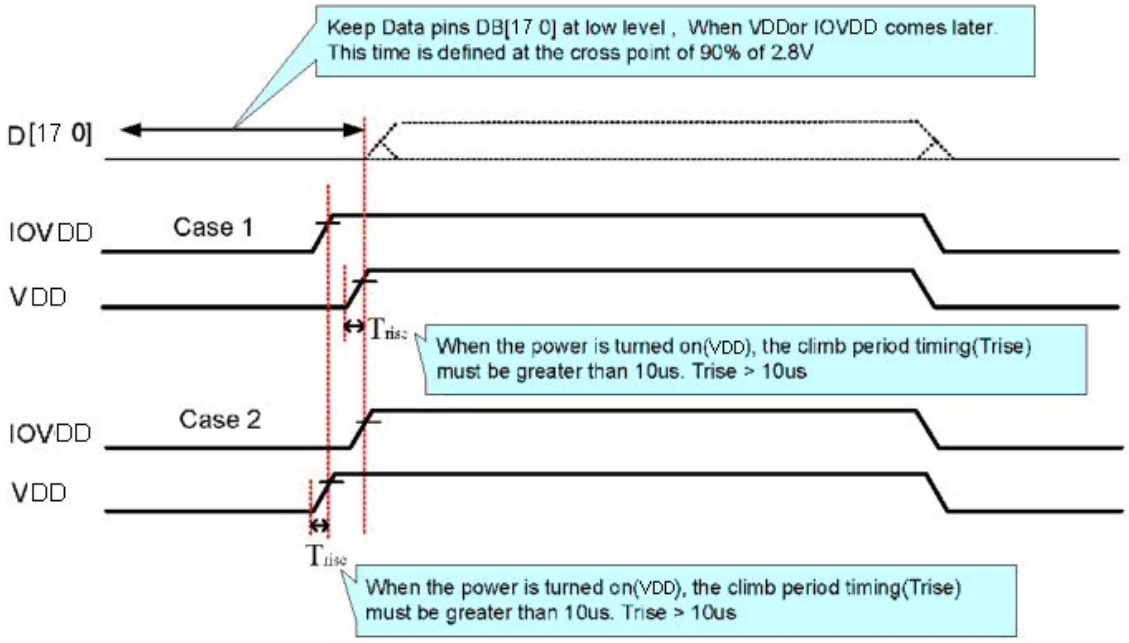
Notes:

1. There are not any abnormal visual effects when one power mode changes to another power mode.
2. There is not any limitation, which is not specified by users, when one power mode changes to another power mode.

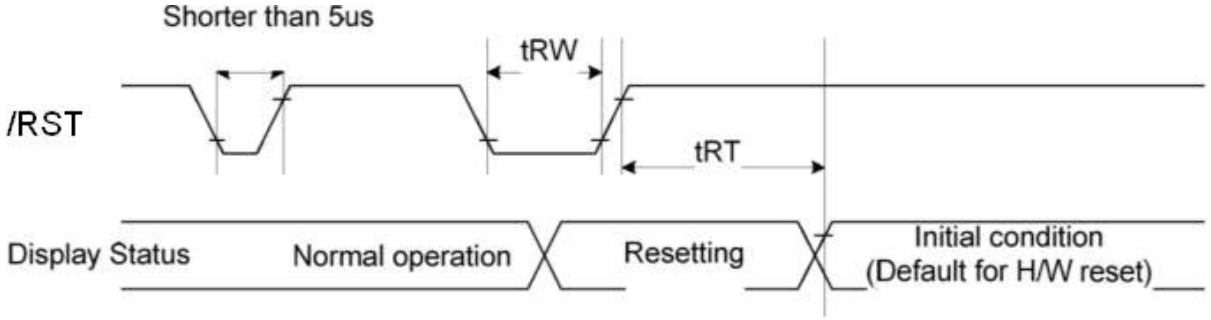
IOVDD and VDD can be applied or powered down in any order. During the Power Off sequence ,if the LCD is in the Sleep In mode, VDD and IOVDD must be powered down with a minimum of 120 msec.If the LCD is in the Sleep In mode, VDD and IOVDD can be powered down with a minimum of 0msec after the /RST has been released. /CS can be applied at any time or can be permanently grounded. /RST has priority over /CS.

Notes:

1. There will be no damage to the ILI9488 if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequence.
3. There will be no abnormal visible effects on the display between the end of the Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the /RST line is not steadily held by the host during the Power On Sequence as defined in Sections 11.1 and 11.2 (ILI9488 datasheet), then it will be necessary to apply the Hardware /RST after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.
5. When the power is turned on, the climb period timing (Trise) must be greater than 10us.
6. Keep data pins D[17:0] at low level, or IOVDD comes later



4.6 Reset timing



Item	Symbol	MIN.	TYP.	MAX.	Unit
Reset LOW pulse width	t_{RW}	1.0	-	-	us
Reset time	T_{RT}	-	-	120	ms

5 . Optical Characteristics

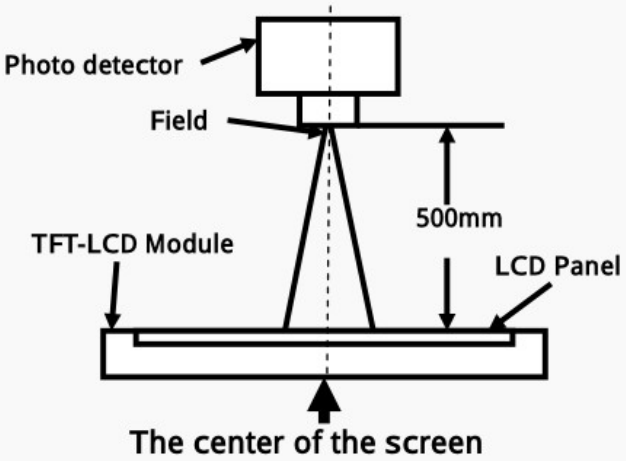
Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	60	70		Degree	Note2,3
		θB		50	60			
		θL		60	70			
		θR		60	70			
Contrast Ratio		CR	θ=0°	400	500			Note 3
Response Time		T_{ON}	25℃		25	35	ms	Note 4
		T_{OFF}						
Chromaticity	White	x	Backlight is on		0.286			Note 1,5
		y			0.304			
	Red	x			0.608			Note 1,5
		y			0.336			
	Green	x			0.341			Note 1,5
		y			0.604			
	Blue	x			0.146			Note 1,5
		y			0.073			
Uniformity		U			80		%	Note 6
NTSC					60		%	Note 5
Luminance		L		250			cd/m^2	Note 7

Test Conditions:

1. I_{BLA} = 120 mA, and the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.

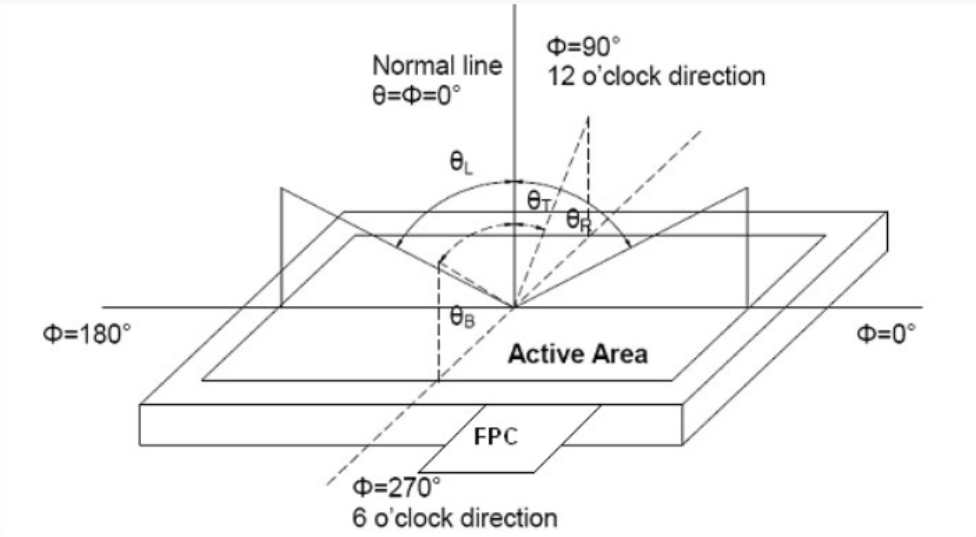
The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80)。



Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

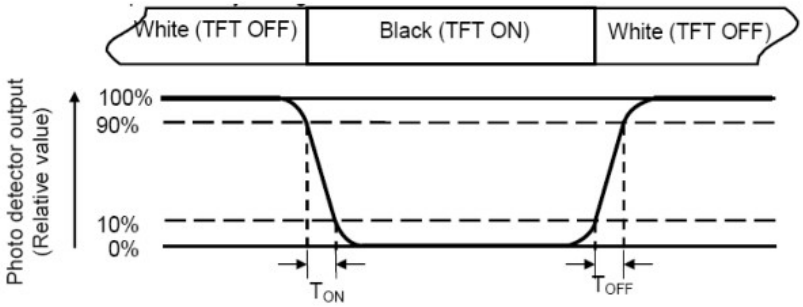
"White state ": The state is that the LCD should drive by Vwhite.

"Black state": The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

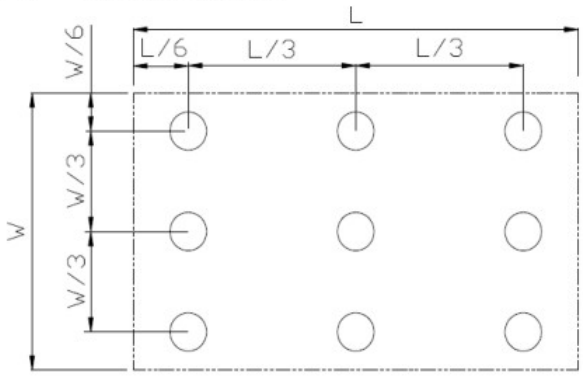
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length W----- Active area width



Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

6. Design and Handling Precaution

1. The LCD panel is made by glass. Any mechanical shock (eg. dropping form high place) will damage the LCD module.
2. Do not add excessive force on the surface of the display, which may cause the Display color change abnormally.
3. The polarizer on the LCD is easily get scratched. If possible, do not remove the LCD protective film until the last step of installation.
4. Never attempt to disassemble or rework the LCD module.
5. Only Clean the LCD with Isopropyl Alcohol or Ethyl Alcohol. Other solvents (eg. water) may damage the LCD.
6. When mounting the LCD module, make sure that it is free form twisting, warping and distortion.
7. Ensure to provide enough space (with cushion) between case and LCD panel to prevent external force adding on it, or it may cause damage to the LCD or degrade the display result.
8. Only hold the LCD module by its side. Never hold LCD module by add force on the heat seal or TAB.
9. Never add force to component of the LCD module. It may cause invisible damage or degrade of the reliability.
10. LCD module could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect the LCD module.
11. When peeling off the protective film from LCD, static charge may cause abnormal display pattern. It is normal and will resume to normal in a short while.
12. Take care and prevent get hurt by the LCD panel sharp edge.
13. Never operate the LCD module exceed the absolute maximum ratings.
14. Keep the signal line as short as possible to prevent noisy signal applying to LCD module.
15. Never apply signal to the LCD module without power supply.
16. IC chip (eg. TAB or COG) is sensitive to the light. Strong lighting environment could possibly cause malfunction. Light sealing structure casing is recommend.
17. LCD module reliability may be reduced by temperature shock.
18. When storing the LCD module, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature. They may damage or degrade the LCD module