深圳市拓普微科技开发有限公司
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LMT035KDH03-NHA

LCD Module User Manual

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Date: 2018-03-19	Date:	Date:

Rev.	Descriptions	Release Date
0.1	New release	2015-11-09
0.2	Update Section 2.1	2018-03-19

Table of Content

1. General Specification

Screen Size(Diagonal) :	3.5 inch
Resolution :	320(RGB) x 240
Interface :	8bit MCU Interface / SPI Interface
Color Depth :	16.7M color (24bit)
Dot Pitch :	0.219 x 0.219 (mm)
Pixel Configuration :	RGB Stripe
Display Mode :	Transmissive / Positive
Surface Treatment :	Anti-Glare Treatment
Viewing Direction :	6 o'clock
Outline Dimension :	92.7 x 72.0 x 10.25 (mm)
Active Area :	70.08 x 52.56 (mm)
Weight :	Approx 68g
Backlight :	LED, White
Operating Temperature :	-20 ~ +70°C
Storage Temperature :	-30 ~ +80°C

Note: Backlight color may slightly change over temperature and driving voltage.

2. Block Diagram

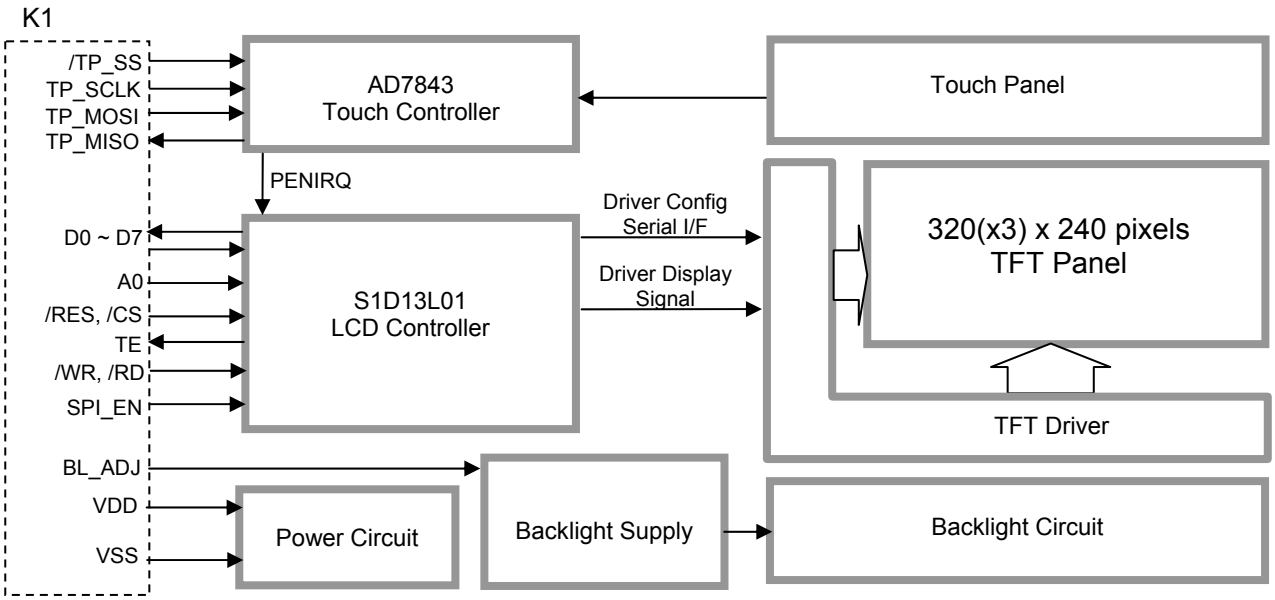


Figure 1

2.1 Terminal Functions

Terminal (K1)

Pin No.	Pin Name	I/O	8bit MCU Mode (Default) Description	SPI Mode Description
1	VSS	Power Input	Power Supply GND (0V)	
2				
3	VDD	Power Input	Positive Power Supply	
4				
5	A0	Input	Access Mode A0=High: Accessing Data A0=Low: Accessing Address	Keep open
6	/CS	Input	Chip Select /CS=Low: Data IO is enabled	
7	/RES	Input	Reset /RES=Low: Reset /RES=High: Normal operation	
8	D0(SI)	Bi-directional I/O	8-bit Bi-directional data bus	Serial input
9	D1(SO)			Serial output
:	:			Keep open
14	D6			Keep open
15	D7			Keep open
16	TE	Output	TE Signal	
17	/RD	Input	Read Enable, active Low	Keep open
18	/WR(SCK)	Input	Write Enable, active Low	Serial clock
19	BL_ADJ	Input	Backlight Driver enable signal, active High, PWM(*3) can be possible	
20	SPI_EN	Input	Keep open	SPI Enable, active high
21	/TP_SS	Input	Touch Panel Serial Select /TP_SS=Low: Data IO is enabled	
22	TP_SCLK	Input	Touch Panel Serial Clock	
23	TP_MOSI	Input	Touch Panel Master output Slave input	
24	TP_MISO	Output	Touch Panel Master input Slave output	

Note:

1. *By default, Pin21 to Pin24 are just for Module with Touch Panel using, and PENIRQ of Touch Panel will feedback to the GPIO3 of S1D13L01 LCD controller, PENIRQ enable is LOW.*
2. *The Origin of Touch Panel in the lower left corner.*
3. *The PWM frequency is between 200Hz and 500Hz.*

For more information and details of Touch please refer to Touch controller (AD7843) datasheet.

3. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	V_{DD}	-0.2	3.7	V	V_{SS} = 0V
Input Voltage	V_{IN}	-0.2	3.7	V	V_{SS} = 0V
Operating Temperature	T_{OP}	-20	+70	℃	No Condensation
Storage Temperature	T_{ST}	-30	+80	℃	No Condensation

Caution:
Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

4. Electrical Characteristics

4.1 DC Characteristics

V_{SS}=0V, V_{DD} =3.3V, T_{OP} =25℃

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Operating Voltage	V_{DD}	2.8	3.3	3.6	V	VDD
Input High Voltage	V_{IH}	-	-	VDD	V	Input pins, Bi-direction pins
Input Low Voltage	V_{IL}	VSS	-	-	V	Input pins, Bi-direction pins
Output High Voltage	V_{OH}	2.6	-	-	V	Bi-direction pins (*1)
Output Low Voltage	V_{OL}	-	-	0.6	V	Bi-direction pins (*2)
Operating Current	I_{DD}	-	145	200	mA	On Backlight Power on status

4.2 AC Characteristics

4.2.1 8080 Mode Timing

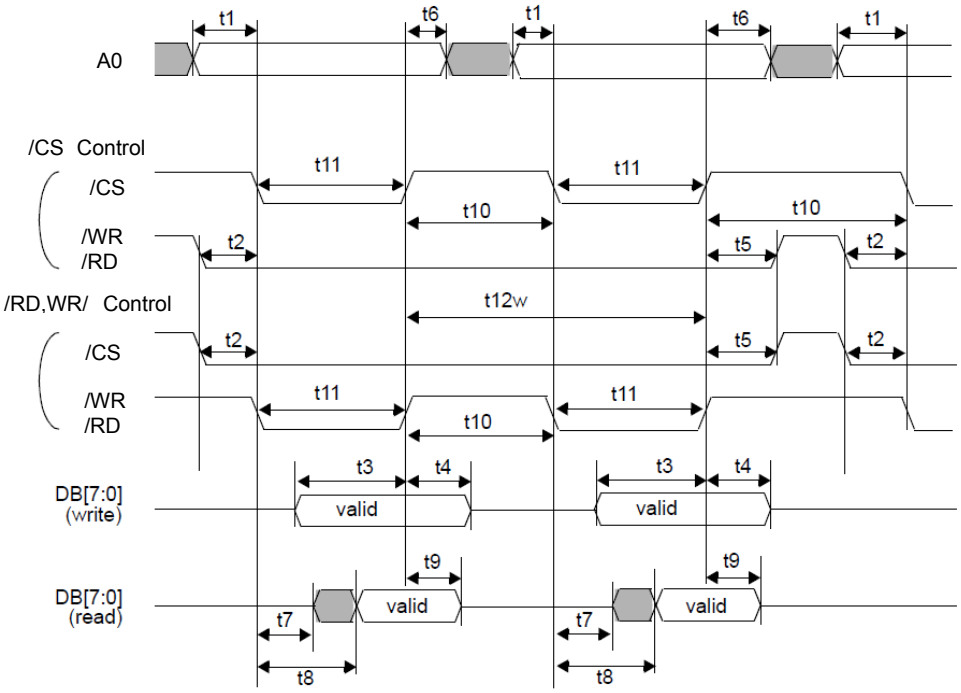


Figure 2

Symbol	Parameter	3.3 Volt		Units
		Min	Max	
t1	A0 setup time to /CS (/WR, /RD)	1	-	ns
t2	/WR, /RD (/CS) setup time to /CS (/WR, /RD)	1	-	ns
t3	DB[7:0] setup time to /CS (/WR) rising edge: write cycle	1	-	ns
t4	DB[7:0] hold time from /CS (/WR) rising edge: write cycle	7	-	ns
t5w	/WR (/CS) hold time from /CS (/WR) rising edge: write cycle	3	-	ns
t5r	/RD (/CS) hold time from /CS (/RD) rising edge: read cycle	0	-	ns
t6	A0 hold time from /CS (/WR, /RD) rising edge	4	-	ns
t7	/CS (/RD) falling edge to DB[7:0] driven: read cycle	-	15	ns
t8	/CS (/RD) falling edge to valid Data: read cycle	-	4xT_{mclk}+17	ns
t9	DB[7:0] hold time from /CS (/RD) rising edge: read cycle	2	12	ns
t10w	End of write to next read/write	5	-	ns
t10r	End of read to next read/write	T_{mclk}+9	-	ns
t11w	/CS (/WR) pulse width for write cycle	3	-	ns
t12w	/CS (/WR) rise to next /CS (/WR) rise: write cycle	3xT_{mclk}+6	-	ns

Note: T_{mclk} = period of internal MCLK clock signal.

Indirect 8-bit Function Select:

A0	/WR	/RD	Comments
0	0	1	Command Write (register address)
1	0	1	Data (Parameter) Write
0	1	0	inhibit
1	1	1	Data (Parameter) Read

4.2.2 SPI Mode Timing

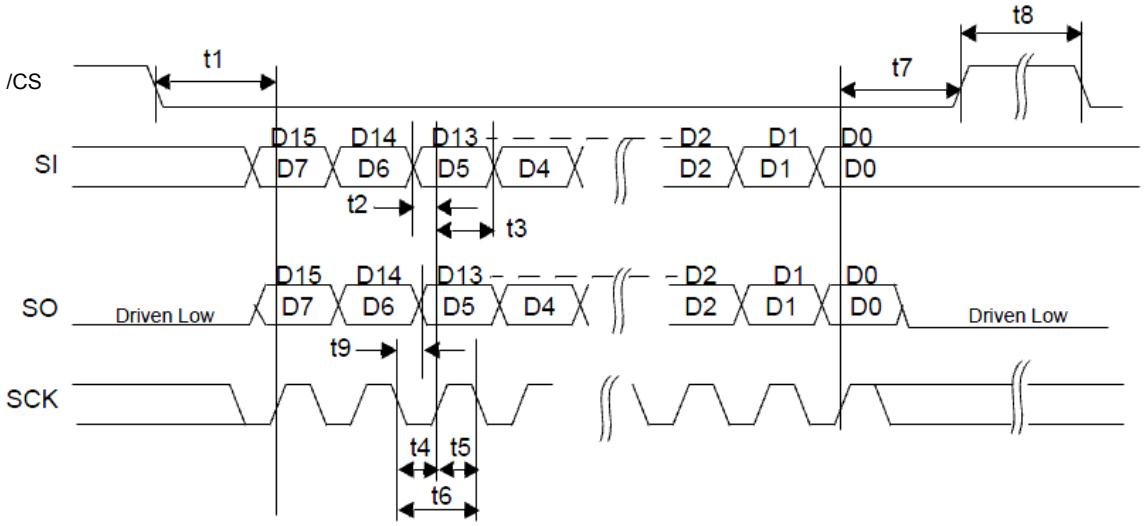


Figure 3

Symbol	Parameter	3.3 Volt		Units
		Min	Max	
t1	Chip select setup time	2	-	ns
t2	SI Data setup time	1	-	ns
t3	SI Data hold time	7	-	ns
t4	Serial clock pulse width low (high)	15	-	ns
t5	Serial clock pulse width high (low)	15	-	ns
t6	Serial clock period	30	-	ns
t7	Chip select hold time	7	-	ns
t8	Chip select de-assert to reassert	2	-	ns
t9	SCK falling edge to SO hold time	3	10	ns

SPI Function Select:

Command	Comments
10000000	8-bit Write
11000000	8-bit Read
10001000	16-bit Write
11001000	16-bit Read
the other	reserved

Write Procedure:

SPI 8bit Write Sequence:

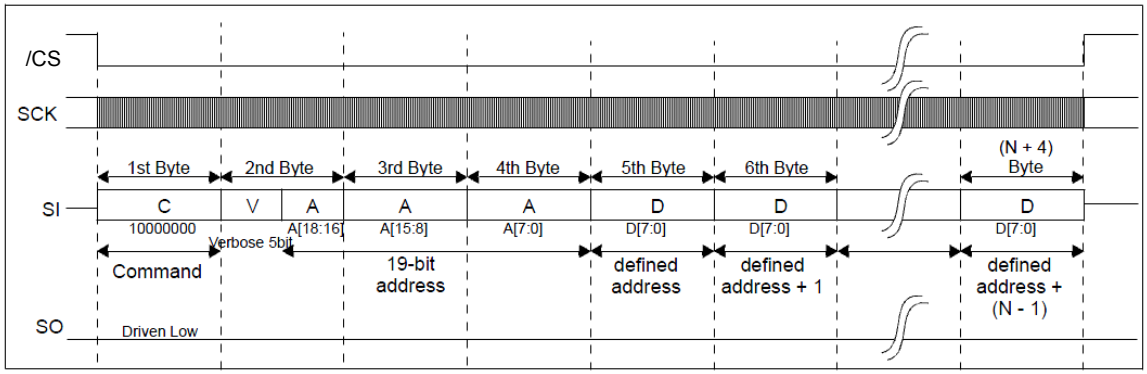


Figure 4

SPI 16bit Write Sequence:

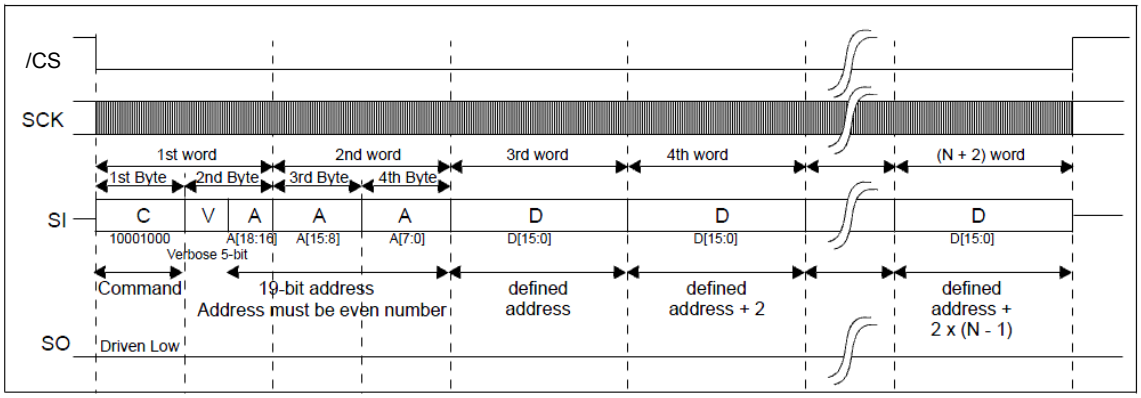


Figure 5

Read Procedure:

SPI 8bit Read Sequence:

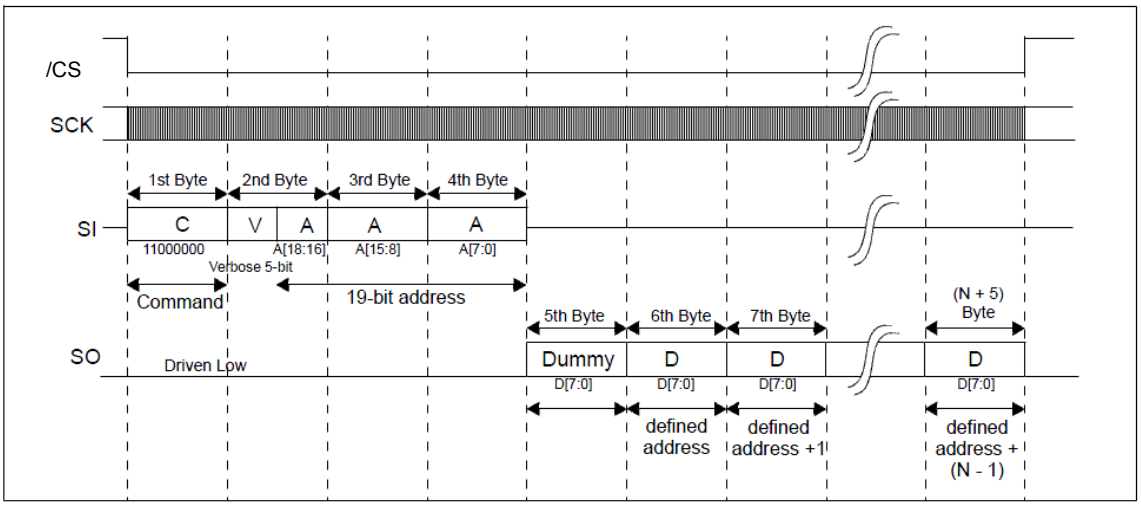


Figure 6

SPI 16bit Read Sequence:

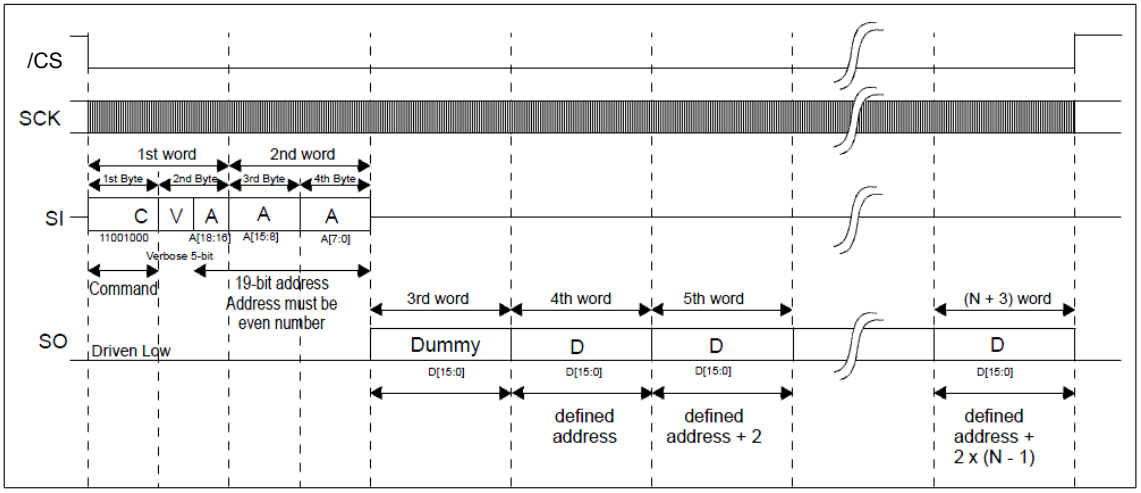


Figure 7

4.2.3 Reset Timing

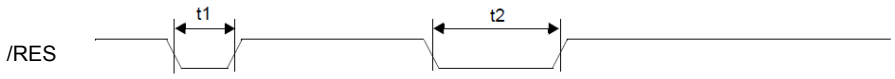


Figure 8

Symbol	Parameter	Min	Max	Units
t1	Reset Pulse Width is ignored	-	42	ns
t2	Active Reset Pulse Width (see Note)	150	-	ns

Note: The Reset input should be held low for longer than 150ns to guarantee reset.

For more information and details please refer to LCD controller (S1D13L01) datasheet.

5. Optical Characteristics

Item	Symbol		Condition	Min.	Typ.	Max.	Unit	Note
Brightness	Bp		θ=0° Φ=0°	-	250	-	Cd/m^2	1
Uniformity	△Bp			80%	-	-		1,2
Viewing Angle	θ1 (Φ=90° or270°)		Cr≥10	-25～+60			Deg	3
	θ2 (Φ=0° or 180°)			-45～+45				
Contrast Ratio	Cr		θ=0° Φ=0°	-	300	-	-	4
Response Time	T_r			-	25	40	ms	5
	T_f			-	25	40	ms	
Color of CIE Coordinate	W	x	θ=0° Φ=0°	-	0.29	-	-	1,6
		y		-	0.31	-	-	
	R	x		-	0.60	-	-	
		y		-	0.37	-	-	
	G	x		-	0.34	-	-	
		y		-	0.57	-	-	
	B	x		-	0.15	-	-	
		y		-	0.09	-	-	
NTSC Ratio	S			50	-		%	

Note：The parameter may slightly change over temperature, driving voltage and materials.

Note 1:
The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment PR-705 (Φ8mm)
Measuring condition:
- Measuring surroundings: Dark room
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.

Measured value at the center point of LCD panel after more than 5 minutes while backlight turning on.

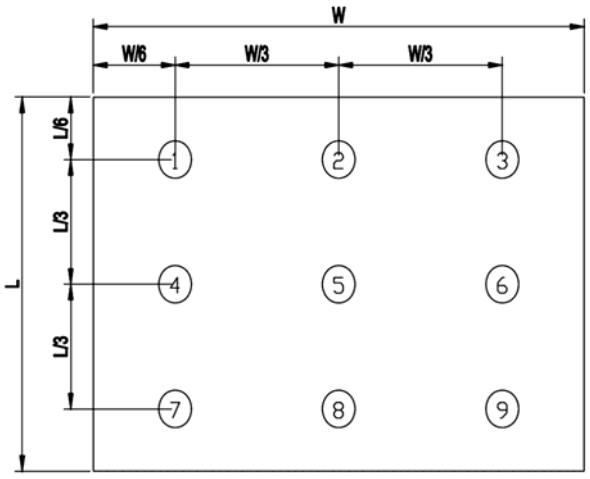


Figure 9

Note 2: reference Figure5
The luminance uniformity is calculated by using following formula.
△Bp = Bp (Min.) / Bp (Max.)×100 (%)
Bp (Max.) = Maximum brightness in 9 measured spots
Bp (Min.) = Minimum brightness in 9 measured spots.

Note 3: reference Figure6
The definition of viewing angle:
Refer to the graph below marked by θ and Φ

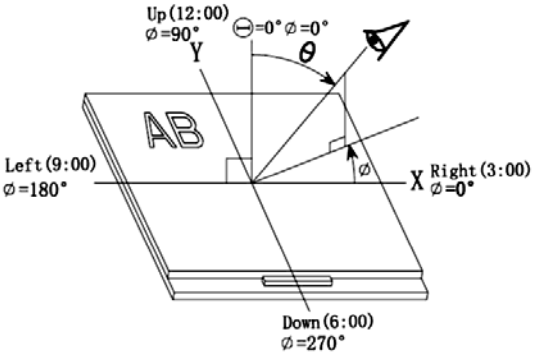


Figure 10

Note 4:
The definition of contrast ratio (Test LCM using PR-705):

$$\text{Contrast Ratio(CR)} = \frac{\text{Luminance When LCD is at "White" state}}{\text{Luminance When LCD is at "Black" state}}$$

(Contrast Ratio is measured in optimum common electrode voltage)

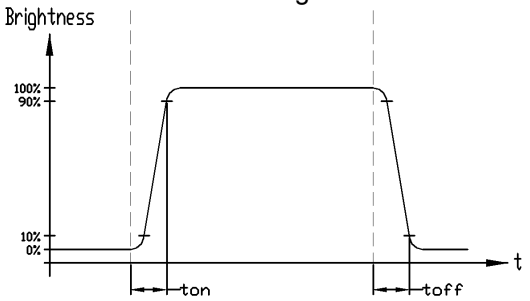


Figure 11

Note 5: reference Figure7
Definition of Response time. (Test LCD using DMS501):
The output signals of photo detector are measured when the input signals are changed from "black" to "white"(falling time)
and from "white" to "black"(rising time), respectively.
The response time is defined as the time interval between the 10% and 90% of amplitudes.Refer to figure as below.

Note 6: reference Figure8
Definition of Color of CIE Coordinate and NTSC Ratio.

Color gamut:

$$S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

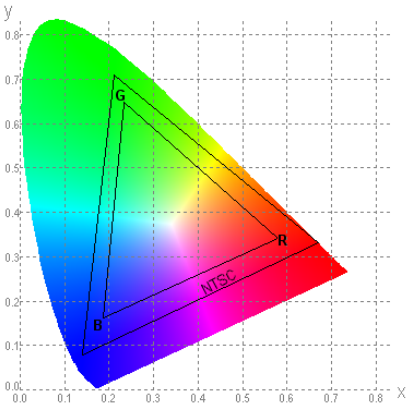


Figure 12

6. Function Specifications

6.1 Command Summary

Command	Para-meter	HEX	A0	/CS	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
Power Save	P1	60804	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Power Save Configuration Register
	P2	D[7:0]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	Power Save		Bit[1:0] = 00 , PSM0 mode Bit[1:0] = 01 , PSM1 mode Bit[1:0] = 1x , NMM mode
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
Software Reset	P1	60806	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Software Reset Register(Write Only)
	P2	D[7:0]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	Bit[8] = 0 , no effect in hardware Bit[8] = 1 , all registers are reset to default values
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	Software Reset	
PLL Setting 0	P1	60810	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PLL Setting Register 0
	P2	D[7:0]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	PLL Bypass	PLL Enable	Bit[0] = 0 , the PLL is disabled Bit[0] = 1 , the PLL enabled Bit[1] = 0 , PLL is selected Bit[1] = 1 , CLKI is selected Bit[15] = 0 , the PLL output is not stable Bit[15] = 1 , the PLL output is stable
		D[15:8]	1	0	0	PLL Lock (RO)	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
PLL Setting 1	P1	60812	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PLL Setting Register 1
	P2	D[7:0]	1	0	0	M-Divider								Bit[9:0] 000h,001h … … 019h,020h : 1:1 ,2:1 … … 33:1(M-Divide Ratio). 021h to 13Fh: Reserved, PFDCLK = CLKI ÷ (M-Divider + 1) Bit[13:10] , must be set to 0000
		D[15:8]	1	0	0	n/a	n/a	N-Counter				M-Divider		
PLL Setting 2	P1	60814	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PLL Setting Register 2
	P2	D[7:0]	1	0	0	L-Counter								Bit[9:0] , must be set between 010h ~ 041h. , and get the M-Divide Ratio from 17:1 to 66:1. POCLK = (L-Counter + 1) x (N-Counter + 1) x PFDCLK
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	L-Counter		
Internal Clock Configuration	P1	60816	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Internal Clock Configuration Register
	P2	D[7:0]	1	0	0	n/a	n/a	n/a	n/a	n/a	PCLK Divide Select			Bit[3:0] = 0000b,0001b … … 1110b,1111b : 1:1 ,2:1 … … 16:1(MCLK to PCLK Frequency Ratio)
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
Panel Setting Miscellaneous	P1	60820	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Panel Setting Miscellaneous Register
	P2	D[7:0]	1	0	0	DE Polarity		PCLK Polarity	n/a	Panel Data Enable	Panel Data Width		Panel Port Enable	Bit[0] = 0 , TFT panel is disable Bit[0] = 1 , TFT panel is enable Bit[2:1] = 01 , TFT 16-bit Bit[2:1] = 10 , TFT 18-bit Bit[2:1] = 11 , TFT 24-bit Bit[3] = 0 , panel data is disable Bit[3] = 1 , panel data is enable Bit[5] = 0, the LCD data outputs transition on the rising edge of PCLK Bit[5] = 1 , the LCD data outputs transition on the falling edge of PCLK Bit[7:6] = 00 , DE Polarity Low active Bit[7:6] = 01 , DE Polarity High active Bit[7:6] = 10 , DE Polarity Fixed to Low Bit[7:6] = 11 , DE Polarity Fixed to High
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
Display Settings	P1	60822	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Display Settings Register
	P2	D[7:0]	1	0	0	TE Status (RO)	TE Function		Display Blank	n/a	Display Blank Polarity	SW Video Invert	Panel Interface Enables	Bit[0] = 0 , HS, VS, DE and PCLK are fixed to H or L and the display pipes are disabled Bit[0] = 1 , enable the panel output and display pipes Bit[1] = 0 , video data is normal Bit[1] = 1 , video data is inverted Bit[2] = 0 , the display blank function operates normally Bit[2] = 1 , the display blank function switches polarity Bit[4] = 0 , the LCD data is masked Bit[4] = 1 , all applicable LCD data outputs are forced to zero or one Bit[6:5] = 00b , TE output is disabled and the pin output is low Bit[6:5] = 01b , TE output is high (1) when the display is in the Vertical Non-Display Period (VNDP) and low (0) when the display is in Vertical Display Period (VDISP) Bit[6:5] = 10b , Line Count Bit[6:5] = 11b , Reserved Bit[7] = 0 , the selected condition in not occurring Bit[7] = 1 , the selected condition in not occurring Bit[8] = 0 , TE is output Bit[8] = 1 , TE is not output
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	TE Output Pin Disable	
HDISP	P1	60824	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Horizontal Display Width Register (HDISP)
	P2	D[7:0]	1	0	0	n/a	Horizontal Display Width							Bit[6:0] = horizontal display width in pixels ÷ 8
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
HNDP	P1	60826	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Horizontal Non-Display Period Register (HNDP)
	P2	D[7:0]	1	0	0	n/a	Horizontal Non-Display Period							Bit[6:0] = horizontal non-display period in PCLK's
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
VDISP	P1	60828	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Vertical Display Height Register (VDISP)
	P2	D[7:0]	1	0	0	Vertical Display Height								Bit[9:0] = vertical display height in lines
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	Vertical Display Height		
VNDP	P1	6082A	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Vertical Non-Display Period Register (VNDP)
	P2	D[7:0]	1	0	0	Vertical Non-Display Period								Bit[7:0] = vertical non-display period in lines
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	

Command	Para-meter	HEX	A0	/CS	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
HSW	P1	6082C	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								HS Pulse Width Register (HSW)
	P2	D[7:0]	1	0	0	HS Pulse Polarity	HS Pulse Width							Bit[6:0] = HS pulse width in PCLK's Bit[7] = 0 , the horizontal sync signal is active low Bit[7] = 1 , the horizontal sync signal is active high
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
HPS	P1	6082E	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								HS Pulse Start Position Register (HPS)
	P2	D[7:0]	1	0	0	n/a	HS Pulse Start Position							Bit[6:0] = HS pulse start position in PCLK's
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
VSW	P1	60830	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								VS Pulse Width Register (VSW)
	P2	D[7:0]	1	0	0	VS Pulse Polarity	n/a	VS Pulse Width						Bit[5:0] = VS pulse width in lines Bit[7] = 0 , the vertical sync signal is active low Bit[7] = 1 , the vertical sync signal is active high
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
VPS	P1	60832	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								VS Pulse Start Position Register (VPS)
	P2	D[7:0]	1	0	0	VS Pulse Start Position								Bit[7:0] = VS pulse start position in lines
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
TE Line Count	P1	60834	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								TE Line Count Register
	P2	D[7:0]	1	0	0	TE Line Count								These bits specify the line count value that is compared with the internal vertical line counter
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	TE Line Count		
Main Layer Setting	P1	60840	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Main Layer Setting Register
	P2	D[7:0]	1	0	0	n/a	n/a	n/a	Main Layer Rotation Select		Main Layer Color Depth			Bit[2:0] = 000b, RGB 8:8:8 (default) Bit[2:0] = 001b, RGB 5:6:5 Bit[2:0] = 010b/011b/111b, Reserved Bit[2:0] = 100b, 24 bpp + LUT1 Bit[2:0] = 101b, 16 bpp + LUT1 Bit[2:0] = 110b, 8 bpp + LUT1 Bit[4:3] = 00b, 0° (Normal) Bit[4:3] = 01b, 90° Bit[4:3] = 10b, 180° Bit[4:3] = 11b, 270° Bit[8] = 0, Synchronous latching of multi-byte layer registers is enabled Bit[8] = 1, Synchronous latching of multi-byte layer registers is disabled
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	Multi-Byte Layer Registers Synchronous Latching Disable	
Main Layer Start Address 0	P1	60842	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Main Layer Start Address Register 0
	P2	D[7:0]	1	0	0	Main Layer Start Address								Bit[15:0] is Bit[15:0] of Main Layer Start Address ,but Bit[1:0] must be set to 00b
		D[15:8]	1	0	0	Main Layer Start Address								
Main Layer Start Address 1	P1	60844	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Main Layer Start Address Register 1
	P2	D[7:0]	1	0	0	n/a		n/a	n/a	n/a	Main Layer Start Address			Bit[2:0] is Bit[18:16] of Main Layer Start Address
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
Main Layer Width	P1	60846	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Main Layer Width Register
	P2	D[7:0]	1	0	0	Main Layer Width								Read Only
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	Main Layer Width		
Main Layer Height	P1	60848	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Main Layer Height Register
	P2	D[7:0]	1	0	0	Main Layer Height								Read Only
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	Main Layer Height		
PIP Layer Setting	P1	60850	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PIP Layer Setting Register
	P2	D[7:0]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	Bit[2:0] = 000b, RGB 8:8:8 (default) Bit[2:0] = 001b, RGB 5:6:5 Bit[2:0] = 010b/011b/111b, Reserved Bit[2:0] = 100b, 24 bpp + LUT1 Bit[2:0] = 101b, 16 bpp + LUT1 Bit[2:0] = 110b, 8 bpp + LUT1 Bit[4:3] = 00b, 0° (Normal) Bit[4:3] = 01b, 90° Bit[4:3] = 10b, 180° Bit[4:3] = 11b, 270°
		D[15:8]	1	0	0	n/a	n/a	n/a	PIP Layer Rotation Select		PIP Layer Color Depth			
PIP Layer Start Address 0	P1	60852	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PIP Layer Start Address Register 0
	P2	D[7:0]	1	0	0	PIP Layer Start Address								Bit[15:0] is Bit[15:0] of Main Layer Start Address ,but Bit[1:0] must be set to 00b
		D[15:8]	1	0	0	PIP Layer Start Address								
PIP Layer Start Address 1	P1	60854	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PIP Layer Start Address Register 1
	P2	D[7:0]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	Bit[2:0] is Bit[18:16] of Main Layer Start Address
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	PIP Layer Start Address			
PIP Layer Width	P1	60856	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PIP Layer Width Register
	P2	D[7:0]	1	0	0	PIP Layer Width								Bit[9:] = PIP Layer Horizontal Display Period in number of pixels PIP Layer Horizontal Display Period in number of pixels
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	PIP Layer Width		

Command	Para-meter	HEX	A0	/CS	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
PIP Layer Height	P1	60858	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PIP Layer Height Register
	P2	D[7:0]	1	0	0	PIP Layer Height								Bit[9:] = PIP Layer Vertical Display Period in number of lines
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	PIP Layer Height		
PIP Layer X Start Position	P1	6085A	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PIP Layer X Start Position Register
	P2	D[7:0]	1	0	0	PIP Layer X Start Position								These bits specify X start position of the PIP Layer on the panel, in lines
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	PIP Layer X Start Position		
PIP Layer Y Start Position	P1	6085C	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PIP Layer Y Start Position Register
	P2	D[7:0]	1	0	0	PIP Layer Y Start Position								These bits specify Y start position of the PIP Layer on the panel, in lines
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	PIP Layer Y Start Position		
PIP Enable	P1	60860	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PIP Enable Register
	P2	D[7:0]	1	0	0	n/a	n/a	n/a	n/a	Blink/ Fade Status (RO)	Blink/Fade Effect			Bit[2:0] = 000b, Blank Bit[2:0] = 001b, Normal Bit[2:0] = 010b, Blink 1 Bit[2:0] = 011b, Blink 2 Bit[2:0] = 100b, Fade Out Bit[2:0] = 101b, Fade In Bit[2:0] = 110b, Fade In/Out Continuous Bit[2:0] = 111b, Reserved Bit[3] = 0b, the PIP layer is not blinking or fading Bit[3] = 1b, the PIP layer is in the process of blinking or fading Bit[15:9] = blink/fade period in frames – 1
		D[15:8]	1	0	0	Blink/Fade Period							n/a	
Alpha Blending	P1	60862	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Alpha Blending Register
	P2	D[7:0]	1	0	0	n/a	Alpha Blending Ratio							Bit[6:0] = 0000000b,0000001b… …0111111b,1000000b : 64:0 (no PIP),63:1 … … 1:63,0:64(full PIP) ; 1000001b ~ 1111111b : Reserved Bit[9:8] = 00b, 1 Bit[9:8] = 01b, 2 Bit[9:8] = 10b, 4 Bit[9:8] = 11b, 8
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	Alpha Blending Step		
Transparency	P1	60864	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Transparency Register
	P2	D[7:0]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	Transparency Enable	Bit[0] = 0b, transparency is disabled Bit[0] = 1b, transparency is enabled
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
Transparency Key Color 0	P1	60866	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Transparency Key Color Register 0
	P2	D[7:0]	1	0	0	Key Color Blue								Bit[15:8] is Key Color Green bits [7:0] Bit[7:0] is Key Color Blue bits [7:0]
		D[15:8]	1	0	0	Key Color Green								
Transparency Key Color 1	P1	60868	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Transparency Key Color Register 1
	P2	D[7:0]	1	0	0	Key Color Red								Bit[7:0] is Key Color Red bits [7:0]
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
GPIO Configuration	P1	608D0	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								GPIO Configuration Register
	P2	D[7:0]	1	0	0	GPIO7 Config	GPIO6 Config	GPIO5 Config	GPIO4 Config	GPIO3 Config	GPIO2 Config	GPIO1 Config	GPIO0 Config	Bit[15:0] = 0b (default), the corresponding GPIO pin is configured as an input pin Bit[15:0] = 1b , the corresponding GPIO pin is configured as an output pin
		D[15:8]	1	0	0	GPIO15 Config	GPIO14 Config	GPIO13 Config	GPIO12 Config	GPIO11 Config	GPIO10 Config	GPIO9 Config	GPIO8 Config	
GPIO Status and Control	P1	608D2	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								GPIO Status and Control Register
	P2	D[7:0]	1	0	0	GPIO7 Status	GPIO6 Status	GPIO5 Status	GPIO4 Status	GPIO3 Status	GPIO2 Status	GPIO1 Status	GPIO0 Status	When GPIOx is configured as an output: Bit[15:0] = 0b, GPIOx low Bit[15:0] = 1b, GPIOx high
		D[15:8]	1	0	0	GPIO15 Status	GPIO14 Status	GPIO13 Status	GPIO12 Status	GPIO11 Status	GPIO10 Status	GPIO9 Status	GPIO8 Status	
GPIO Pull-Down Control	P1	608D4	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								GPIO Pull-Down Control Register
	P2	D[7:0]	1	0	0	GPIO7 Pull-down Control	GPIO6 Pull-down Control	GPIO5 Pull-down Control	GPIO4 Pull-down Control	GPIO3 Pull-down Control	GPIO 2 Pull-down Control	GPIO1 Pull-down Control	GPIO0 Pull-down Control	Bit[15:0] = 0b, the pull-down resistor for the associated GPIO pin is inactive. Bit[15:0] = 1b, the pull-down resistor for the associated GPIO pin is active.
		D[15:8]	1	0	0	GPIO15 Pull-down Control	GPIO14 Pull-down Control	GPIO13 Pull-down Control	GPIO12 Pull-down Control	GPIO11 Pull-down Control	GPIO10 Pull-down Control	GPIO9 Pull-down Control	GPIO8 Pull-down Control	

Note: Access of PLL Setting 0, PLL Setting 1, PLL Setting 2 and Internal Clock Configuration is only possible in Power Save Mode PSM0.

For more information and details please refer to S1D13L01 datasheet.

7. Precautions of using LCD Modules

Mounting

- For mounting use the holes arranged in the four corners of the LCD Module.
- Make sure to provide an even force on to LCD module. Uneven force (ex. twisted stress) should not be applied to the module. The casing on which a module is mounted should have sufficient strength to absorb any external force, so the force can't be transmitted directly to the module.
- It is suggested to attach a transparent protective plate to the surface of the module in order to protect the polarizer. It should have sufficient strength to resist external force.
- The housing should provide sufficient thermal radiation to satisfy the temperature specification.
- Acetic Acid type and Chlorine-type materials for the cover case are not desirable because the former generates corrosive gases, which may attack the polarizer at high temperatures which may cause circuit break by electro-chemical reactions.
- Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. Never treat the polarizer with chemical agents. Do not touch the surface of polarizer with bare hand or greasy cloth. Otherwise it may result in some cosmetics deterioration of the polarizer.
- When the surface becomes dusty, please wipe gently with absorbent cotton or another soft material. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer may affect the appearance.

Operating

- Spike noise may cause deterioration of the circuitry. Noise should be within a range of ±200mV. (Over and under voltage)
- The LCD response time is depends on the temperature. (At lower temperatures, it becomes slower)
- Brightness depends on the temperature as well. (At lower temperatures, it becomes less bright and it takes more time until the brightness is stable after power on).
- Try to avoid sudden temperature change, because they may cause condensation. Condensation may damage the polarizer or the circuitry. After fading condensation a smear or spot may occur.
- When fixed patterns are displayed for a long time, remnant images are likely to occur.
- The LCD module incorporates high frequency circuitry. Sufficient suppression of electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized interferences.

Electrostatic Discharge Control

- Since a module is composed of electronic circuits, it may be affected by electrostatic discharge.
- Make sure that the worker, who is assembling the module into equipment, is connected to ground through a ESD wrist band or insure other ESD protection.
- Avoid touching any electrical contact of the module without proper ESD protection.

Strong Light Exposure

- Strong light exposure causes degradation of polarizer and color filter.

Storage

- When storing modules as spares for a long time, precautions are necessary.
- Store the LCD modules in a dark place.
- Do not expose the module to sunlight or fluorescent light.
- Keep the temperature between 5°C and 35°C at normal humidity.
- The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

Protection Film

- When the protection film is peeled off, static electricity is generated between the film and polarizer. The film should be peeled off slowly and carefully by people who are electrically grounded. It is suggested to do that process while using an ion air blower or other suitable ESD equipment.
- The protection film is attached to the polarizer with a small amount of glue. If some stress is applied e.g. by rubbing the protection film against the polarizer during the time it is peeled off, some protection film may remain on top of the polarizer. Please carefully peel off the remaining protection film without rubbing it against the polarizer.
- When the module, with protection film attached, is stored for a long time, some very small amount of glue may remain still on the polarizer after the protection film is peeled off. You can remove the glue easily. In such a case please wipe them off with absorbent cotton or another soft material.

Transportation

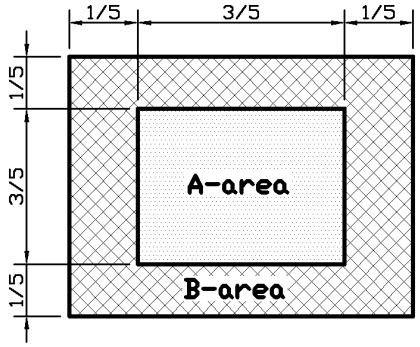
The LCD modules should not be exposed to drop, shock, excessive pressure, water or sunshine during transportation.

Appendix A Inspection items and criteria for appearance defects

Items	Criteria			
Open Segment or Common	Not permitted			
Short	Not permitted			
Wrong Viewing Angle	Not permitted			
Decliners	Not permitted			
Contrast Ration Uneven	According to the limit specimen			
Crosstalk	According to the limit specimen			
White spots	X>1 pixel	A-area	Not permitted	Max 6 spots allowed
		B-area	Max. 1 allowed	
	1/2 pixel<X≤1 pixel	A-area	Not permitted	
		B-area	Max. 2 allowed	
	X≤1/2 pixel	A-area	Max. 1 allowed	
		B-area	Max. 4 allowed	
Black Sport	X>1 pixel	A-area	Not permitted	
		B-area	Max. 2 allowed	
	X≤1/2 pixel	A-area	Max. 1 allowed	
		B-area	Max. 4 allowed	
Line Defect	Apparent vertical horizontal line defects are not permitted			

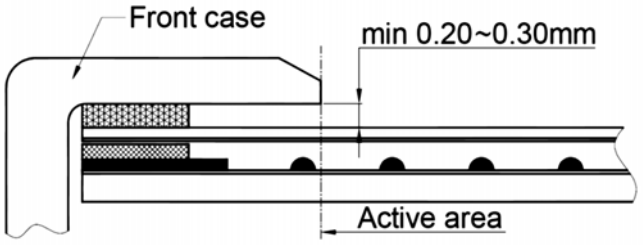
Notes:

4. *On Pixel includes 3 dots (RedDot + GreenDot + BlueDot)*
5. *Definition of Panel "A-area" and "B-area"*

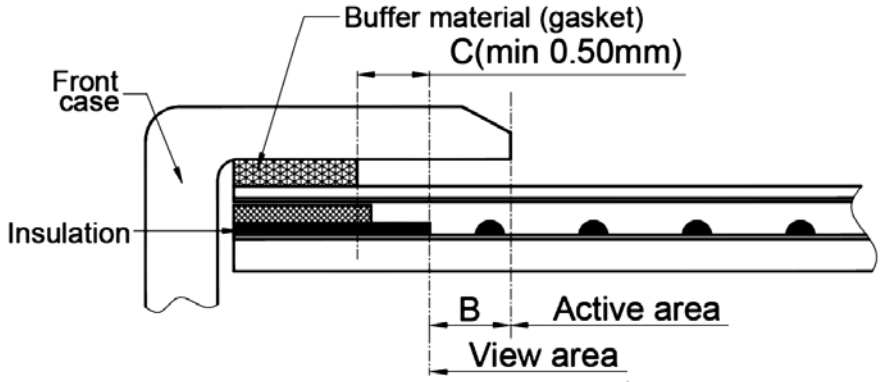


附录：Touch panel Design Precautions

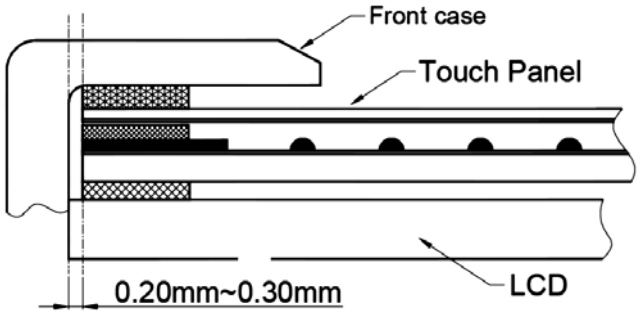
1. It should prevent front case touching the touch panel Active Area (A.A.) to prevent abnormal touch.
   It should left gab (e.g. 0.2~0.3mm) in between.



2. Outer case design should take care about the area outside the A.A.
   Those areas contain circuit wires which is having different thickness. Touching those areas could deform the ITO film. As a result case the ITO cold be damaged and shorten its lifetime.
   It is suggested to protect those areas with gasket (between the front case and the touch panel).
   The suggested figures are B≥0.50mm; C≥0.50mm。



3. The front case side wall should keep space (e.g. 0.2 ~ 0.3mm) from the touch panel.



4. In general design,
   touch panel V.A. should be bigger than the LCD V.A.
   and touch panel A.A. should be bigger than the LCD A.A.