MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

LMT339, LMT2901

ADVANCE INFORMATION

QUAD SINGLE SUPPLY COMPARATORS

QUAD COMPARATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

These comparators are designed for use in level detection, low level sensing and memory applications in Consumer Automotive and Industrial electronic applications.

- Single or Split Supply Operation
- Low Input Bias Current — 25 nA (Typ)
- Low Input Offset Current — ±5.0 nA (Typ)
- Low Input Offset Voltage — ±2.0 mV (Typ)
- Input Common-Mode Voltage Range to Ground
- Low Output Saturation Voltage — 130 mV (Typ) @ 4.0 mA
- TTL and CMOS Compatible

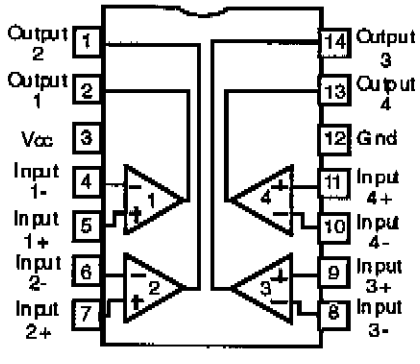
N SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
SO-14

MAXIMUM RATINGS (TA= 25°C Unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 36 ±18	Vdc
Input Differential Voltage Range	V_{IDR}	Vcc	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to 36	Vdc
Output Short Circuit Duration	t_S	Continuous	Sec
Power Dissipation, Plastic DIP	P_D	1.0	W
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

PIN CONNECTIONS



ORDERING INFORMATION		
Device	Package	Temperature Range
LMT339N LMT339D	8 Pin Plastic DIP SO-8	0°C to 70°C
LMT2901N LMT2901D	8 Pin Plastic DIP SO-8	-40°C to 105°C

CAUTION: These devices do not have internal ESD protection circuitry and are rated as CLASS 1 devices per the ESD test method in Mil-Std-883D. They should be handled using standard ESD prevention methods to avoid damage to the device.

MacRev 3.0

ELECTRICAL CHARACTERISTICS (V_{CC}= +5.0V, V_{EE}= Ground, T_A=25°C unless otherwise noted)

CHARACTERISTICS	SYMBOL	LMT339			LMT2901			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Note 4)	V_{IO}	—	±2.0	±5.0	—	±2.0	±7.0	mVdc
Input Offset Current (Note 4)	I_{IO}	—	±5.0	±50	—	±5.0	±50	nA
Input Bias Current (Note 4, 5) (Output in Linear Range)	I_{IB}	—	25	250	—	25	250	nA
Input Common-Mode Voltage Range	V_{ICR}	0	—	V_{CC} -1.5	0	—	V_{CC} -1.5	V
Voltage Gain $R_L \geq 15$ kΩ, V_{CC} = 15 Vdc	A_V	—	200	—	25	100	—	V/mV
Large Signal Response Time V_I = TTL Logic Swing, V_{ref} =1.4 Vdc, V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	—	—	300	—	—	300	—	ns
Response Time (Note 6) V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	—	—	1.3	—	—	1.3	—	µs
Output Sink Current V_I (-) ≥ + 1.0 Vdc, V_I (+) = 0, $V_O \leq$ 1.5 Vdc	I_{sink}	6.0	16	—	6.0	16	—	mA
Saturation Voltage V_I (-) ≥ +1.0 Vdc, V_I (+) = 0, $I_{sink} \leq$ 4.0 mA	V_{sat}	—	200	400	—	200	400	mV
Output Leakage Current V_I (+) ≥ +1.0 Vdc, V_I (-) = 0, V_O = +5.0 Vdc	I_{OL}	—	0.1	—	—	0.1	—	nA
Supply Current R_L = ∞ (For All Comparators)	I_{CC}	—	0.8	2.0	—	0.8	2.0	mA

PERFORMANCE CHARACTERISTICS (V_{CC}= +5.0V, V_{EE}= Ground, T_A=T_{LOW} to T_{HIGH})

CHARACTERISTICS	SYMBOL	LMT339			LMT2901			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	—	—	±9.0	—	—	±15	mVdc
Input Offset Current	I_{IO}	—	—	±150	—	—	±200	nA
Input Bias Current (Note 5) (Output in Linear Range)	I_{IB}	—	25	400	—	25	500	nA
Input Common-Mode Voltage Range	V_{ICR}	0	—	V_{CC} -2.0	0	—	V_{CC} -2.0	V
Saturation Voltage V_I (-) ≥ +1.0 Vdc, V_I (+) = 0, $I_{sink} \leq$ 4.0 mA	V_{sat}	—	—	700	—	—	700	mV
Output Leakage Current V_I (+) ≥ +1.0 Vdc, V_I (-) = 0, V_O = 30 Vdc	I_{OL}	—	—	1.0	—	—	1.0	µA
Differential Input Voltage All $V_I \geq$ 0 Vdc	V_{ID}	—	—	V_{CC}	—	—	V_{CC}	mA

NOTES:

1. T_{LOW} = 0°C, T_{HIGH} = +70°C (for LMT339)
   T_{LOW} = -40°C, T_{HIGH} = +105°C (for LMT2901)
2. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}. Output short circuits to V_{CC} can cause excessive heating and eventual destruction.
3. This magnitude of input current will only occur if the leaks are driven more negative than ground or the negative supply voltage. This is due to the PNP collectorbase junction becoming forward biased, acting as an input clamp diode. There is also a lateral PNP parasitic transistor action which can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time that an input is driven negative. This will not destroy the device when limited to the max rating and normal output states will recover when the inputs become ≥ ground or negative supply.
4. At the output switch point, $V_O \approx$ 1.4 Vdc, $R_S \leq$ 100 Ω, 5.0 Vdc ≤ V_{CC} ≤ 30 Vdc, with the inputs over the full common-mode range (0 Vdc to V_{CC} - 1.5 Vdc).
5. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
6. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.

This data sheet contains preliminary information and design objective. All specifications are subject to change without notice.