National Semiconductor

LMV1090

PRELIMINARY
July 1, 2009

Dual Input, Far Field Noise Suppression Microphone Amplifier

General Description

The LMV1090 is a fully analog dual differential input, differential output, microphone array amplifier designed to reduce background acoustic noise, while delivering superb speech clarity in voice communication applications.

The LMV1090 preserves near-field voice signals within 4cm of the microphones while rejecting far-field acoustic noise greater than 50cm from the microphones. Up to 20dB of far-field rejection is possible in a properly configured and using ±0.5dB matched micropohones.

Part of the Powerwise™ family of energy efficient solutions, the LMV1090 consumes only 600µA of supply current providing superior performance over DSP solutions consuming greater than ten times the power.

The dual microphone inputs and the processed signal output are differential to provide excellent noise immunity. The microphones are biased with an internal low-noise bias supply.

Key Specifications

- Far Field Noise Suppression Electrical * 34dB (typ)
- $SNRI_E$ 26dB (typ)
- Supply current 600µA (typ)
- Standby current 0.1µA (typ)
- Signal-to-Noise Ratio (Voice band) 65dB (typ)
- Total Harmonic Distortion + Noise 0.1% (typ)
- PSRR (217Hz) 99dB (typ)

*$FFNS_E$ at f = 1kHz

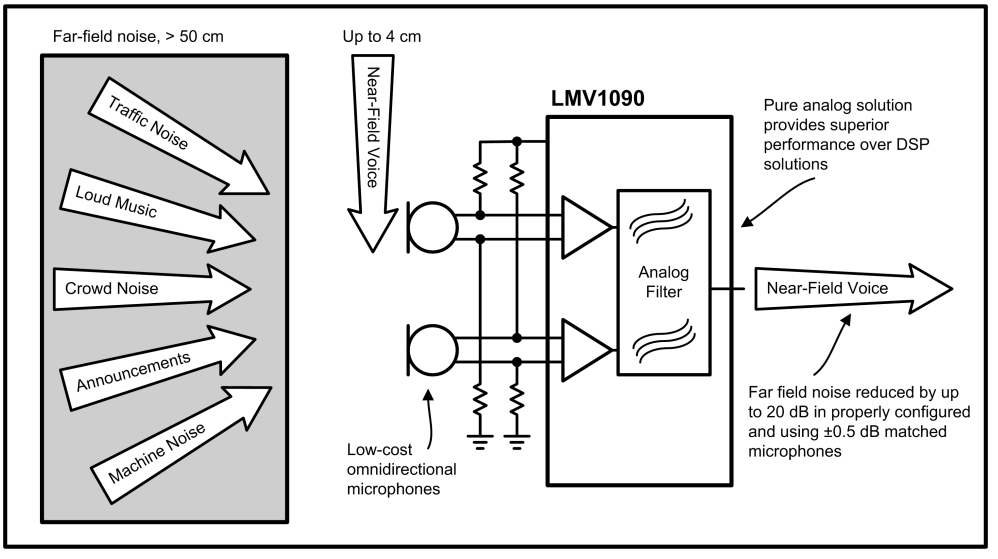
Features

- No loss of voice intelligibility
- No added processing delay
- Low power consumption
- Differential outputs
- Excellent RF immunity
- Adjustable 12 - 54dB gain
- Shutdown function
- Space-saving 16–bump micro SMD package

Applications

- Mobile headset
- Mobile and handheld two-way radios
- Bluetooth and other powered headsets
- Hand-held voice microphones
- Cell phones

System Diagram



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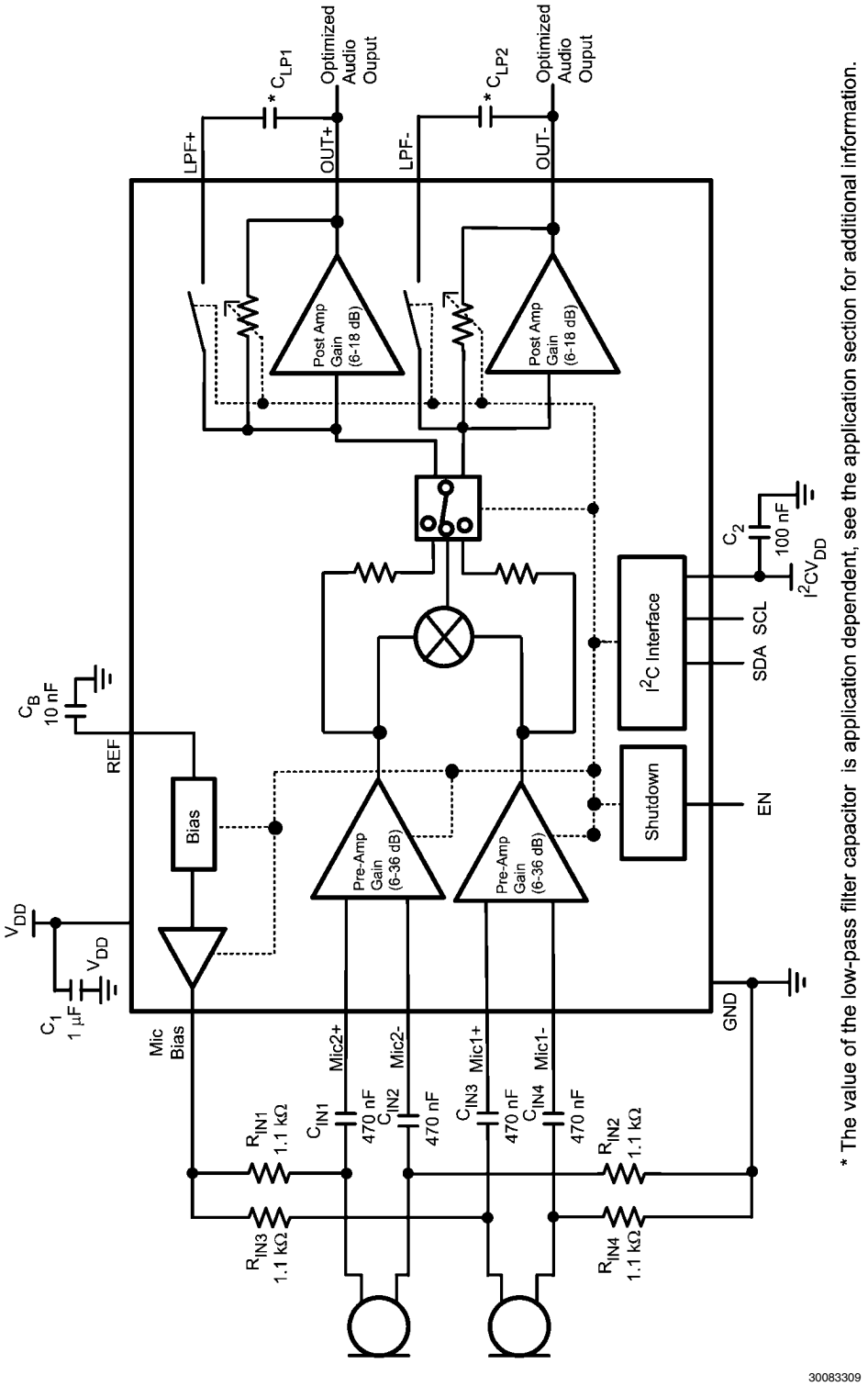
Typical Application

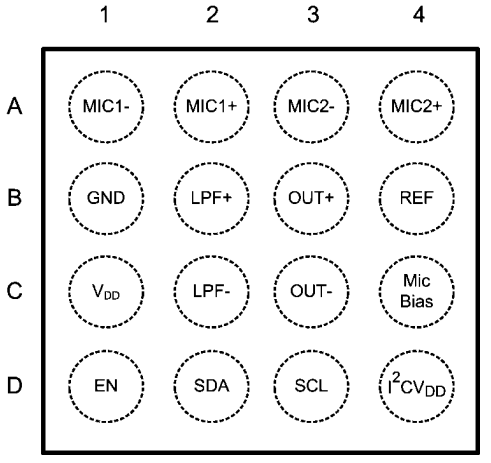


* The value of the low-pass filter capacitor is application dependent, see the application section for additional information.

FIGURE 1. Typical Dual Microphone Far Field noise Cancelling Application

Connection Diagrams

16–Bump micro SMD package



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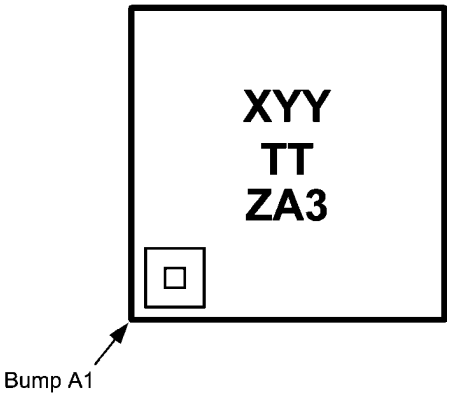
Top View
Order Number LMV1090TL
See NS Package Number TLA1611A

16–Bump micro SMD Marking



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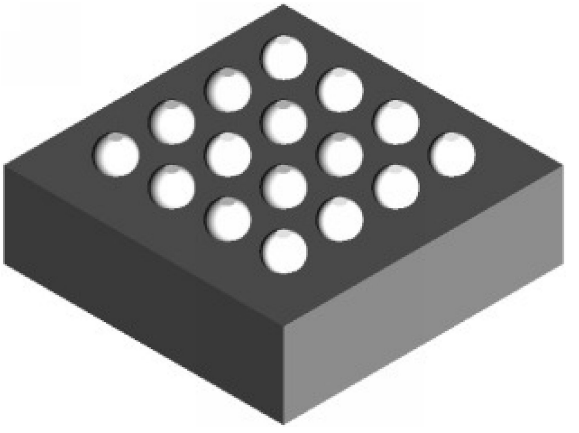
Top View
X = Plant Code
YY = Date Code
TT = Die Traceability
ZA3 = LMV1090TL

micro SMD Package View



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Bottom View

Ordering Information

Order Number	Package	Package Drawing Number	Device Marking	Transport Media
LMV1090TL	16 Bump µSMD	TLA1611A	XYTTZA3	250 units on tape and reel
LMV1090TLX	16 Bump µSMD	TLA1611A	XYTTZA3	1000 units on tape and reel

TABLE 1. Pin Name and Function

Bump Number	Pin Name	Pin Function	Pin Type
A1	MIC1–	Microphone 1 negative input	Analog Input
A2	MIC1+	Microphone 1 positive input	Analog Input
A3	MIC2–	Microphone 2 negative input	Analog Input
A4	MIC2+	Microphone 2 positive input	Analog Input
B1	GND	Amplifier ground	Ground
B2	LPF+	Low Pass Filter for positive output	Analog Input
B3	OUT+	Positive optimized audio output	Analog Output
B4	REF	Reference voltage de-coupling	Analog Reference
C1	V_{DD}	Power supply	Supply
C2	LPF-	Low Pass Filter for negative output	Analog Input
C3	OUT-	Negative optimized audio output	Analog Output
C4	Mic Bias	Microphone Bias	Analog Output
D1	EN	Chip enable	Digital input
D2	SDA	I^2C data	Digital Input/Output
D3	SCL	I^2C clock	Digital Input
D4	I^2CV_{DD}	I^2C power supply	Supply

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	-85°C to +150°C
Power Dissipation (Note 3)	Internally Limited
ESD Rating (Note 4)	2000V
ESD Rating (Note 5)	200V
CDM	500V
Junction Temperature (T_{JMAX})	150°C
Mounting Temperature	235°C
Infrared or Convection (20 sec.)	

Thermal Resistance

θ_{JA} (microSMD)	70°C/W

Soldering Information See AN-112 “microSMD Wafers Level Chip Scale Package.”

Operating Ratings (Note 1)

Supply Voltage	$2.7V \le V_{DD} \le 5.5V$
I^2CV_{DD} Supply Voltage (Note 8)	$1.7V \le I^2CV_{DD} \le 5.5V$
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$

Electrical Characteristics 3.3V (Notes 1, 2)

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V_{DD} = 3.3V, V_{IN} = 18mV_{P-P}, f = 1kHz, EN = V_{DD}, Pre Amp gain = 20dB, Post Amp gain = 6dB, R_L = 100kΩ, and C_L = 4.7pF, f = 1kHz pass through mode.

Symbol	Parameter	Conditions	LMV1090 Typical (Note 6)	LMV1090 Limit (Note 7)	Units (Limits)
SNR	Signal-to-Noise Ratio	V_{IN} = 18mV_{P-P} A-weighted, Audio band	63		dB
		V_{OUT} = 18V_{P-P}, A-Weighted voice band (300–3400Hz)	65		dB
e_N	Input Referred Noise level	A-Weighted	5		μV_{RMS}
V_{IN}	Maximum Input Signal	THD+N < 1%, Pre Amp Gain = 6dB	880	820	mV_{P-P} (min)
V_{OUT}	Maximum AC Output Voltage	Differential Out+, Out- THD+N < 1%	1.2	1.1	V_{RMS} (min)
	DC Level at Outputs	Out+, Out-	820		mV
THD+N	Total Harmonic Distortion + Noise	Differential Out+ and Out-	0.1	0.2	% (max)
Z_{IN}	Input Impedance		142	110 220	kΩ (min) kΩ (max)
Z_{OUT}	Output Impedance (Differential)		220		Ω
Z_{LOAD}	Load Impedance (Out+, Out-) (Note 10)	R_{LOAD} C_{LOAD}		10 100	kΩ (min) pF (max)
A_M	Microphone Preamplifier Gain Range	minimum maximum	6 36		dB dB
A_{MR}	Microphone Preamplifier Gain Adjustment Resolution		2	1.7 2.3	dB (min) dB (max)
A_P	Post Amplifier Gain Range	minimum maximum	6 18		dB dB
A_{PR}	Post Amplifier Gain Resolution		3	2.6 3.4	dB (min) dB (max)
$FFNS_E$	Far Field Noise Suppression Electrical	f = 1kHz (See Test Method) f = 300Hz (See Test Method)	34 42	26	dB dB
$SNRI_E$	Signal-to-Noise Ratio Improvement Electrical	f = 1kHz (See Test Method) f = 300Hz (See Test Method)	26 33	18	dB dB
PSRR	Power Supply Rejection Ratio	Input Referred, Input AC grounded			
		f_{RIPPLE} = 217Hz (V_{RIPPLE} = 100mV_{P-P})	99	85	dB (min)
		f_{RIPPLE} = 1kHz (V_{RIPPLE} = 100mV_{P-P})	95	80	dB (min)
CMRR	Common Mode Rejection Ratio	input referred	60		dB
V_{BM}	Microphone Bias Supply Voltage	I_{BIAS} = 1.2mA	2.0	1.85 2.15	V (min) V (max)

e_{VBM}	Mic bias noise voltage on V_{REF} pin	A-Weighted, C_B = 10nF	7		μV_{RMS}
I_{DDQ}	Supply Quiescent Current	V_{IN} = 0V	0.60	0.80	mA (max)
I_{DD}	Supply Current	V_{IN} = 25mV$_{P-P}$ both inputs Noise cancelling mode	0.60		mA
I_{SD}	Shut Down Current	EN pin = GND	0.1	0.7	µA (max)
$I_{DD}I^2C$	I²C supply current	I²C Idle Mode	25	100	nA (max)
T_{ON}	Turn-On Time			40	ms (max)
T_{OFF}	Turn-Off Time			60	ms (max)

Electrical Characteristics 5.0V (Notes 1, 8)

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V_{DD} = 5V, V_{IN} = 18mV$_{P-P}$, EN = V_{DD}, Pre Amp gain = 20dB, Post Amp gain = 6dB, R_L = 100kΩ, and C_L = 4.7pF, f = 1kHz pass through mode.

Symbol	Parameter	Conditions	LMV1090		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
SNR	Signal-to-Noise Ratio	V_{IN} = 18mV$_{P-P}$ A-weighted, Audio band	63		dB
		V_{OUT} = 18mV$_{P-P}$, A-weighted voice band (300–3400Hz)	65		dB
e_N	Input Referred Noise level	A-Weighted	5		μV_{RMS}
V_{IN}	Maximum Input Signal	THD+N < 1%	880	820	mV$_{P-P}$ (min)
V_{OUT}	Maximum AC Output Voltage	f = 1kHz, THD+N < 1% between differential output	1.2	1.1	V_{RMS} (min)
	DC Output Voltage		820		mV
THD+N	Total Harmonic Distortion + Noise	Differential Out+ and Out-	0.1	0.2	% (max)
Z_{IN}	Input Impedance		142	110 220	kΩ (min) kΩ (max)
Z_{OUT}	Output Impedance		220		Ω
A_M	Microphone Preamplifier Gain Range	minimum maximum	6 36		dB dB
A_{MR}	Microphone Preamplifier Gain Adjustment Resolution		2	1.7 2.3	dB (min) dB (max)
A_P	Post Amplifier Gain Range	minimum maximum	6 18		dB dB
A_{PR}	Post Amplifier Gain Adjustment Resolution		3	2.6 3.4	dB (min) dB (max)
$FFNS_E$	Far Field Noise Suppression Electrical	f = 1kHz (See Test Method) f = 300Hz (See Test Method)	34 42	26	dB dB
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PSRR	Power Supply Rejection Ratio	Input Referred, Input AC grounded			
		f_{RIPPLE} = 217Hz (V_{RIPPLE} = 100mV$_{P-P}$)	99	85	dB (min)
		f_{RIPPLE} = 1kHz (V_{RIPPLE} = 100mV$_{P-P}$)	95	80	dB (min)
CMRR	Common Mode Rejection Ratio	input referred	60		dB
V_{BM}	Microphone Bias Supply Voltage	I_{BIAS} = 1.2mA	2.0	1.85 2.15	V (min) V (max)
e_{VBM}	Microphone bias noise voltage on V_{REF} pin	A-Weighted, C_B = 10nF	7		μV_{RMS}
I_{DDQ}	Supply Quiescent Current	V_{IN} = 0V	0.60	0.80	mA (max)
I_{DD}	Supply Current	V_{IN} = 25mV$_{P-P}$ both inputs Noise cancelling mode	0.60		mA
I_{SD}	Shut Down Current	EN pin = GND	0.1		µA

Symbol	Parameter	Conditions	LMV1090		Units (Limits)
			Typical	Limit	
$I_{DD}I^2C$	I²C supply current	I²C Idle Mode	25	100	nA (max)
T_{ON}	Turn On Time			40	mA (max)
T_{OFF}	Turn Off Time			60	ms (max)

Digital Interface Characteristics I²C_V_{DD} = 2.2V to 5.5V (Notes 2, 8)

The following specifications apply for V_{DD} = 5.0V and 3.3V, T_A = 25°C, 2.2V ≤ I²C_V_{DD} ≤ 5.5V, unless otherwise specified.

Symbol	Parameter	Conditions	LMV1090		Units (Limits)
			Typical (Note 4)	Limits (Notes 5, 7)	
t_1	I²C Clock Period			2.5	µs (min)
t_2	I²C Data Setup Time			100	ns (min)
t_3	I²C Data Stable Time			0	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)
t_6	I²C Data Hold Time			100	ns (min)
V_{IH}	I²C Input Voltage High	EN, SCL, SDA		0.7xI²CV_{DD}	V (min)
V_{IL}	I²C Input Voltage Low	EN, SCL, SDA		0.3xI²CV_{DD}	V (max)

Digital Interface Characteristics I²C_V_{DD} = 1.7V to 2.2V

The following specifications apply for V_{DD} = 5.0V and 3.3V, T_A = 25°C, 1.7V ≤ I²C_V_{DD} ≤ 2.2V, unless otherwise specified.

Symbol	Parameter	Conditions	LMV1090		Units (Limits)
			Typical (Note 6)	Limits (Note 7)	
t_1	I²C Clock Period			2.5	µs (min)
t_2	I²C Data Setup Time			250	ns (min)
t_3	I²C Data Stable Time			0	ns (min)
t_4	Start Condition Time			250	ns (min)
t_5	Stop Condition Time			250	ns (min)
t_6	I²C Data Hold Time			250	ns (min)
V_{IH}	I²C Input Voltage High	EN, SCL, SDA		0.7xI²CV_{DD}	V (min)
V_{IL}	I²C Input Voltage Low	EN, SCL, SDA		0.3xI²CV_{DD}	V (max)

Note 1: "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum* Ratings or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: *The Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: The maximum power dissipation must be de-rated at elevated temperatures and is dictated by T_{JMAX}, θ_{JC}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in the *Absolute Maximum Ratings*, whichever is lower. For the LMV1090, T_{JMAX} = 150°C and the typical θJA for this microSMD package is 70°C/W and for the LLP package θ_{JA} is 64°C/W Refer to the Thermal Considerations section for more information.

Note 4: Human body model, applicable std. JESD22-A114C.

Note 5: Machine model, applicable std. JESD22-A115-A.

Note 6: Typical values represent most likely parametric norms at T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 7: Datasheet min/max specification limits are guaranteed by test, or statistical analysis.

Note 8: The voltage at I²CV_{DD} must not exceed the voltage on V_{DD}.

Note 9: Default value used for performance measurements.

Note 10: Guaranteed by design.

Test Methods

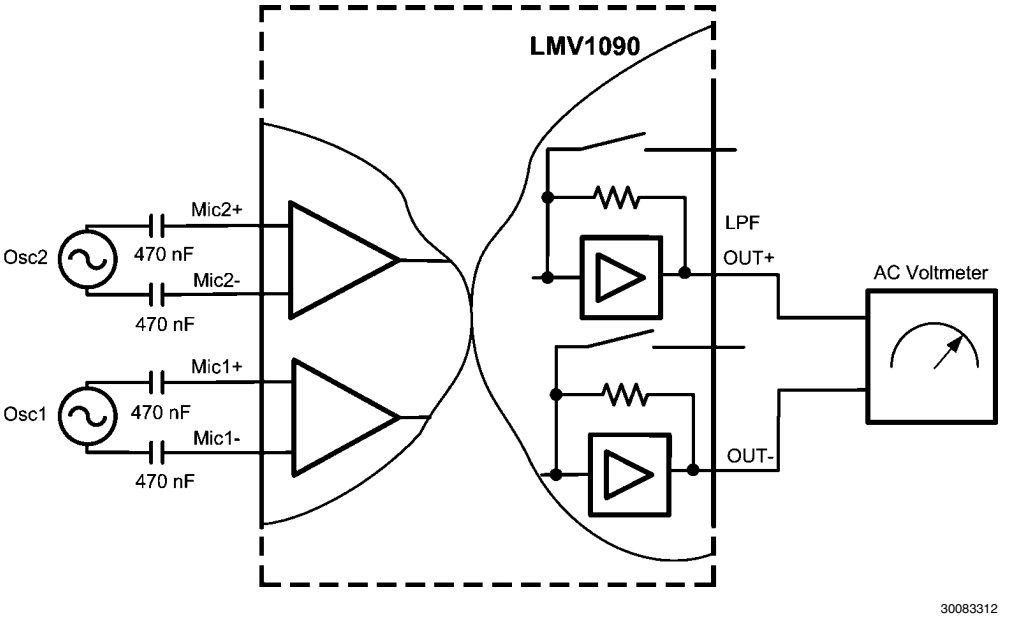


FIGURE 2. $FFNS_E$, $NFSL_E$, $SNRI_E$ Test Circuit

FAR FIELD NOISE SUPPRESSION ($FFNS_E$)

For optimum noise suppression the far field noise should be in a broadside array configuration from the two microphones (see Figure 8). Which means the far field sound source is equidistance from the two microphones. This configuration allows the amplitude of the far field signal to be equal at the two microphone inputs, however a slight phase difference may still exist. To simulate a real world application a slight phase delay was added to the $FFNS_E$ test. The block diagram from Figure 3 is used with the following procedure to measure the $FFNS_E$.

1. A sine wave with equal frequency and amplitude ($25mV_{P-P}$) is applied to Mic1 and Mic2. Using a signal generator, the phase of Mic 2 is delayed by 1.1° when compared with Mic1.
2. Measure the output level in dBV (X)
3. Mute the signal from Mic2
4. Measure the output level in dBV (Y)
5. $FFNS_E$ = Y - X dB

NEAR FIELD SPEECH LOSS ($NFSL_E$)

For optimum near field speech preservation, the sound source should be in an endfire array configuration from the two microphones (see Figure 9). In this configuration the speech signal at the microphone closest to the sound source will have greater amplitude than the microphone further away. Additionally the signal at microphone further away will experience a phase lag when compared with the closer microphone. To simulate this, phase delay as well as amplitude shift was added to the $NFSL_E$ test. The schematic from Figure 3 is used with the following procedure to measure the $NFSL_E$.

1. A $25mV_{P-P}$ and $17.25mV_{P-P}$ ($0.69*25mV_{P-P}$) sine wave is applied to Mic1 and Mic2 respectively. Once again, a signal generator is used to delay the phase of Mic2 by 15.9° when compared with Mic1.
2. Measure the output level in dBV (X)
3. Mute the signal from Mic2
4. Measure the output level in dBV (Y)
5. $NFSL_E$ = Y - X dB

SIGNAL TO NOISE RATIO IMPROVEMENT ELECTRICAL ($SNRI_E$)

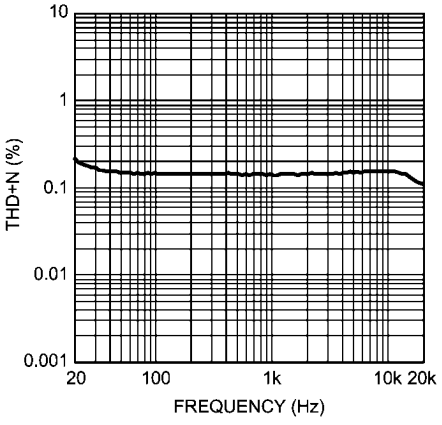
The $SNRI_E$ is the ratio of $FFNS_E$ to $NFSL_E$ and is defined as:

$$SNRI_E = FFNS_E - NFSL_E$$

Typical Performance Characteristics

Unless otherwise specified, T_J = 25°C, V_{DD} = 3.3V, Input Voltage = 18mV_{P-P}, f =1 kHz, pass through mode (Note 8), Pre Amp gain = 20dB, Post Amp gain = 6dB, R_L = 100kΩ, and C_L = 4.7pF.

THD+N vs Frequency
Mic1 = AC GND, Mic2 = 36mV_{P-P}
Noise Canceling Mode



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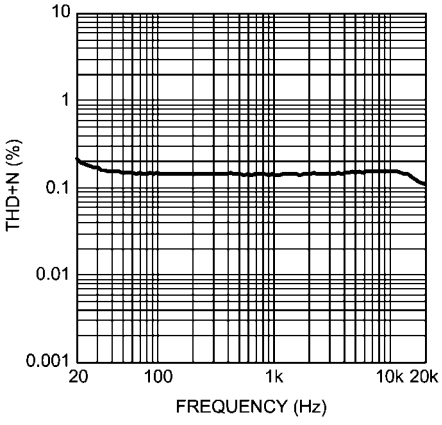
THD+N vs Frequency
Mic2 = AC GND, Mic1 = 36mV_{P-P}
Noise Canceling Mode



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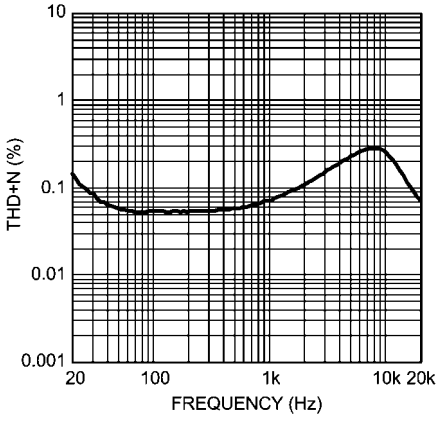
THD+N vs Frequency
Mic1 = 36mV_{P-P}
Mic1 Pass Through Mode



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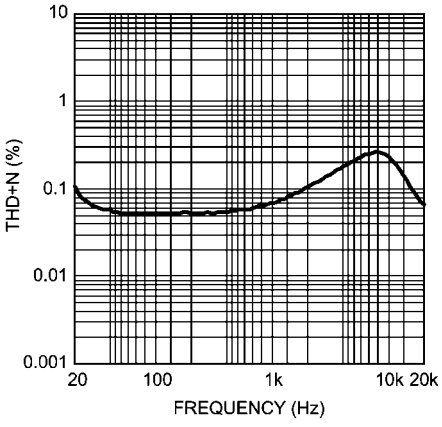
THD+N vs Frequency
Mic2 = 36mV_{P-P}
Mic2 Pass Through Mode



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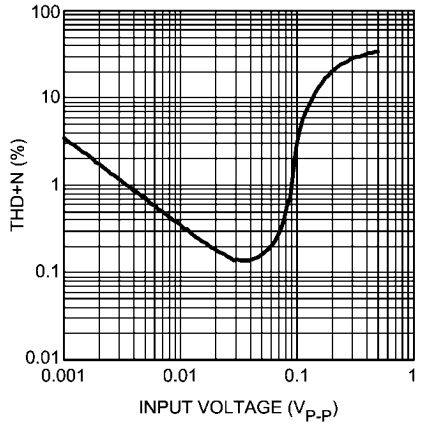
THD+N vs Input Voltage
Mic1 = AC GND, f = 1kHz
Mic2 Noise Canceling Mode



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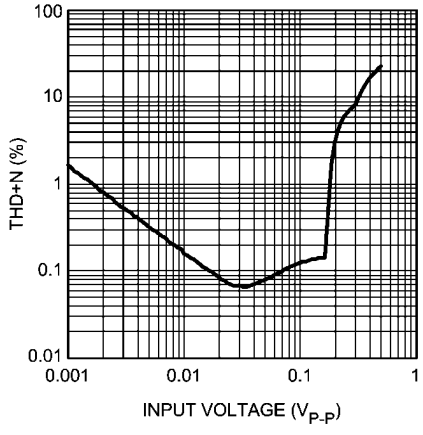
THD+N vs Input Voltage
Mic2 = AC GND, f = 1kHz
Mic1 Noise Canceling Mode



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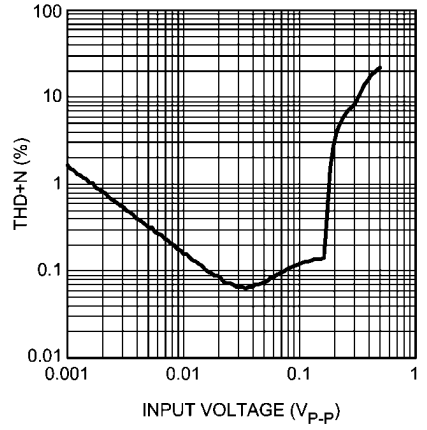
THD+N vs Input Voltage
f = 1kHz
Mic1 Pass Through Mode



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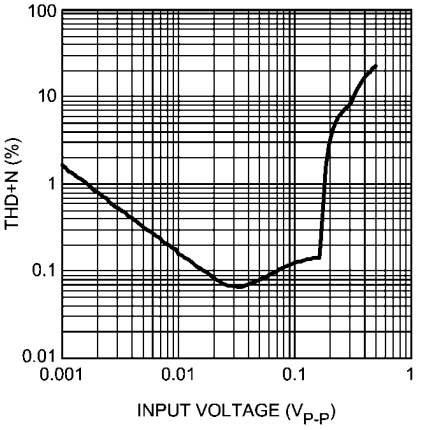
THD+N vs Input Voltage
f = 1kHz
Mic2 Pass Through Mode



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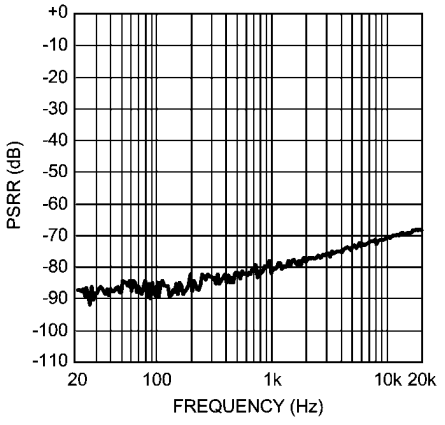
PSRR vs Frequency
Pre Amp Gain = 20dB, Post Amp Gain = 6dB
V_{RIPPLE} = 100mV_{P-P}, Mic1 = Mic2 = AC GND
Mic1 Pass Through Mode



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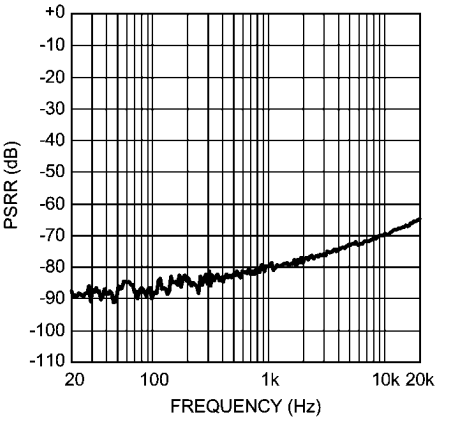
PSRR vs Frequency
Pre Amp Gain = 20dB, Post Amp Gain = 6dB
V_{RIPPLE} = 100mV_{P-P}, Mic1 = Mic2 = AC GND
Mic2 Pass Through Mode



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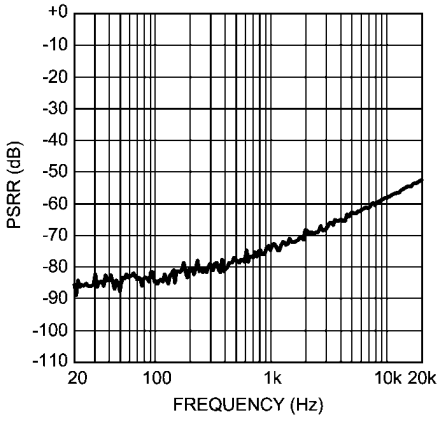
PSRR vs Frequency
Pre Amp Gain = 20dB, Post Amp Gain = 6dB
V_{RIPPLE} = 100mV_{P-P}, Mic1 = Mic2 = AC GND
Noise Canceling Mode



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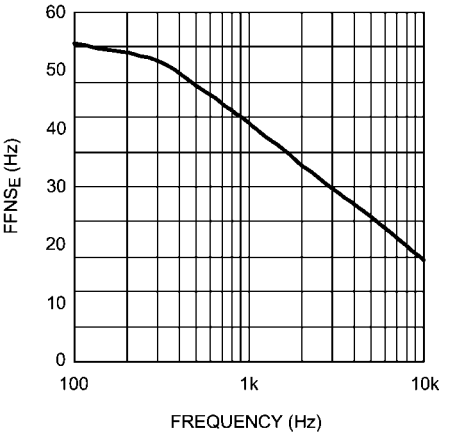
Far Field Noise Suppression Electrical vs Frequency



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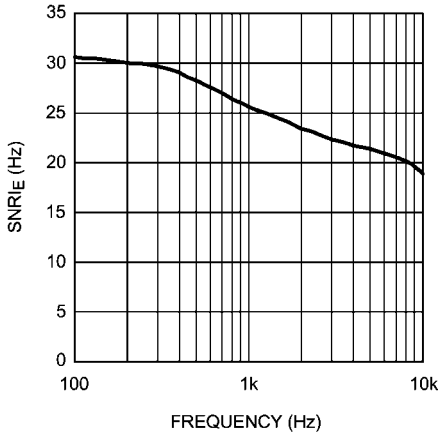
Signal-to-Noise Ratio Electrical vs Frequency



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Application Data

INTRODUCTION

The LMV1090 is a fully analog single chip solution to reduce the far field noise picked up by microphones in a communication system. A simplified block diagram is provided in *Figure 3*.

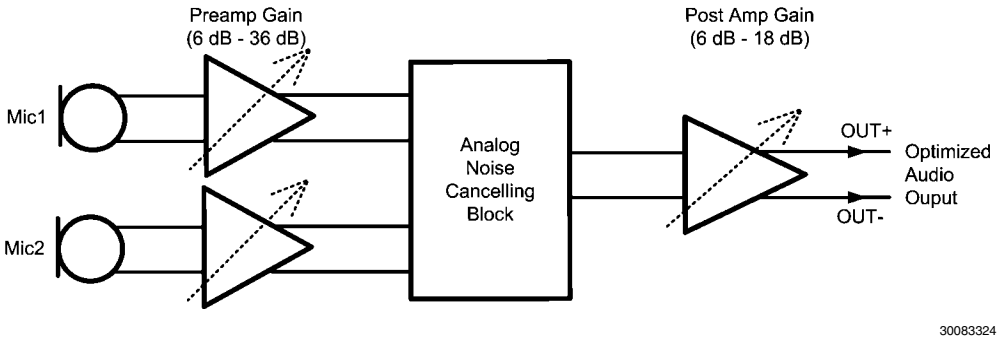


FIGURE 3. Simplified Block Diagram of the LMV1090

The output signal of the microphones is amplified by a preamplifier with adjustable gain between 6dB and 36dB. After the signals are matched the analog noise cancelling suppresses the far field noise signal. The output of the analog noise cancelling processor is amplified in the post amplifier with adjustable gain between 6dB and 18dB. For optimum noise and EMI immunity, the microphones have a differential connection to the LMV1090 and the output of the LMV1090 is also differential. The adjustable gain functions can be controlled via I²C.

Power Supply Circuits

A low drop-out (LDO) voltage regulator in the LMV1090 allows the device to be independent of supply voltage variations.

The Power On Reset (POR) circuitry in the LMV1090 requires the supply voltage to rise from 0V to V_{DD} in less than 100ms.

The Mic Bias output is provided as a low noise supply source for the electret microphones. The noise voltage on the Mic Bias microphone supply output pin depends on the noise voltage on the internal the reference node. The de-coupling capacitor on the V_{REF} pin determines the noise voltage on this internal reference. This capacitor should be larger than 1nF; having a larger capacitor value will result in a lower noise voltage on the Mic Bias output.

Most of the logic levels for the digital control interface are relative to I^2CV_{DD} voltage. This eases interfacing to the micro controller of the application containing the LMV1090. The supply voltage on the I^2CV_{DD} pin must never exceed the voltage on the V_{DD} pin.

Only the four pins that determine the default power up gain have logic levels relative to V_{DD}.

Shutdown Function

As part of the Powerwise™ family, the LMV1090 consumes only 0.50mA of current. In many applications the part does not need to be continuously operational. To further reduce the power consumption in the inactive period, the LMV1090 provides two individual microphone power down functions. When either one of the shutdown functions is activated the part will go into shutdown mode consuming only a few µA of supply current.

SHUTDOWN VIA HARDWARE PIN

The hardware shutdown function is operated via the EN pin. In normal operation the EN pin must be at a 'high' level (V_{DD}). Whenever a 'low' level (GND) is applied to the EN pin the part will go into shutdown mode disabling all internal circuits.

Gain Balance and Gain Budget

In systems where input signals have a high dynamic range, critical noise levels or where the dynamic range of the output voltage is also limited, careful gain balancing is essential for the best performance. Too low of a gain setting in the preamplifier can result in higher noise levels while too high of a gain setting in the preamplifier will result in clipping and saturation in the noise cancelling processor and output stages.

The gain ranges and maximum signal levels for the different functional blocks are shown in *Figure 4*. Two examples are given as a guideline on how to select proper gain settings.

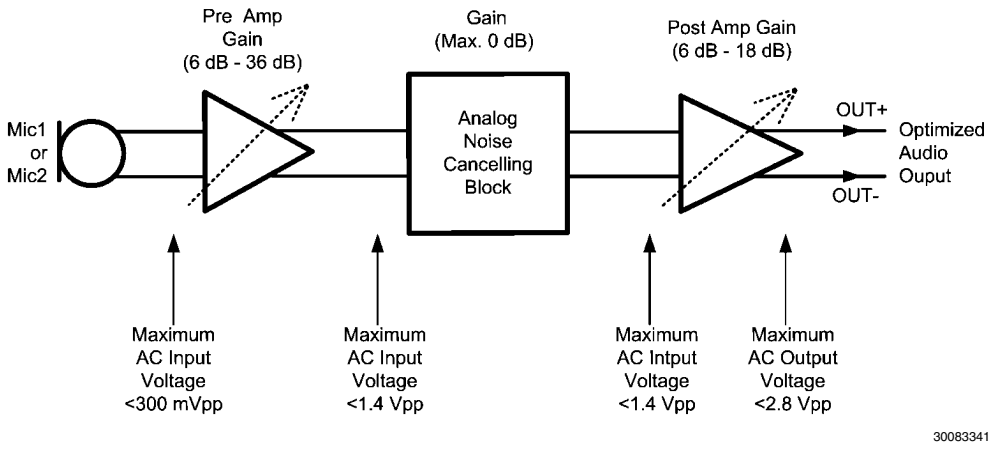


FIGURE 4. Maximum Signal Levels

Example 1

An application using microphones with $50mV_{P-P}$ maximum output voltage, and a baseband chip after the LMV1090 with $1.5V_{P-P}$ maximum input voltage.

For optimum noise performance, the gain of the input stage should be set to the maximum.

1. $50mV_{P-P}$ +36 dB = $3.1V_{P-P}$.
2. $3.1V_{P-P}$ is higher than the maximum $1.4V_{P-P}$ allowed for the Noise Cancelling Processor (NCP). This means a gain lower than 28.9dB should be selected.
3. Select the nearest lower gain from the gain settings shown in Table 2, 28dB is selected. This will prevent the NCP from being overloaded by the microphone. With this setting, the resulting output level of the Pre Amplifier will be $1.26V_{P-P}$.
4. The NCP can have a maximum processing gain of 9dB (depending on the calibration result) which will result in $3.5V_{P-P}$ at the output of the LMV1090. This level is higher then maximum level that is allowed at the input of the post amp of the LMV1090. Therefore the preamp gain has to be reduced, to $1.4V_{P-P}$ minus 9dB = $0.5V_{P-P}$. This limits the preamp gain to a maximum of 20dB.
5. The baseband chip limits the maximum output voltage to $1.5V_{P-P}$ with the minimum of 6dB post amp gain, this results in requiring a lower level at the input of the post amp of $0.75V_{P-P}$. Now calculating this for a maximum NCP gain of 9dB the output of the preamp must be $<266mV_{P-P}$.
6. Calculating the new gain for the preamp will result in <1.4dB gain.
7. The nearest lower gain will be 14dB.

So using preamp gain = 14dB and postamp gain = 6dB is the optimum for this application.

Example 2

An application using microphones with $10mV_{P-P}$ maximum output voltage, and a baseband chip after the LMV1090 with $3.3V_{P-P}$ maximum input voltage.

For optimum noise performance we would like to have the maximum gain at the input stage.

1. $10mV_{P-P}$ + 36dB = $631mV_{P-P}$.
2. This is lower than the maximum $1.4V_{P-P}$ so this is OK.
3. The NCP can have a maximum processing gain of 9dB (depending on the calibration result) which will result in $3.5V_{P-P}$ at the output of the LMV1090. This level is higher then maximum level that is allowed at the input of the Post Amp of the LMV1090. Therefore the Pre Amp gain has to be reduced, to $1.4V_{P-P}$ minus 9dB = $0.5V_{P-P}$. This limits the Pre Amp gain to a maximum of 34dB.
4. With a Post Amp gain setting of 6dB the output of the Post Amp will be $2.8V_{P-P}$ which is OK for the baseband.
5. The nearest lower Post Amp gain will be 6dB.

So using preamp gain = 34dB and postamp gain = 6dB is optimum for this application.

I²C Compatible Interface

The LMV1090 is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line are uni-directional. *The LMV1090 and the master can communicate at clock rates up to 400kHz. Figure 5 shows the I²C Interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LMV1090 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition (Figure 6). The data line is 8 bits long and is always followed by an acknowledge pulse (Figure 7).

I²C Compatible Interface Power Supply Pin (I^2CV_{DD})

The LMV1090 I²C interface is powered up through the I^2CV_{DD} pin. The LMV1090 I²C interface operates at a voltage level set by the I^2CV_{DD} pin which can be set independent to that of the main power supply pin V_{DD}. This is ideal whenever logic levels for the I²C Interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system.

I²C Bus Format

The I²C bus format is shown in Figure 7. The START signal, the transition of SDA from HIGH to LOW while SCL is HIGH is generated, alerting all devices on the bus that a device address is being written to the bus. The 7-bit device address is written to the bus, most significant bit (MSB) first followed by the R/W bit, R/W = 0 indicates the master is writing to the slave device, R/W = 1 indicates the master wants to read data from the slave device. Set R/W = 0; the LMV1090 is a WRITE-ONLY device and will not respond to the R/W =1. The data is latched in on the rising edge of the clock. Each address bit must be stable while SCL is HIGH. After the last address bit is transmitted, the mater device release SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LMV1090 receives the correct address, the device pulls the SDA line low, generating an acknowledge bit (ACK)

Once the master device registers the ACK bit, the 8-bit register data word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register data word is sent, the LMV1090 sends another ACK bit. Following the acknowledgement of the last register data word, the master issues a STOP bit, allowing SDA to go high while SCL is high.

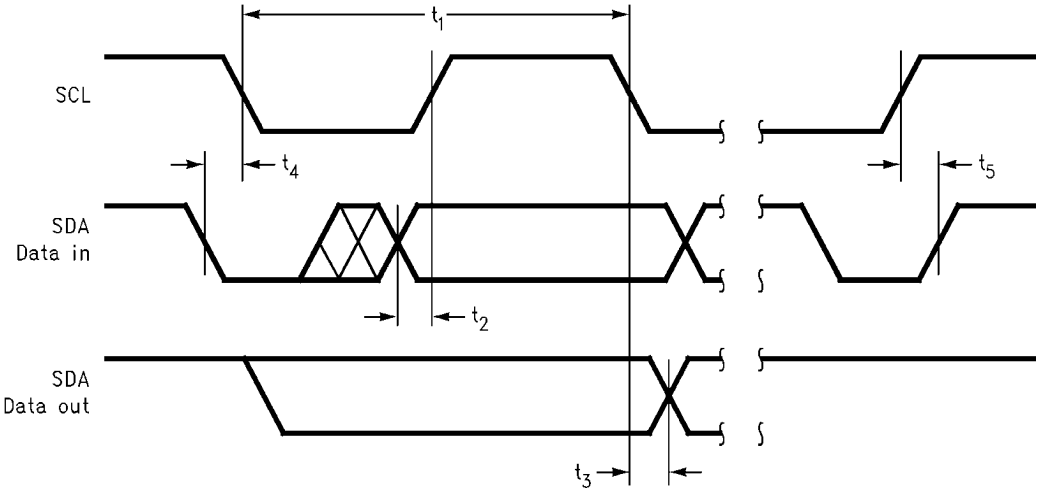


FIGURE 5: I²C Timing Diagram

*The data line is bi-directional (open drain)

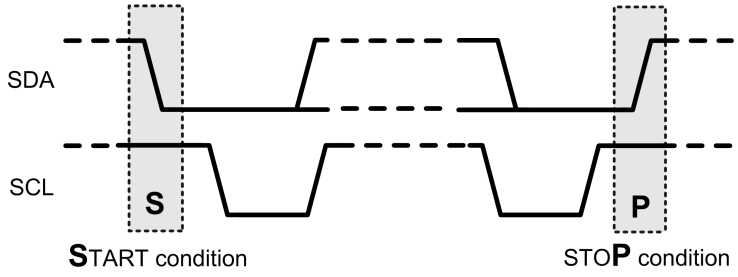


FIGURE 6: I²C Start Stop Conditions

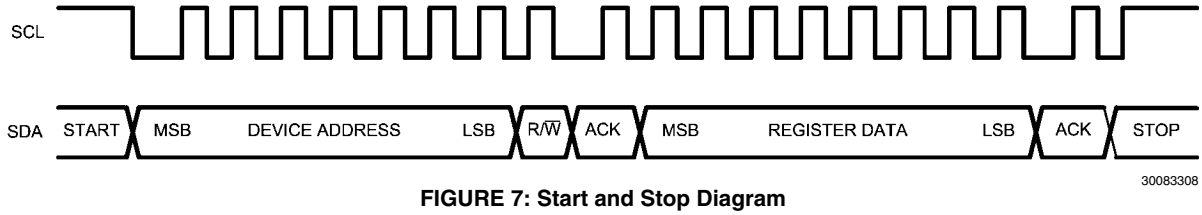


FIGURE 7: Start and Stop Diagram

TABLE 2. Chip Address

	B7	B6	B5	B4	B3	B2	B1	B0/$\overline{W}$
Chip Address	1	1	0	0	1	1	1	0

NOTE: The 7th Bit (B7) of the Register Data determines whether it will activate Register A or Register B.

TABLE 3. I²C Timing Parameters

Symbol	Parameter	Limit		Units
		Min	Max	
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		µs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time (Output direction, delay generated by LMV1090)	300	900	ns
5	Data Hold Time (Input direction, delay generated by the Master)	0	900	ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	20	300	ns
8	Fall Time of SDA and SCL	15	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
C_B	Capacitive Load for Each Bus Line	10	200	pF

NOTE: Data guaranteed by design.

TABLE 4. I²C Register Description

Address B[7]	Reg.	Bits	Description		Default
0	A	Gain setting for the pre amplifier from 6dB up to 36dB in 2dB steps			
		[3:0]	0000	6dB	0000
			0001	8dB	
			0010	10dB	
			0011	12dB	
			0100	14dB	
			0101	16dB	
			0110	18dB	
			0111	20dB	
			1000	22dB	
			1001	24dB	
			1010	26dB	
			1011	28dB	
			1100	30dB	
			1101	32dB	
			1110	34dB	
			1111	36dB	
		Gain setting for the post amplifier from 6dB to 18dB in 3dB steps			
		[6:4]	000	6dB	000
			001	9dB	
			010	12dB	
			011	15dB	
			100	18dB	
			101	18dB	
			110	18dB	
			111	18dB	
			111	18dB	
1	B	[1:0]	B[0] = mute mic 1 and B[1] = mute mic 2 (0 = microphone on)		00
		[3:2]	Mic enable bits, B[3] = enable Mic 2, B[2] = enable Mic 1 (1 = enable), B3 and B2 both 0 = disable Mic 1 and Mic 2		00
		Mic select bits			
		[5:4]	00	Noise cancelling mode	00
			01	Only Mic 1 enabled (pass through)	
			10	Only Mic 2 enabled (pass through)	
			11	Mic 1 + Mic 2	
		[6]	Not Used		

Microphone Placement

Because the LMV1090 is a microphone array Far Field Noise Reduction solution, proper microphone placement is critical for optimum performance. Two things need to be considered: The spacing between the two microphones and the position of the two microphones relative to near field source

If the spacing between the two microphones is too small near field speech will be canceled along with the far field noise. Conversely, if the spacing between the two microphones is large, the far field noise reduction performance will be degraded. The optimum spacing between Mic 1 and Mic 2 is 1.5-2.5cm. This range provides a balance of minimal near field speech loss and maximum far field noise reduction. The microphones should be in line with the desired sound source 'near speech' and configured in an endfire array (see Figure 9) orientation from the sound source. If the 'near speech' (desired sound source) is equidistant to the source like a broadside array (see Figure 8) the result will be a great deal of near field speech loss.

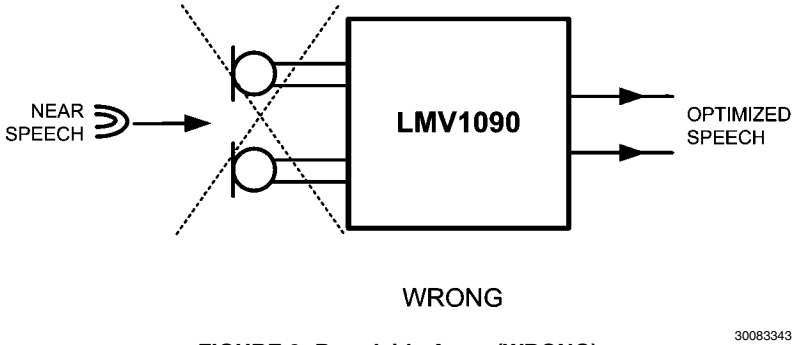


FIGURE 8: Broadside Array (WRONG)

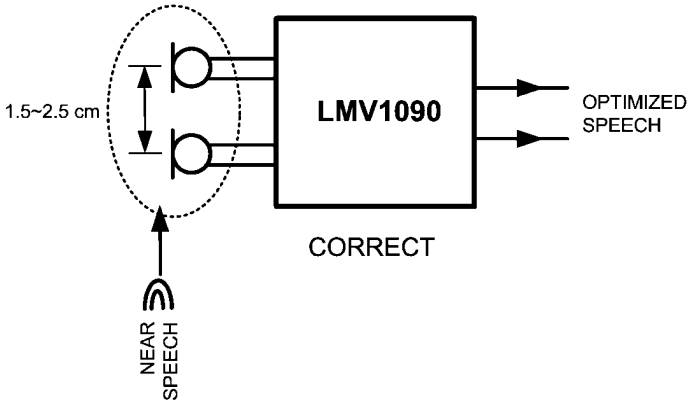


FIGURE 9: Endfire Array (CORRECT)

Low-Pass Filter At The Output

At the output of the LMV1090 there is a provision to create a 1st order low-pass filter (only enabled in 'Noise Cancelling' mode). This low-pass filter can be used to compensate for the change in frequency response that results from the noise cancellation process. The change in frequency response resembles a first-order high-pass filter, and for many of the applications it can be compensated by a first-order low-pass filter with cutoff frequency between 1.5kHz and 2.5kHz.

The transfer function of the low-pass filter is derived as:

$$H(s) = \frac{\text{Post Amplifier gain}}{sR_fC_f+1}$$

This low-pass filter is created by connecting a capacitor between the LPF pin and the OUT pin of the LMV1090. The value of this capacitor also depends on the selected output gain. For different gains the feedback resistance in the low-pass filter network changes as shown in *Table 5*.

TABLE 5. Low-Pass Filter Internal Impedance

Post Amplifier Gain Setting (dB)in Pass Through mode	Feedback Resistance R_f (kΩ)
6	20
9	29
12	40
15	57
18	80

This will result in the following values for a cutoff frequency of 2000 Hz:

TABLE 6. Low-Pass Filter Capacitor For 2kHz

Post Amplifier Gain Setting (dB)	R_f (kΩ)	C_f (nF)
6	20	3.9
9	29	2.7
12	40	2.0
15	57	1.3
18	80	1.0

Measurement Setup

Because of the nature of the calibration system it is not possible to predict the absolute gain in the two microphone channels of the Far Field Noise Cancelling System. This is because, after the calibration function has been operated, the noise cancelling circuit will compensate for the difference in gain between the microphones. In Noise Cancelling mode, this can result in a final gain offset of max 3dB between the gain set in the registers (A[3:0] and B[2:0]) and the actual measured gain between input and output of the LMV1090. After performing a calibration the frequency characteristic of the microphone channels will be matched for the two microphones. As a result of this matching there can be a slight slope in the frequency characteristic in one or both amplifiers.

A-WEIGHTED FILTER

The human ear is sensitive for acoustic signals within a frequency range from about 20Hz to 20kHz. Within this range the sensitivity of the human ear is not equal for each frequency. To approach the hearing response, weighting filters are introduced. One of those filters is the A-weighted filter.

The A-weighted filter is used in signal to noise measurements, where the wanted audio signal is compared to device noise and distortion.

The use of this filter improves the correlation of the measured values to the way these ratios are perceived by the human ear.

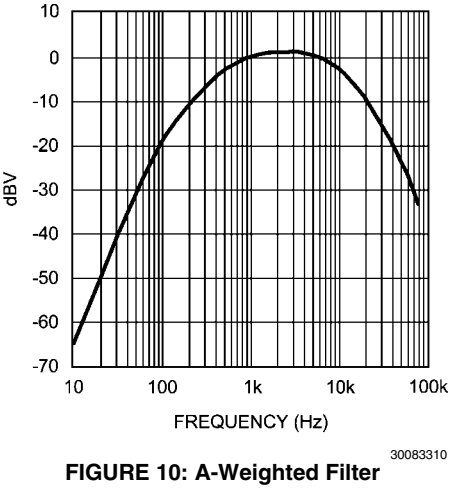


FIGURE 10: A-Weighted Filter

MEASURING NOISE AND SNR

The overall noise of the LMV1090 is measured within the frequency band from 10Hz to 22kHz using an A-weighted filter.

The Mic+ and Mic- inputs of the LMV1090 are AC shorted between the input capacitors, see Figure 11.

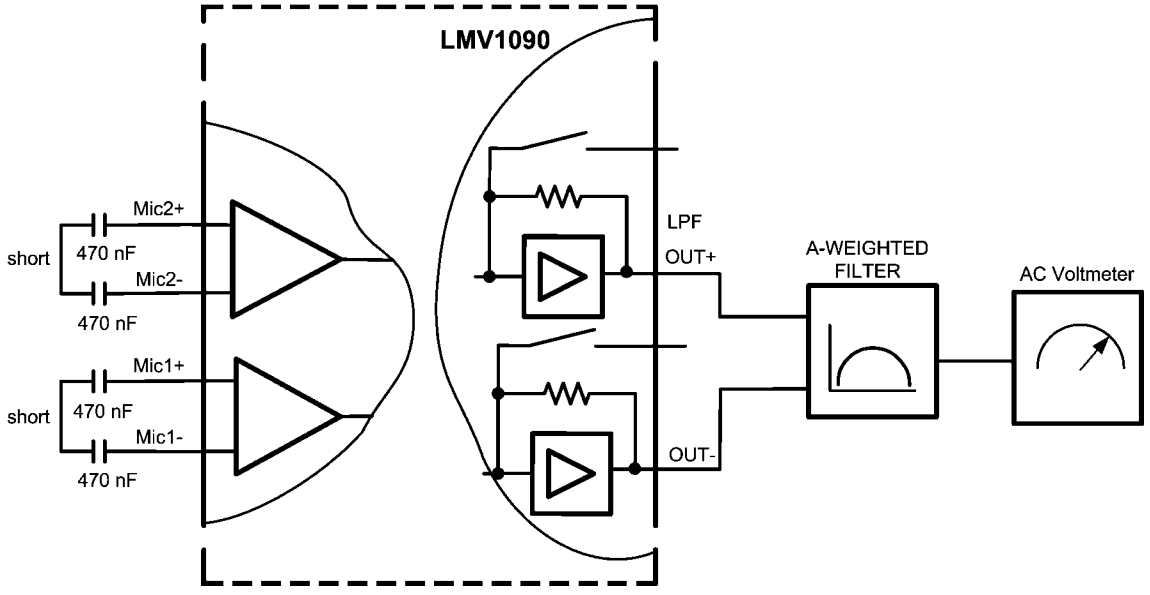


FIGURE 11: Noise Measurement Setup

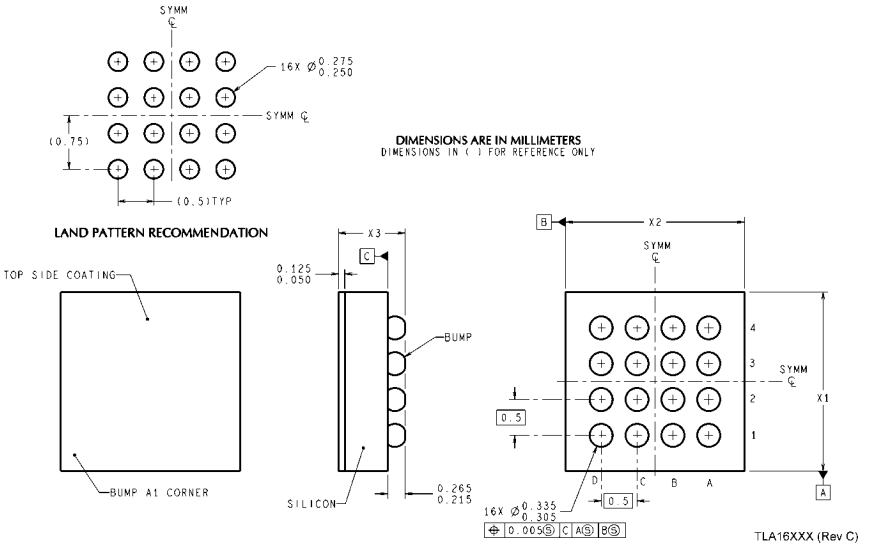
For the signal to noise ratio (SNR) the signal level at the output is measured with a 1kHz input signal of 18mV$_{P-P}$ using an A-weighted filter. This voltage represents the output voltage of a typical electret condenser microphone at a sound pressure level of 94dB SPL, which is the standard level for these measurements. The LMV1090 is programmed for 26dB of total gain (20dB preamplifier and 6dB postamplifier) with only Mic1 or Mic2 used. (See also *I²C Compatible* Interface).

The input signal is applied differentially between the Mic+ and Mic-. Because the part is in Pass Through mode the low-pass filter at the output of the LMV1090 is disabled.

Revision History

Rev	Date	Description
0.01	10/15/08	First edited PDF.
0.02	10/20/08	Text edits.
0.03	10/22/08	Deleted some sections in the Application Information.
0.04	12/12/08	Text edits.
0.05	12/17/08	Re-arranged format.
0.06	01/05/09	Text edits.
0.07	01/07/09	Edited the project's title.
0.08	01/09/09	Text/limits edits.
0.09	01/12/09	Text edits and added 2 tables (I^2C micro tables).
0.10	01/26/09	Text edits.
0.11	02/19/09	Deleted the sign ($Clarisound_{TM}$) from the D/S.
0.12	02/26/09	Text edits.
0.13	03/12/09	Text edits.
0.14	03/19/09	Typical and Limit values edits in the EC tables.
0.15	04/17/09	Added the Typical Performance curves.
0.16	05/06/09	Fixed spelling typo.
0.17	05/12/09	Text edits, then released a “PRODUCT BRIEF” (1st page only).
0.18	05/19/09	Edited the System diagram and input Typical values edits in the EC tables.
0.19	05/21/09	Text edits.
0.20	05/26/09	Edited the markings and the Ordering Information table.
0.21	005/27/09	Updated Typical and Limit values in the EC tables.
0.22	06/03/09	Changed the Limit values (from 850 to 820) on both the 3.3V and 5.0 V EC tables.
0.23	06/04/09	Text edits.
0.24	07/01/09	Input Typical and Limit value edits (Zin) on both the 3.3V and 5.0V EC tables.

Physical Dimensions inches (millimeters) unless otherwise noted



16 Bump micro SMD Technology
NS Package Number TLA1611A
X_1 = 1970mm X_2 = 1970mm X_3 = 600mm

Notes

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