LMV79x 17-MHz, Low-Noise, CMOS Input, 1.8-V Operational Amplifiers With Shutdown

1 Features

Typical 5-V Supply, Unless Otherwise Noted

- Input Referred Voltage Noise 5.8 nV/√Hz
- Input Bias Current 100 fA
- Unity Gain Bandwidth 17 MHz
- Supply Current per Channel Enable Mode
  - LMV791 1.15 mA
  - LMV792 1.30 mA
- Supply Current per Channel in Shutdown Mode 0.02 µA
- Rail-to-Rail Output Swing
  - At 10-kΩ Load, 25 mV from Rail
  - At 2-kΩ Load, 45 mV from Rail
- Ensured 2.5-V and 5-V Performance
- Total Harmonic Distortion 0.01% at1 kHz, 600 Ω
- Temperature Range −40°C to 125°C

2 Applications

- Photodiode Amplifiers
- Active Filters and Buffers
- Low-Noise Signal Processing
- Medical Instrumentation
- Sensor Interface Applications

3 Description

The LMV791 (single) and the LMV792 (dual) low-noise, CMOS input operational amplifiers offer a low input voltage noise density of 5.8 nV/√Hz while consuming only 1.15 mA (LMV791) of quiescent current. The LMV791 and LMV792 are unity gain stable operational amplifiers and have gain bandwidth of 17 MHz. The LMV79x have a supply voltage range of 1.8 V to 5.5 V and can operate from a single supply. The LMV79x each feature a rail-to-rail output stage capable of driving a 600-Ω load and sourcing as much as 60 mA of current.

The LMV79x family provides optimal performance in low-voltage and low-noise systems. A CMOS input stage, with typical input bias currents in the range of a few femtoamperes, and an input common-mode voltage range which includes ground, make the LMV791 and the LMV792 ideal for low-power sensor applications. The LMV79x family has a built-in enable feature which can be used to optimize power dissipation in low power applications.

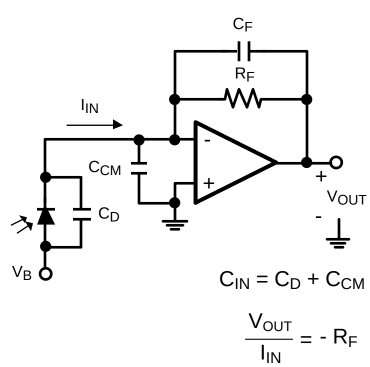
The LMV791x are manufactured using TI's advanced VIP50 process and are offered in a 6-pin SOT and a 10-pin VSSOP package respectively.

Device Information(1)

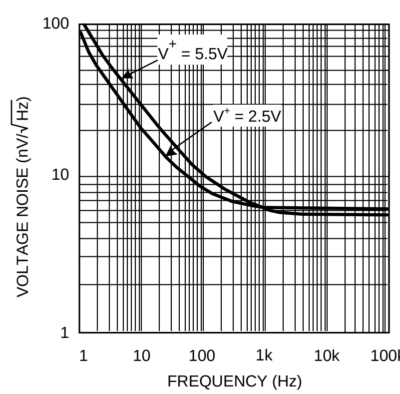
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV791	SOT (6)	2.90 mm × 1.60 mm
LMV792	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Photodiode Transimpedance Amplifier



Low-Noise CMOS Input



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (March 2013) to Revision G — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Updated the format of the Enable and Shutdown Pin Voltage Range in the *2.5-V Electrical Characteristics* table for clarity ... 5
- Updated the format of the Enable and Shutdown Pin Voltage Range in the *5-V Electrical Characteristics* table for clarity . 7

Changes from Revision E (March 2013) to Revision F — **Page**

- Changed layout of National Data Sheet to TI format ... 23

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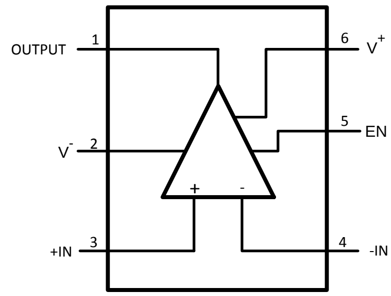
5 Pin Configuration and Functions

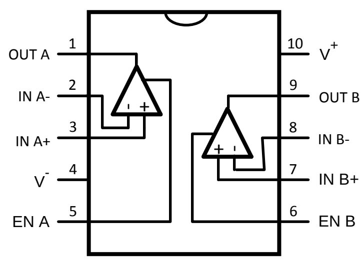
LMV791 DDC Package
6-Pin SOT
Top View



Pin Functions—LMV791

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	5	I	Enable
+IN	3	I	Noninverting Input
–IN	4	I	Inverting Input
Out	1	O	Output
V+	6	P	Positive (highest) Supply Voltage
V–	2	P	Negative (lowest) Supply Voltage

LMV792 DGS Package
10-Pin VSSOP
Top View



Pin Functions—LMV792

PIN		I/O	DESCRIPTION
NAME	NO.		
EN A	5	I	Enable A
EN B	6	I	Enable B
IN A+	3, 7	I	Inverting Input
IN A–	2, 8	I	Noninverting Input
Out	1	O	Output B
Out B	9	O	Output B
V+	10	P	Positive (highest) Supply Voltage
V–	4	P	Negative (lowest) Supply Voltage

6 Specifications

6.1 Absolute Maximum Ratings

See [1][2]

		MIN	MAX	UNIT
V_{IN} differential			±0.3	V
Supply voltage ($V^+ – V^-$)			6	V
Input/Output pin voltage		$V^+ + 0.3$	$V^- − 0.3$	V
Junction temperature[3]			150	°C
Soldering information	Infrared or convection (20 sec)		235	°C
	Wave soldering lead temperature (10 sec)		260	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PCB.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1][2]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[3]	±1000	
		Machine model[4]	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human Body Model is 1.5 kΩ in series with 100 pF.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(4) Machine Model is 0 Ω in series with 200 pF

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
Temperature[1]		−40	125	°C
Supply voltage ($V^+ – V^-$)	$−40°C \le T_J \le 125°C$	2	5.5	V
	$0°C \le T_J \le 125°C$	1.8	5.5	V

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PCB.

6.4 Thermal Information

THERMAL METRIC[1]		LMV791	LMV792	UNIT
		DDC (SOT-23)	DGS (VSSOP)	
		6 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	191.8	179.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.1	70.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.9	99.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	11.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.5	98.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PCB.

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6.5 2.5-V Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_J = 25°C, V^+ = 2.5 V, V^- = 0 V, $V_{CM} = V^+/2 = V_O$, $V_{EN} = V^+$.

PARAMETER		TEST CONDITIONS			MIN[1]	TYP[2]	MAX[1]	UNIT
V_{OS}	Input offset voltage	T_J = 25 °C				0.1	±1.35	mV
		−40°C ≤ T_J ≤ 125°C					±1.65	
TC V_{OS}	Input offset voltage temperature drift	LMV791[3]				−1		μV/°C
		LMV792[3]				−1.8		
I_B	Input bias current	V_{CM} = 1 V[4] [5]	T_J = 25 °C			0.05	1	pA
			−40°C ≤ T_J ≤ 85 °C				25	
			−40°C ≤ T_J ≤ 125 °C				100	
I_{OS}	Input offset current	V_{CM} = 1 V[5]				10		fA
CMRR	Common-mode rejection ratio	0 V ≤ V_{CM} ≤ 1.4 V	T_J = 25 °C		80	94		dB
			−40°C ≤ T_J ≤ 125°C		75			
PSRR	Power supply rejection ratio	2.0V ≤ V^+ ≤ 5.5V, V_{CM} = 0 V	T_J = 25 °C		80	100		dB
			−40°C ≤ T_J ≤ 125°C		75			
		1.8 V ≤ V^+ ≤ 5.5 V, V_{CM} = 0 V			80	98		
CMVR	Common-mode voltage range	CMRR ≥ 60 dB	T_J = 25 °C		−0.3		1.5	V
		CMRR ≥ 55 dB	−40°C ≤ T_J ≤ 125°C		−0.3		1.5	
A_{VOL}	Open-loop voltage gain	V_{OUT} = 0.15 V to 2.2 V, R_{LOAD} = 2 kΩ to $V^+/2$	LMV791	T_J = 25 °C	85	98		dB
				−40°C ≤ T_J ≤ 125°C	80			
			LMV792	T_J = 25 °C	82	92		
				−40°C ≤ T_J ≤ 125°C	78			
		V_{OUT} = 0.15 V to 2.2 V, R_{LOAD} = 10 kΩ to $V^+/2$	T_J = 25 °C		88	110		
			−40°C ≤ T_J ≤ 125°C		84			
V_{OUT}	Output voltage swing high	R_{LOAD} = 2 kΩ to $V^+/2$	T_J = 25 °C			25	75	mV from either rail
			−40°C ≤ T_J ≤ 125°C				82	
		R_{LOAD} = 10 kΩ to $V^+/2$	T_J = 25 °C			20	65	
			−40°C ≤ T_J ≤ 125°C				71	
	Output voltage swing low	R_{LOAD} = 2 kΩ to $V^+/2$	T_J = 25 °C			30	75	
			−40°C ≤ T_J ≤ 125°C				78	
		R_{LOAD} = 10 kΩ to $V^+/2$	T_J = 25 °C			15	65	
			−40°C ≤ T_J ≤ 125°C				67	
I_{OUT}	Output current	Sourcing to V^- V_{IN} = 200 mV[6]	T_J = 25 °C		35	47		mA
			−40°C ≤ T_J ≤ 125°C		28			
		Sinking to V^+ V_{IN} = –200 mV[6]	T_J = 25 °C		7	15		
			−40°C ≤ T_J ≤ 125°C		5			
I_S	Supply current per amplifier	Enable mode V_{EN} ≥ 2.1 V	LMV791	T_J = 25 °C		0.95	1.3	mA
				−40°C ≤ T_J ≤ 125°C			1.65	
			LMV792 per channel	T_J = 25 °C		1.1	1.50	
				−40°C ≤ T_J ≤ 125°C			1.85	
		Shutdown mode, V_{EN} < 0.4 per channel	T_J = 25 °C			0.02	1	μA
			−40°C ≤ T_J ≤ 125°C				5	
SR	Slew rate	A_V = +1, Rising (10% to 90%)				8.5		V/μs
		A_V = +1, Falling (90% to 10%)				10.5		
GBW	Gain bandwidth					14		MHz
e_n	Input referred voltage noise density	f = 1 kHz				6.2		nV/√Hz
i_n	Input referred current noise density	f = 1 kHz				0.01		pA/√Hz
t_{on}	Turnon time					140		ns
t_{off}	Turnoff time					1000		ns
V_{EN}	Enable pin voltage range	Enable mode			2.1	2		V
		Shutdown mode				0.5	0.4	

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using the statistical quality control (SQC) method.
(2) Typical values represent the parametric norm at the time of characterization.
(3) Offset voltage average drift is determined by dividing the change in V_{OS} by temperature change.
(4) Positive current corresponds to current flowing into the device.
(5) This parameter is specified by design and/or characterization and is not tested in production.
(6) The short circuit test is a momentary test, the short circuit duration is 1.5 ms.

2.5-V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_J = 25°C, V^+ = 2.5 V, V^- = 0 V, V_{CM} = V^+/2 = V_O, V_{EN} = V^+.

PARAMETER		TEST CONDITIONS	MIN[1]	TYP[2]	MAX[1]	UNIT
I_{EN}	Enable pin input current	Enable mode V_{EN} = 2.5 V[4]		1.5	3	μA
		Shutdown mode V_{EN} = 0 V[4]		0.003	0.1	
THD+N	Total harmonic distortion + noise	f = 1 kHz, A_V = 1, R_{LOAD} = 600 Ω		0.01%		

6.6 5-V Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V^+/2 = V_O, V_{EN} = V^+.

PARAMETER		TEST CONDITIONS			MIN[1]	TYP[2]	MAX[1]	UNIT
V_{OS}	Input offset voltage	T_J = 25 °C				0.1	±1.35	mV
		−40°C ≤ T_J ≤ 125°C					±1.65	
TC V_{OS}	Input offset voltage temperature drift	LMV791[3]				−1		μV/°C
		LMV792[3]				−1.8		
I_B	Input bias current	V_{CM} = 2 V[4] [5]	T_J = 25 °C			0.1	1	pA
			−40°C ≤ T_J ≤ 85°C				25	
			−40°C ≤ T_J ≤ 125°C				100	
I_{OS}	Input offset current	V_{CM} = 2 V[5]				10		fA
CMRR	Common-mode rejection ratio	0 V ≤ V_{CM} ≤ 3.7 V	T_J = 25 °C		80	100		dB
			−40°C ≤ T_J ≤ 125°C		75			
PSRR	Power supply rejection ratio	2.0V ≤ V^+ ≤ 5.5 V, V_{CM} = 0 V	T_J = 25 °C		80	100		dB
			−40°C ≤ T_J ≤ 125°C		75			
		1.8V ≤ V^+ ≤ 5.5 V, V_{CM} = 0 V			80	98		
CMVR	Common-mode voltage range	CMRR ≥ 60 dB	T_J = 25 °C		−0.3		4	V
		CMRR ≥ 55 dB	−40°C ≤ T_J ≤ 125°C		−0.3		4	
A_{VOL}	Open-loop voltage gain	V_{OUT} = 0.3V to 4.7V, R_{LOAD} = 2 kΩ to V^+/2	LMV791	T_J = 25 °C	85	97		dB
				−40°C ≤ T_J ≤ 125°C	80			
			LMV792	T_J = 25 °C	82	89		
				−40°C ≤ T_J ≤ 125°C	78			
		V_{OUT} = 0.3V to 4.7V, R_{LOAD} = 10 kΩ to V^+/2	T_J = 25 °C		88	110		
			−40°C ≤ T_J ≤ 125°C		84			
V_{OUT}	Output voltage swing high	R_{LOAD} = 2 kΩ to V^+/2	T_J = 25 °C			35	75	mV from either rail
			−40°C ≤ T_J ≤ 125°C				82	
		R_{LOAD} = 10 kΩ to V^+/2	T_J = 25 °C			25	65	
			−40°C ≤ T_J ≤ 125°C				71	
	Output voltage swing low	R_{LOAD} = 2 kΩ to V^+/2	LMV791	T_J = 25 °C		42	75	
				−40°C ≤ T_J ≤ 125°C			78	
			LMV792	T_J = 25 °C		45	80	
				−40°C ≤ T_J ≤ 125°C			83	
		R_{LOAD} = 10 kΩ to V^+/2	T_J = 25 °C			20	65	
			−40°C ≤ T_J ≤ 125°C				67	
I_{OUT}	Output current	Sourcing to V^- V_{IN} = 200 mV[6]	T_J = 25 °C		45	60		mA
			−40°C ≤ T_J ≤ 125°C		37			
		Sinking to V^+ V_{IN} = –200 mV[6]	T_J = 25 °C		10	21		
			−40°C ≤ T_J ≤ 125°C		6			
I_S	Supply current per amplifier	Enable mode V_{EN} ≥ 4.6 V	LMV791	T_J = 25 °C		1.15	1.4	mA
				−40°C ≤ T_J ≤ 125°C			1.75	
			LMV792 per channel	T_J = 25 °C		1.3	1.7	
				−40°C ≤ T_J ≤ 125°C			2.05	
		Shutdown mode (V_{EN} ≤ 0.4 V)	T_J = 25 °C			0.14	1	μA
			−40°C ≤ T_J ≤ 125°C				5	

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using the statistical quality control (SQC) method.
(2) Typical values represent the parametric norm at the time of characterization.
(3) Offset voltage average drift is determined by dividing the change in V_{OS} by temperature change.
(4) Positive current corresponds to current flowing into the device.
(5) This parameter is specified by design and/or characterization and is not tested in production.
(6) The short circuit test is a momentary test, the short circuit duration is 1.5 ms.

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5-V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V^+/2 = V_O, V_{EN} = V^+.

PARAMETER		TEST CONDITIONS	MIN[1]	TYP[2]	MAX[1]	UNIT
SR	Slew rate	A_V = +1, Rising (10% to 90%)	6	9.5		V/μs
		A_V = +1, Falling (90% to 10%)	7.5	11.5		
GBW	Gain bandwidth			17		MHz
e_n	Input referred voltage noise density	f = 1 kHz		5.8		nV/$\sqrt{Hz}$
i_n	Input referred current noise density	f = 1 kHz		0.01		pA/$\sqrt{Hz}$
t_{on}	Turnon time			110		ns
t_{off}	Turnoff time			800		ns
V_{EN}	Enable pin voltage range	Enable mode	4.6	4.5		V
		Shutdown mode		0.5	0.4	
I_{EN}	Enable pin input current	Enable mode V_{EN} = 5 V[4]		5.6	10	μA
		Shutdown mode V_{EN} = 0 V[4]		0.005	0.2	
THD+N	Total harmonic distortion + noise	f = 1 kHz, A_V = 1, R_{LOAD} = 600 Ω		0.01%		

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6.7 Typical Characteristics

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2, V_{EN} = V^+.

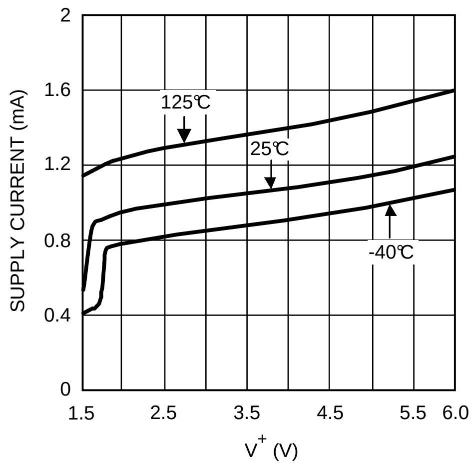

Figure 1. Supply Current vs Supply Voltage (LMV791)

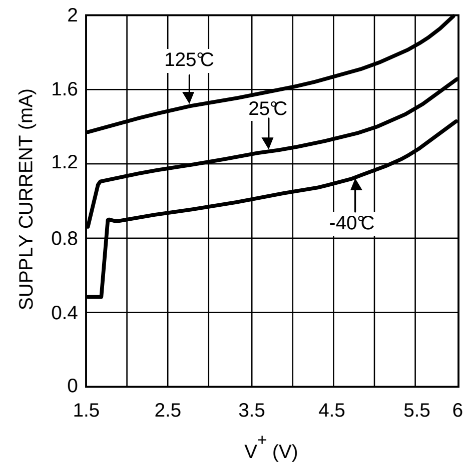

Figure 2. Supply Current vs Supply Voltage (LMV792)

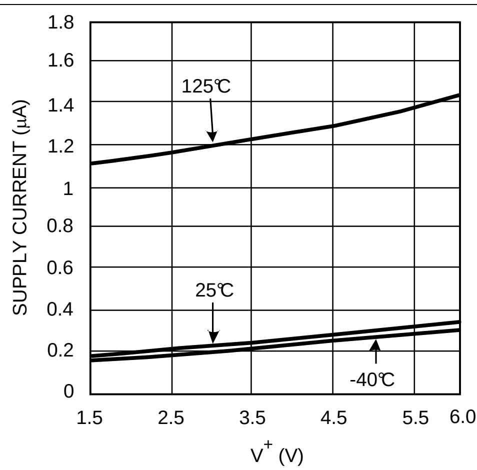

Figure 3. Supply Current vs Supply Voltage in Shutdown Mode

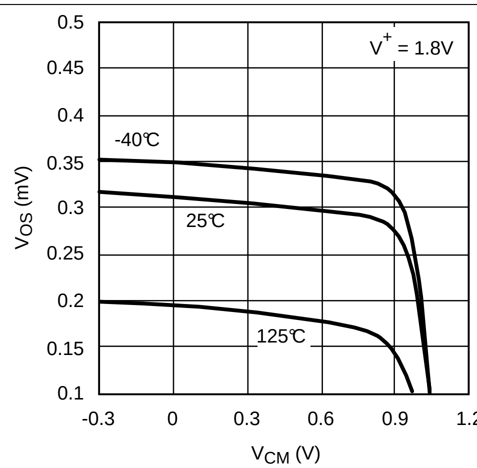

Figure 4. V_{OS} vs V_{CM}

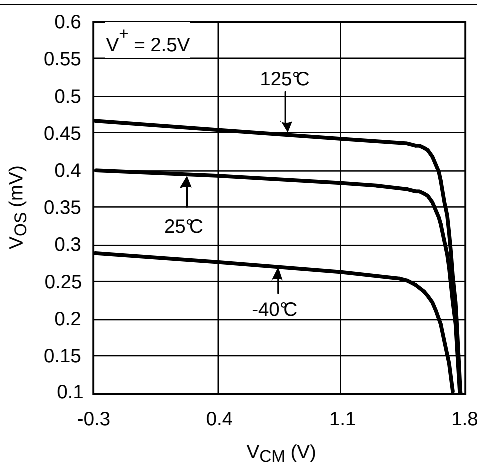

Figure 5. V_{OS} vs V_{CM}

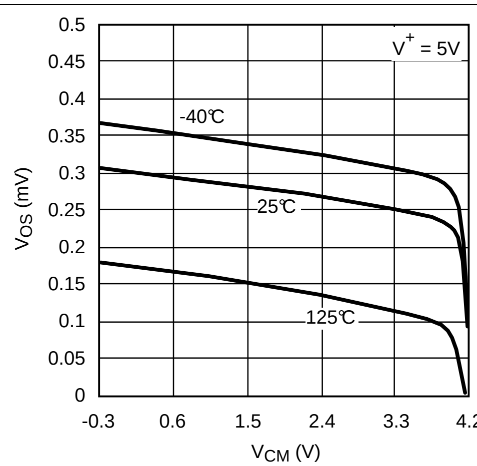

Figure 6. V_{OS} vs V_{CM}

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Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2, V_{EN} = V^+.

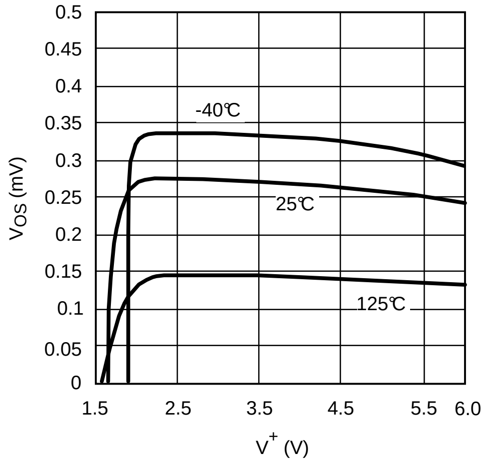

Figure 7. V_{OS} vs Supply Voltage

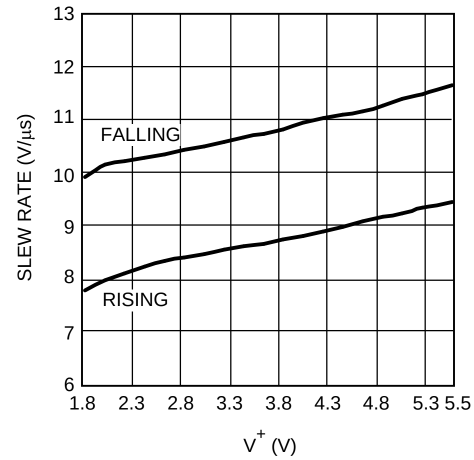

Figure 8. Slew Rate vs Supply Voltage

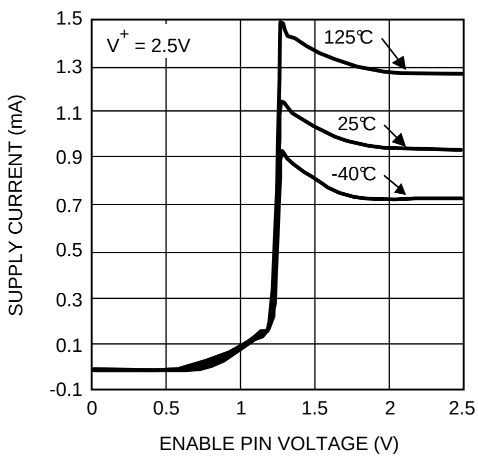

Figure 9. Supply Current vs Enable Pin Voltage (LMV791)

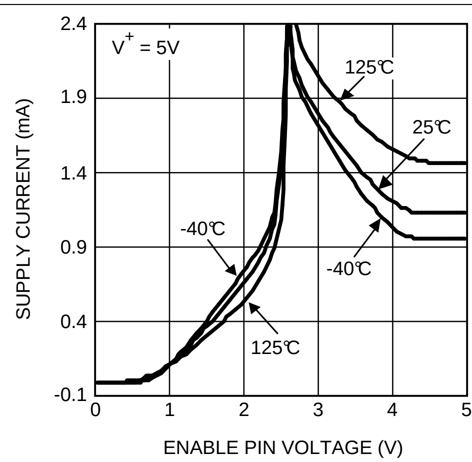

Figure 10. Supply Current vs Enable Pin Voltage(LMV791)

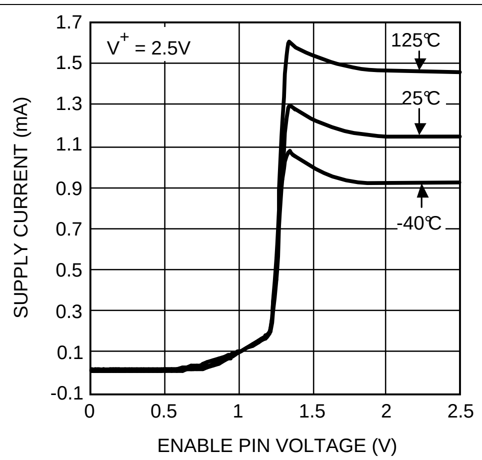

Figure 11. Supply Current vs Enable Pin Voltage (LMV792)

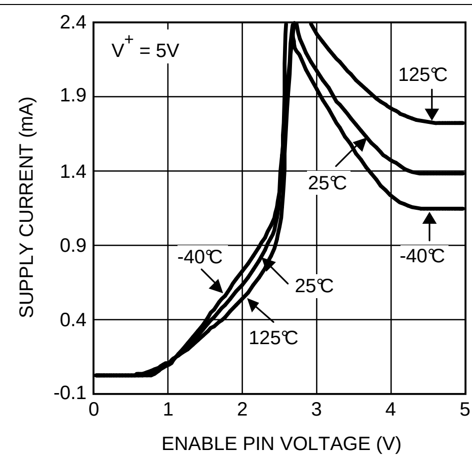

Figure 12. Supply Current vs Enable Pin Voltage (LMV792)

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2, V_{EN} = V^+.

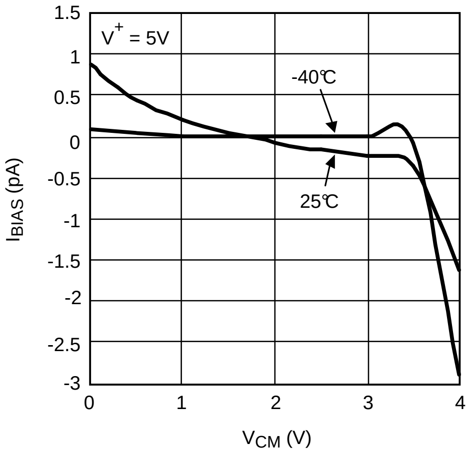

Figure 13. Input Bias Current vs V_{CM}

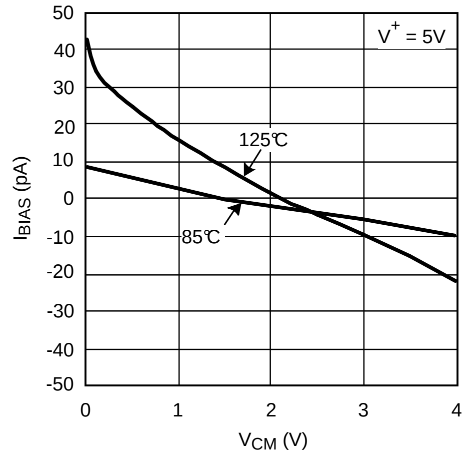

Figure 14. Input Bias Current vs V_{CM}

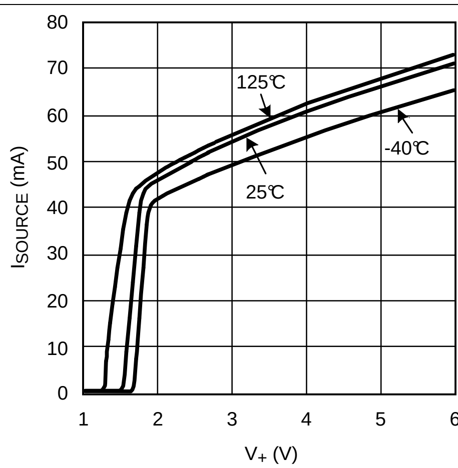

Figure 15. Sourcing Current vs Supply Voltage

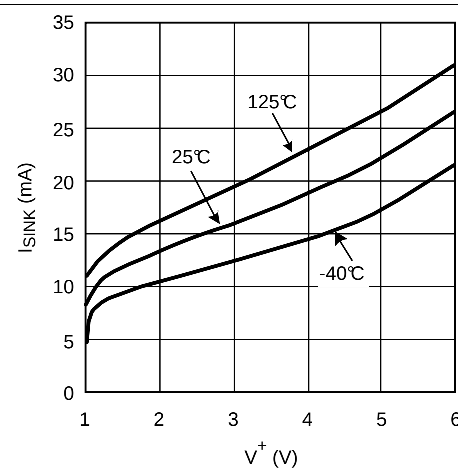

Figure 16. Sinking Current vs Supply Voltage

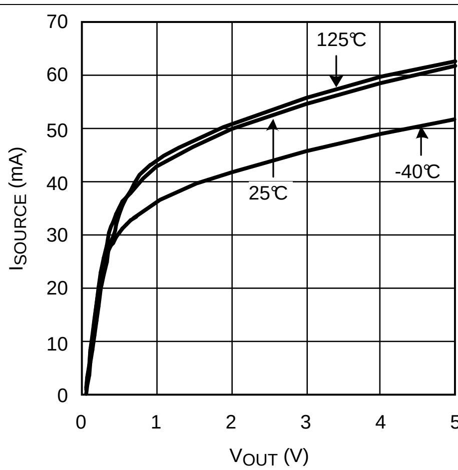

Figure 17. Sourcing Current vs Output Voltage

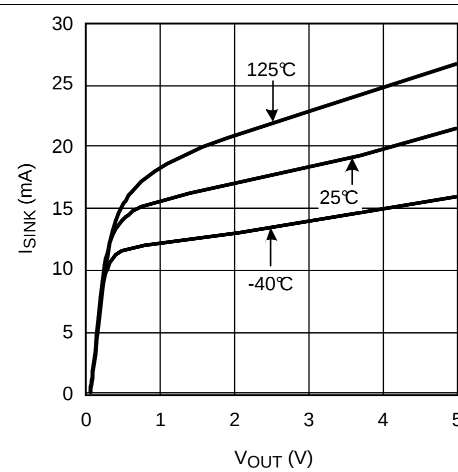

Figure 18. Sinking Current vs Output Voltage

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Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2, V_{EN} = V^+.

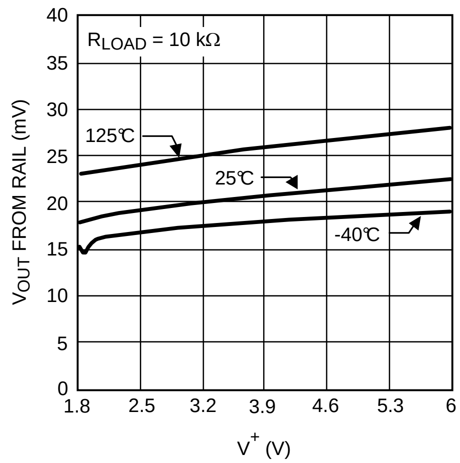

Figure 19. Positive Output Swing vs Supply Voltage

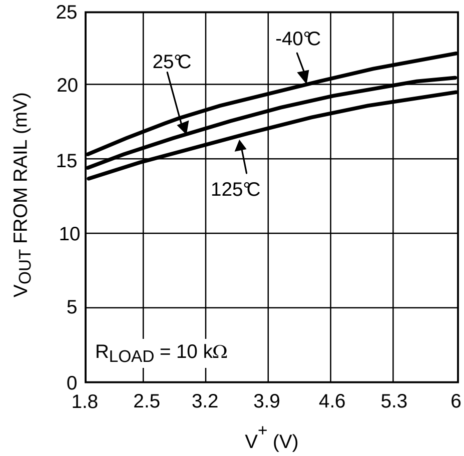

Figure 20. Negative Output Swing vs Supply Voltage

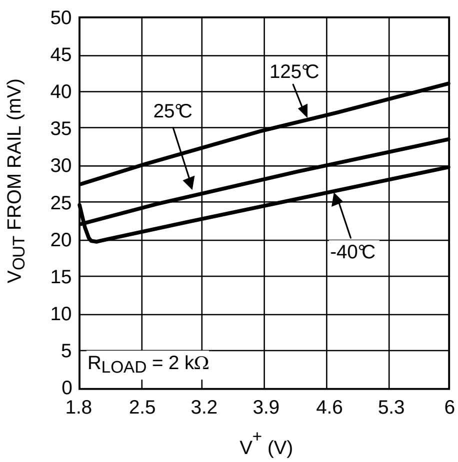

Figure 21. Positive Output Swing vs Supply Voltage

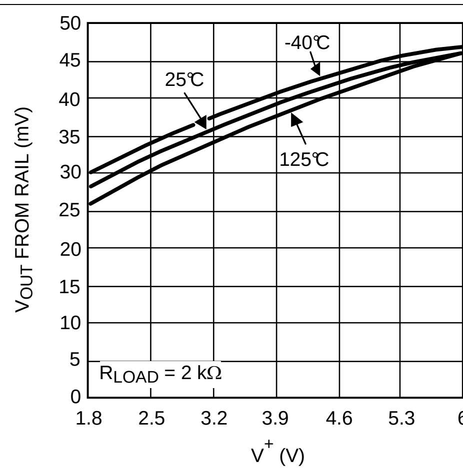

Figure 22. Negative Output Swing vs Supply Voltage

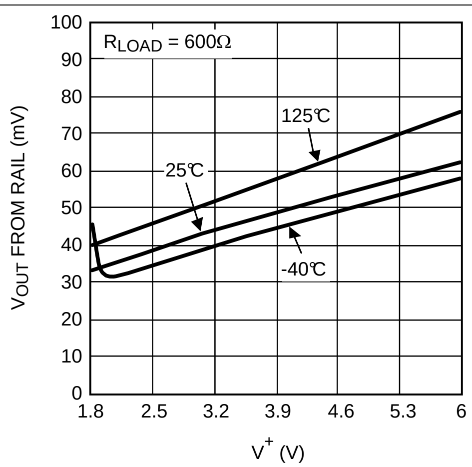

Figure 23. Positive Output Swing vs Supply Voltage

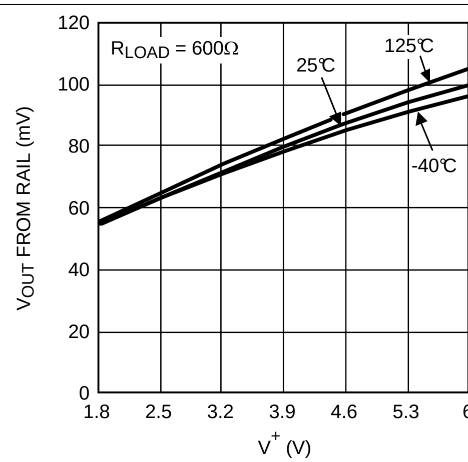

Figure 24. Negative Output Swing vs Supply Voltage

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = $V^+/2$, V_{EN} = V^+.

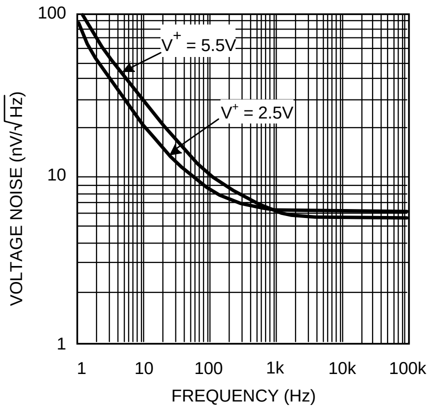

Figure 25. Input Referred Voltage Noise vs Frequency

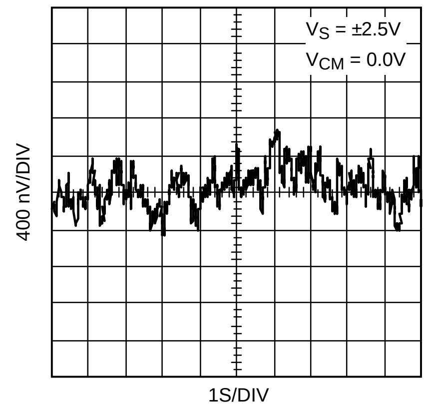

Figure 26. Time Domain Voltage Noise

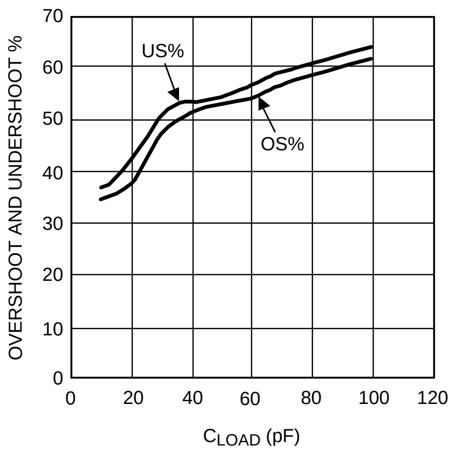

Figure 27. Overshoot and Undershoot vs C_{LOAD}

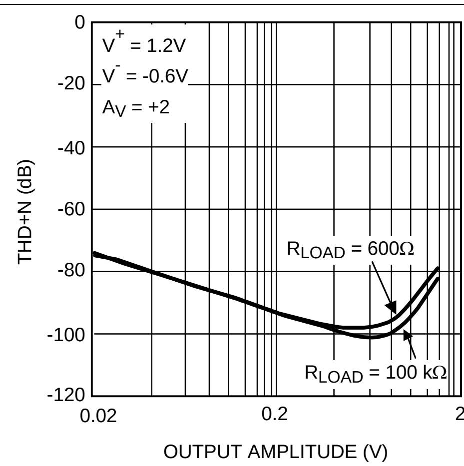

Figure 28. THD+N vs Peak-to-Peak Output Voltage (V_{OUT})

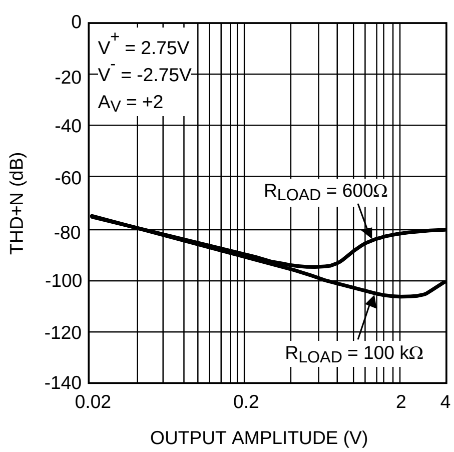

Figure 29. THD+N vs Peak-to-Peak Output Voltage (V_{OUT})

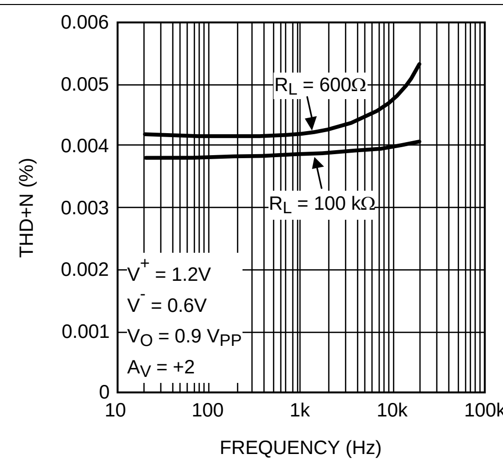

Figure 30. THD+N vs Frequency

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Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2, V_{EN} = V^+.

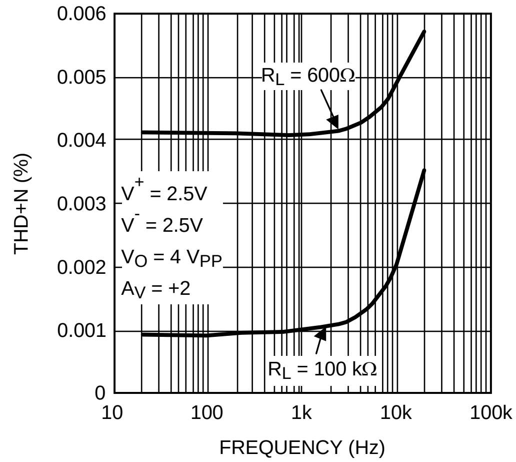

Figure 31. THD+N vs Frequency

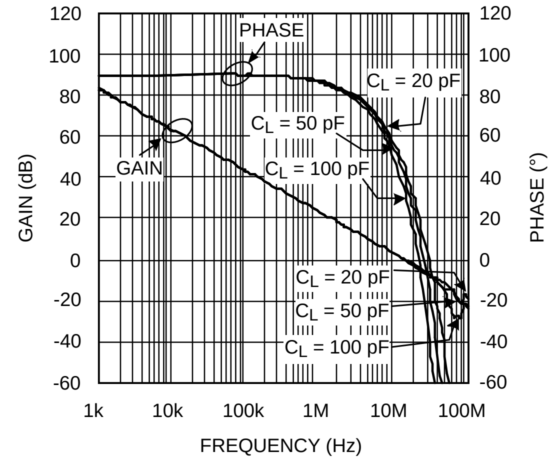

Figure 32. Open-Loop Gain and Phase With Capacitive Load

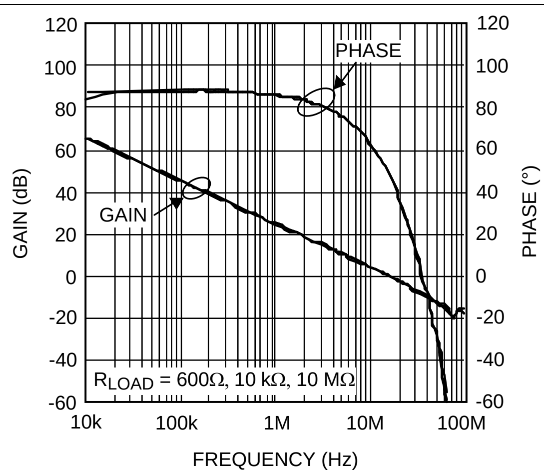

Figure 33. Open-Loop Gain and Phase With Resistive Load

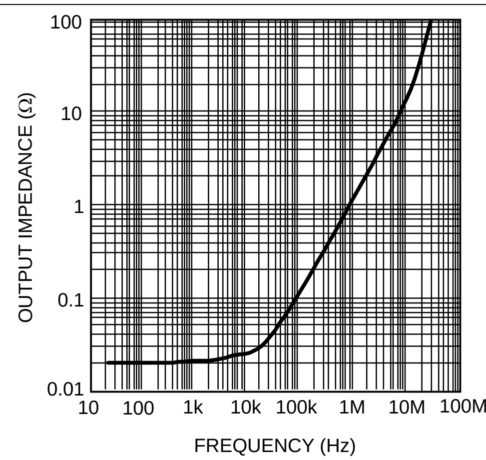

Figure 34. Closed-Loop Output Impedance vs Frequency

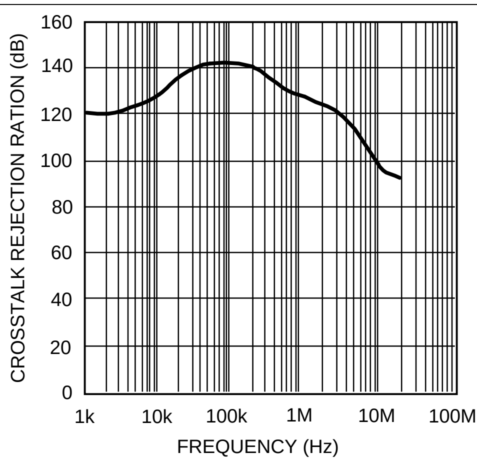

Figure 35. Crosstalk Rejection

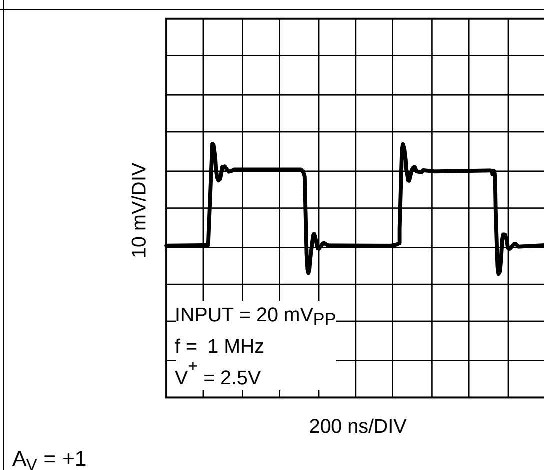

Figure 36. Small Signal Transient Response

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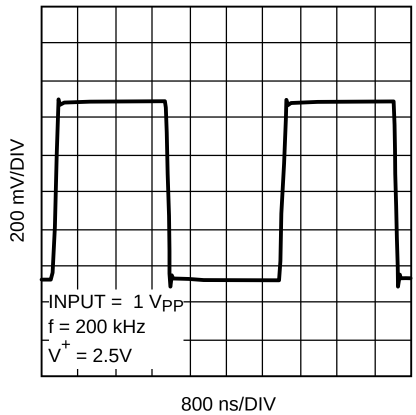
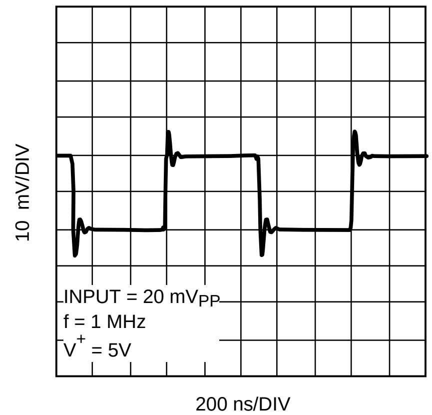
Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2, V_{EN} = V^+.



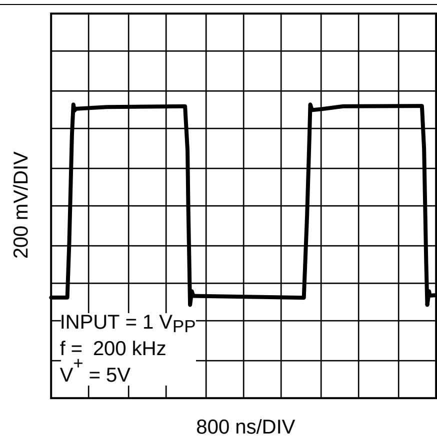
A_V = +1

Figure 37. Large Signal Transient Response



A_V = +1

Figure 38. Small Signal Transient Response



A_V = +1

Figure 39. Large Signal Transient Response

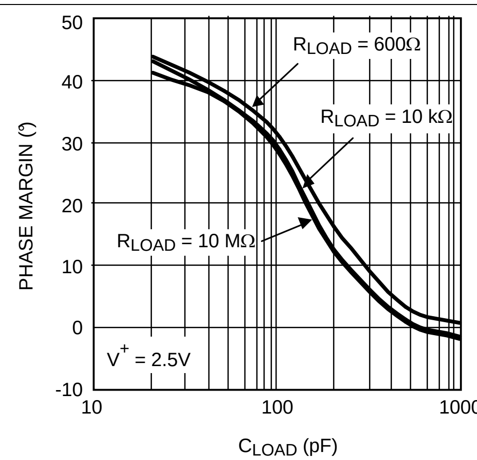


Figure 40. Phase Margin vs Capacitive Load (Stability)

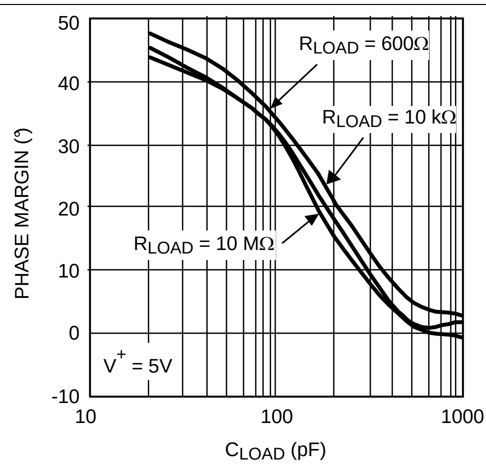


Figure 41. Phase Margin vs Capacitive Load (Stability)

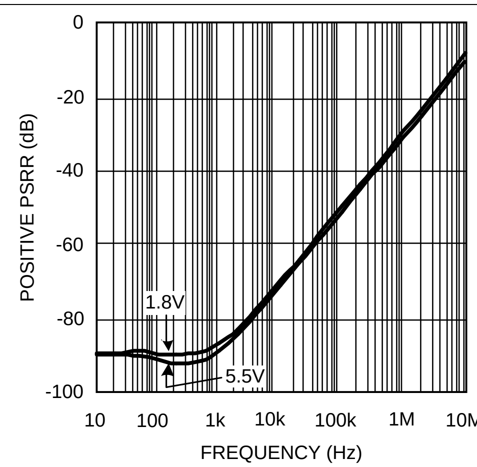


Figure 42. Positive PSRR vs Frequency

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Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = $V^+/2$, V_{EN} = V^+.

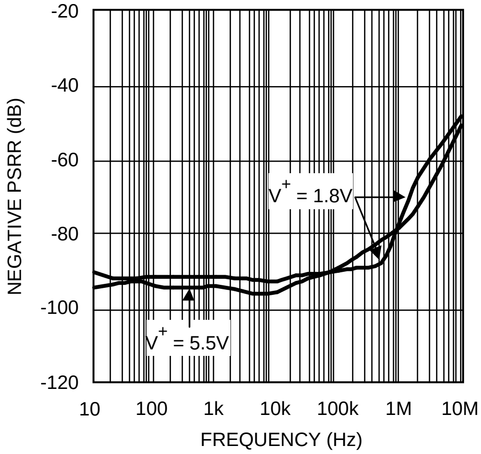


Figure 43. Negative PSRR vs Frequency

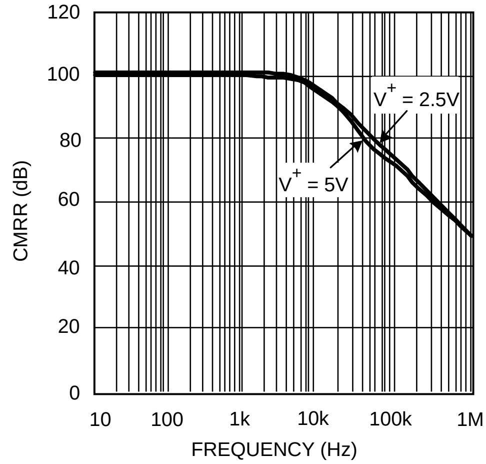


Figure 44. CMRR vs Frequency

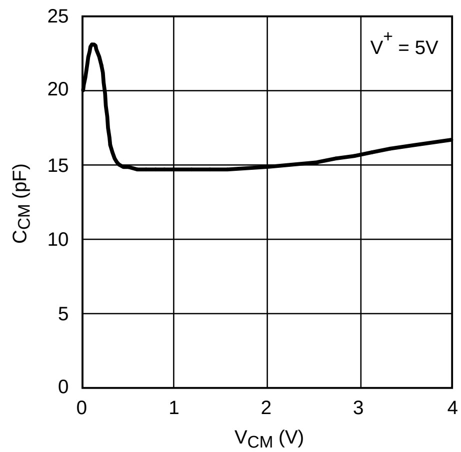


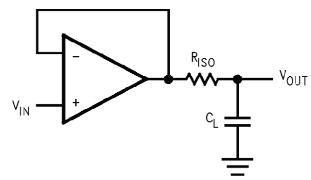
Figure 45. Input Common-Mode Capacitance vs V_{CM}

7 Detailed Description

7.1 Overview

The LMV79x family provides optimal performance in low-voltage and low-noise systems. A low-noise CMOS input stage, with typical input bias currents in the range of a few femtoamperes, and an input common-mode voltage range which includes ground make the LMV791 and the LMV792 ideal for low-power sensor applications

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Wide Bandwidth at Low Supply Current

The LMV791 and LMV792 are high performance operational amplifiers that provide a unity gain bandwidth of 17 MHz while drawing a low supply current of 1.15 mA. This makes them ideal for providing wideband amplification in portable applications. The shutdown feature can also be used to design more power efficient systems that offer wide bandwidth and high performance while consuming less average power.

7.3.2 Low Input Referred Noise and Low Input Bias Current

The LMV79x have a very low input referred voltage noise density (5.8 nV/√Hz at 1 kHz). A CMOS input stage ensures a small input bias current (100 fA) and low input referred current noise (0.01 pA/√Hz). This is very helpful in maintaining signal fidelity, and makes the LMV791 and LMV792 ideal for audio and sensor-based applications.

7.3.3 Low Supply Voltage

The LMV791 and the LMV792 have performance ensured at 2.5-V and 5-V supply. The LMV791 family is ensured to be operational at all supply voltages between 2 V and 5.5 V, for ambient temperatures ranging from −40°C to 125°C, thus using the entire battery lifetime. The LMV791 and LMV792 are also ensured to be operational at 1.8-V supply voltage, for temperatures between 0°C and 125°C. This makes the LMV791 family ideal for usage in low-voltage commercial applications.

7.3.4 Rail-to-Rail Output and Ground Sensing

Rail-to-rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating at low supply voltages. An innovative positive feedback scheme is used to boost the current drive capability of the output stage. This allows the LMV791 and the LMV792 to source more than 40 mA of current at 1.8-V supply. This also limits the performance of the LMV791 family as comparators, and hence the usage of the LMV791 and the LMV792 in an open-loop configuration is not recommended. The input common-mode range includes the negative supply rail which allows direct sensing at ground in single supply operation.

7.3.5 Shutdown Feature

The LMV791 family is ideal for battery-powered systems. With a low supply current of 1.15 mA and a shutdown current of 140 nA typically, the LMV791 and LMV792 allow the designer to maximize battery life. The enable pin of the LMV791 and the LMV792 allows the operational amplifier to be turned off and reduce its supply current to less than 1 μA. To power on the operational amplifier the enable pin should be higher than V^+ – 0.5 V, where V^+ is the positive supply. To disable the operational amplifier, the enable pin voltage should be less than V^- + 0.5 V, where V^- is the negative supply.

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Feature Description (continued)

7.3.6 Small Size

The small footprint of the LMV791 and the LMV792 package saves space on printed-circuit-boards, and enables the design of smaller electronic products, such as mobile phones, tablets, or other portable systems. Long traces between the signal source and the operational amplifier make the signal path susceptible to noise. By using a physically smaller LMV791 and LMV792 package, the operational amplifier can be placed closer to the signal source, reducing noise pick-up and increasing signal integrity.

7.4 Device Functional Modes

7.4.1 Capacitive Load Tolerance

The LMV791 and LMV792 can directly drive up to 120 pF in unity gain without oscillation. The unity gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the output impedance of the amplifier and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. To drive a heavier capacitive load, the circuit in Figure 46 can be used.

In Figure 46, the isolation resistor R_{ISO} and the load capacitor C_L form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of R_{ISO}. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Increased R_{ISO} would, however, result in a reduced output swing and short circuit current.

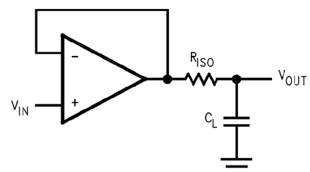
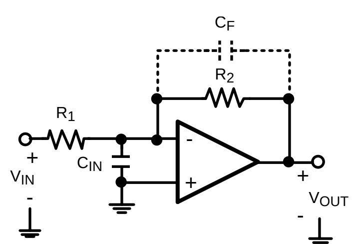


Figure 46. Isolation of C_L to Improve Stability

7.4.2 Input Capacitance and Feedback Circuit Elements

The LMV791 family has a very low input bias current (100 fA) and a low 1/f noise corner frequency (400 Hz), which makes it ideal for sensor applications. However, to obtain this performance a large CMOS input stage is used, which adds to the input capacitance of the operational amplifier, C_{IN}. Though this does not affect the DC and low frequency performance, at higher frequencies the input capacitance interacts with the input and the feedback impedances to create a pole, which results in lower phase margin and gain peaking. This can be controlled by being selective in the use of feedback resistors, as well as by using a feedback capacitance, C_F. For example, in the inverting amplifier shown in Figure 47, if C_{IN} and C_F are ignored and the open-loop gain of the operational amplifier is considered infinite then the gain of the circuit is $-R_2/R_1$. An operational amplifier, however, usually has a dominant pole, which causes its gain to drop with frequency. Hence, this gain is only valid for DC and low frequency. To understand the effect of the input capacitance coupled with the non-ideal gain of the operational amplifier, the circuit needs to be analyzed in the frequency domain using a Laplace transform.



$$A_V = -\frac{V_{OUT}}{V_{IN}} = -\frac{R_2}{R_1}$$

Figure 47. Inverting Amplifier

Device Functional Modes (continued)

For simplicity, the operational amplifier is modeled as an ideal integrator with a unity gain frequency of A_0. Hence, its transfer function (or gain) in the frequency domain is A_0/s. Solving the circuit equations in the frequency domain, ignoring C_F for the moment, results in an expression for the gain shown in Equation 1.

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_2/R_1}{\left[1 + \frac{s}{\left(\frac{A_0\,R_1}{R_1 + R_2}\right)} + \frac{s^2}{\left(\frac{A_0}{C_{IN}\,R_2}\right)}\right]} \tag{1}$$

It can be inferred from the denominator of the transfer function that it has two poles, whose expressions can be obtained by solving for the roots of the denominator and are shown in Equation 2.

$$P_{1,2} = \frac{-1}{2C_{IN}}\left[\frac{1}{R_1} + \frac{1}{R_2} \pm \sqrt{\left(\frac{1}{R_1} + \frac{1}{R_2}\right)^2 - \frac{4\,A_0 C_{IN}}{R_2}}\right] \tag{2}$$

Equation 2 shows that as the values of R_1 and R_2 are increased, the magnitude of the poles, and hence the bandwidth of the amplifier, is reduced. This theory is verified by using different values of R_1 and R_2 in the circuit shown in Figure 46 and by comparing their frequency responses. In Figure 48 the frequency responses for three different values of R_1 and R_2 are shown. When both R_1 and R_2 are 1 kΩ, the response is flattest and widest; whereas, it narrows and peaks significantly when both their values are changed to 10 kΩ or 30 kΩ. So it is advisable to use lower values of R_1 and R_2 to obtain a wider and flatter response. Lower resistances also help in high-sensitivity circuits because they add less noise.

A way of reducing the gain peaking is by adding a feedback capacitance C_F in parallel with R_2. This introduces another pole in the system and prevents the formation of pairs of complex conjugate poles which cause the gain to peak. Figure 49 shows the effect of C_F on the frequency response of the circuit. Adding a capacitance of 2 pF removes the peak, while a capacitance of 5 pF creates a much lower pole and reduces the bandwidth excessively.

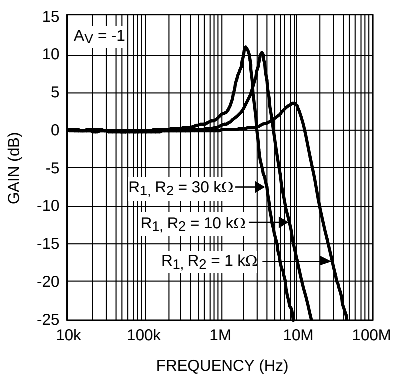


Figure 48. Gain Peaking Caused by Large R_1, R_2

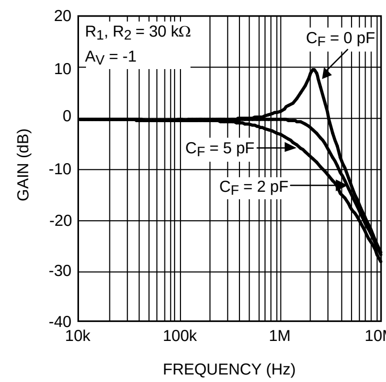


Figure 49. Gain Peaking Eliminated by C_F

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

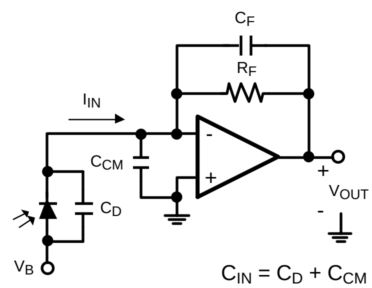
The LMV791 and LMV792 family of amplifiers is specified for operation from 1.8 V to 5.5 V. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

8.2 Typical Applications

These application examples highlight a few of the circuits where the LMV791 and LMV792 may be used.

8.2.1 Transimpedance Amplifier

CMOS input operational amplifiers are often used in transimpedance applications as they have an extremely high input impedance. A transimpedance amplifier converts a small input current into a voltage. This current is usually generated by a photodiode. The transimpedance gain, measured as the ratio of the output voltage to the input current, is expected to be large and wide-band. Because the circuit deals with currents in the range of a few nA, low-noise performance is essential. The LMV79x are CMOS input operational amplifiers providing wide bandwidth and low noise performance, and are hence ideal for transimpedance applications.



$$C_{IN} = C_D + C_{CM}$$

$$\frac{V_{OUT}}{I_{IN}} = -R_F$$

Figure 50. Photodiode Transimpedance Amplifier

8.2.1.1 Design Requirements

Usually, a transimpedance amplifier is designed on the basis of the current source driving the input. A photodiode is a very common capacitive current source, which requires transimpedance gain for transforming its miniscule current into easily-detectable voltages. The photodiode and gain of the amplifier are selected with respect to the speed and accuracy required of the circuit. A faster circuit would require a photodiode with lesser capacitance and a faster amplifier. A more sensitive circuit would require a sensitive photodiode and a high gain. A typical transimpedance amplifier is shown in Figure 50. The output voltage of the amplifier is given by the equation $V_{OUT} = -I_{IN}R_F$. Because the output swing of the amplifier is limited, R_F should be selected such that all possible values of I_{IN} can be detected.

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Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

The LMV79x have a large gain-bandwidth product (17 MHz), which enables high gains at wide bandwidths. A rail-to-rail output swing at 5.5-V supply allows detection and amplification of a wide range of input currents. A CMOS input stage with negligible input current noise and low input voltage noise allows the LMV79x to provide high-fidelity amplification for wide bandwidths. These properties make the LMV79x ideal for systems requiring wide-band transimpedance amplification.

As mentioned earlier, the following parameters are used to design a transimpedance amplifier: the amplifier gain-bandwidth product, A_0; the amplifier input capacitance, C_{CM}; the photodiode capacitance, C_D; the transimpedance gain required, R_F; and the amplifier output swing. Once a feasible R_F is selected using the amplifier output swing, these numbers can be used to design an amplifier with the desired transimpedance gain and a maximally flat frequency response.

An essential component for obtaining a maximally flat response is the feedback capacitor, C_F. The capacitance seen at the input of the amplifier, C_{IN}, combined with the feedback capacitor, R_F, generate a phase lag which causes gain-peaking and can destabilize the circuit. C_{IN} is usually just the sum of C_D and C_{CM}. The feedback capacitor C_F creates a pole, f_P in the noise gain of the circuit, which neutralizes the zero in the noise gain, f_Z, created by the combination of R_F and C_{IN}. If properly positioned, the noise gain pole created by C_F can ensure that the slope of the gain remains at 20 dB/decade till the unity gain frequency of the amplifier is reached, thus ensuring stability. As shown in Figure 51, f_P is positioned such that it coincides with the point where the noise gain intersects the open-loop gain of the operational amplifier. In this case, f_P is also the overall 3-dB frequency of the transimpedance amplifier. The value of C_F needed to make it so is given by Equation 3. A larger value of C_F causes excessive reduction of bandwidth, while a smaller value fails to prevent gain peaking and instability.

$$C_F = \frac{1 + \sqrt{1 + 4\pi R_F C_{IN} A_0}}{2\pi R_F A_0} \tag{3}$$

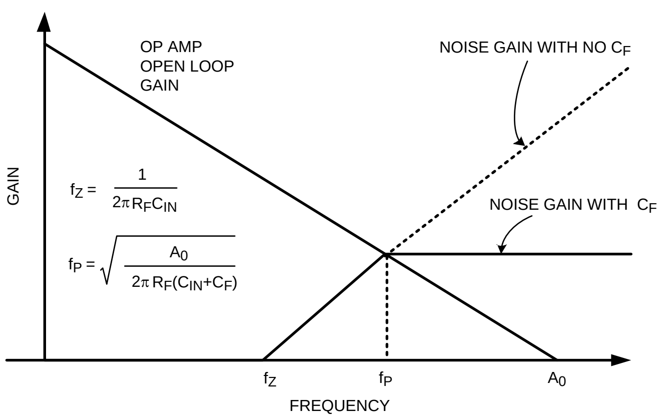

Figure 51. C_F Selection for Stability

Calculating C_F from Equation 3 can sometimes return unreasonably small values (<1 pF), especially for high-speed applications. In these cases, its often more practical to use the circuit shown in Figure 52 in order to allow more reasonable values. In this circuit, the capacitance C_F' is (1+ R_B/R_A) time the effective feedback capacitance, C_F. A larger capacitor can now be used in this circuit to obtain a smaller effective capacitance.

For example, if a C_F of 0.5 pF is needed, while only a 5-pF capacitor is available, R_B and R_A can be selected such that R_B/R_A = 9. This would convert a C_F' of 5 pF into a C_F of 0.5 pF. This relationship holds as long as $R_A < R_F$.

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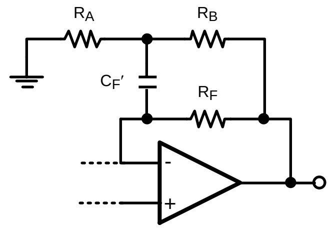
Typical Applications (continued)



$$C_F' = \left(1 + \frac{R_B}{R_A}\right) C_F$$

Figure 52. Obtaining Small C_F from large C_F'

8.2.2 Application Curves

The LMV791 was used to design a number of amplifiers with varying transimpedance gains and source capacitances. The gains, bandwidths and feedback capacitances of the circuits created are summarized in Table 1. The frequency responses are presented in Figure 53 and Figure 54. The feedback capacitances are slightly different from the formula in Equation 3, because the parasitic capacitance of the board and the feedback resistor R_F had to be accounted for.

Table 1. Frequency Response Results

Transimpedance, A_{TI}	C_{IN}	C_F	3-dB Frequency
470000	50 pF	1.5 pF	350 kHz
470000	100 pF	2.0 pF	250 kHz
470000	200 pF	3.0 pF	150 kHz
47000	50 pF	4.5 pF	1.5 MHz
47000	100 pF	6.0 pF	1 MHz
47000	200 pF	9.0 pF	700 kHz

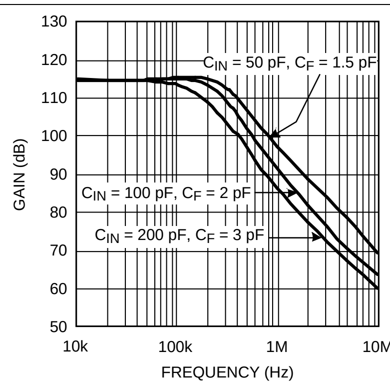


Figure 53. Frequency Response for A_{TI} = 470000

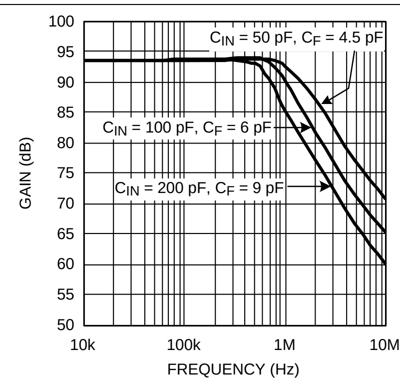
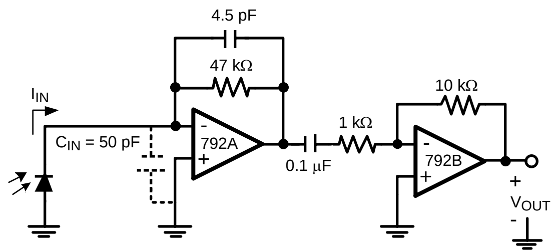


Figure 54. Frequency Response for A_{TI} = 47000

8.2.3 High-Gain, Wideband Transimpedance Amplifier Using the LMV792

The LMV792, dual, low-noise, wide-bandwidth, CMOS input operational amplifier IC can be used for compact, robust and integrated solutions for sensing and amplifying wide-band signals obtained from sensitive photodiodes. One of the two operational amplifiers available can be used to obtain transimpedance gain while the other can be used for amplifying the output voltage to further enhance the transimpedance gain. The wide bandwidth of the operational amplifiers (17 MHz) ensures that they are capable of providing high gain for a wide range of frequencies. The low input referred noise (5.8 nV/$\sqrt{Hz}$) allows the amplifier to deliver an output with a high SNR (signal to noise ratio). The small VSSOP-10 footprint saves space on printed-circuit-boards and allows ease of design in portable products.

The circuit shown in Figure 55, has the first operational amplifier acting as a transimpedance amplifier with a gain of 47000, while the second stage provides a voltage gain of 10. This provides a total transimpedance gain of 470000 with a −3-dB bandwidth of about 1.5 MHz, for a total input capacitance of 50 pF. The frequency response for the circuit is shown in Figure 56



$$A_{TI} = \frac{V_{OUT}}{I_{IN}} = 470{,}000$$

Figure 55. 1.5-MHz Transimpedance Amplifier, With A_{TI} = 470000

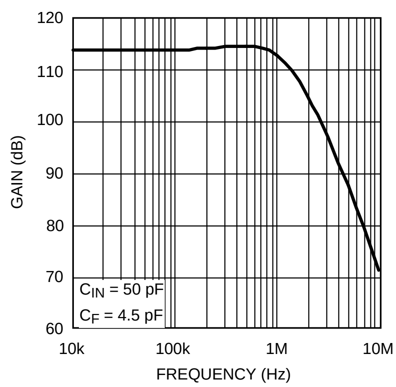


Figure 56. 1.5-MHz Transimpedance Amplifier Frequency Response

8.2.4 Audio Preamplifier With Bandpass Filtering

With low input referred voltage noise, low supply voltage and low supply current, and a low harmonic distortion, the LMV791 family is ideal for audio applications. Its wide unity gain bandwidth allows it to provide large gain for a wide range of frequencies and it can be used to design a preamplifier to drive a load of as low as 600 Ω with less than 0.01% distortion. Two amplifier circuits are shown in Figure 57 and Figure 58. Figure 57 is an inverting amplifier, with a 10-kΩ feedback resistor, R_2, and a 1-kΩ input resistor, R_1, and hence provides a gain of −10. Figure 58 is a noninverting amplifier, using the same values of $R_1$and R_2, and provides a gain of 11. In either of these circuits, the coupling capacitor C_{C1} decides the lower frequency at which the circuit starts providing gain, while the feedback capacitor C_F decides the frequency at which the gain starts dropping off. Figure 59 shows the frequency response of the inverting amplifier with different values of C_F.

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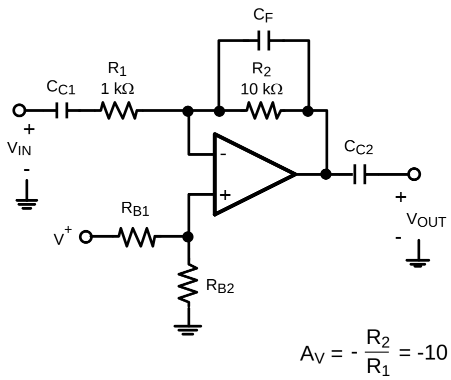

Figure 57. Inverting Audio Preamplifier

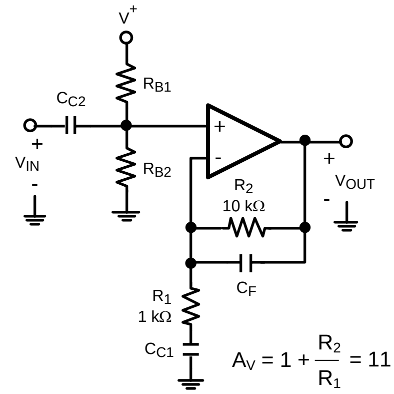

Figure 58. Noninverting Audio Preamplifier

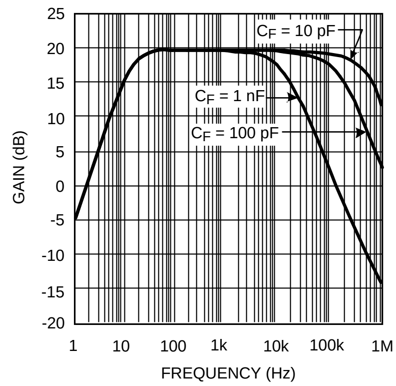

Figure 59. Frequency Response of the Inverting Audio Preamplifier

8.2.5 Sensor Interfaces

The low input bias current and low input referred noise of the LMV791 and LMV792 make them ideal for sensor interfaces. These circuits are required to sense voltages of the order of a few μV, and currents amounting to less than a nA, and hence the operational amplifier needs to have low voltage noise and low input bias current. Typical applications include infrared (IR) thermometry, thermocouple amplifiers and pH electrode buffers. Figure 60 is an example of a typical circuit used for measuring IR radiation intensity, often used for estimating the temperature of an object from a distance. The IR sensor generates a voltage proportional to I, which is the intensity of the IR radiation falling on it. As shown in Figure 60, K is the constant of proportionality relating the voltage across the IR sensor (V_{IN}) to the radiation intensity, I. The resistances R_A and R_B are selected to provide a high gain to amplify this voltage, while C_F is added to filter out the high-frequency noise.

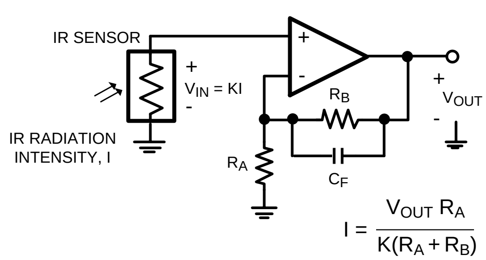

Figure 60. IR Radiation Sensor

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9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, TI recommends that 10-nF capacitors be placed as close as possible to the operational amplifier power supply pins. For single-supply, place a capacitor between V^+ and V^- supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between V^- and ground.

10 Layout

10.1 Layout Guidelines

Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.

Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.

Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.

The ground pin should be connected to the PCB ground plane at the pin of the device.

The feedback components should be placed as close to the device as possible minimizing strays.

10.2 Layout Example

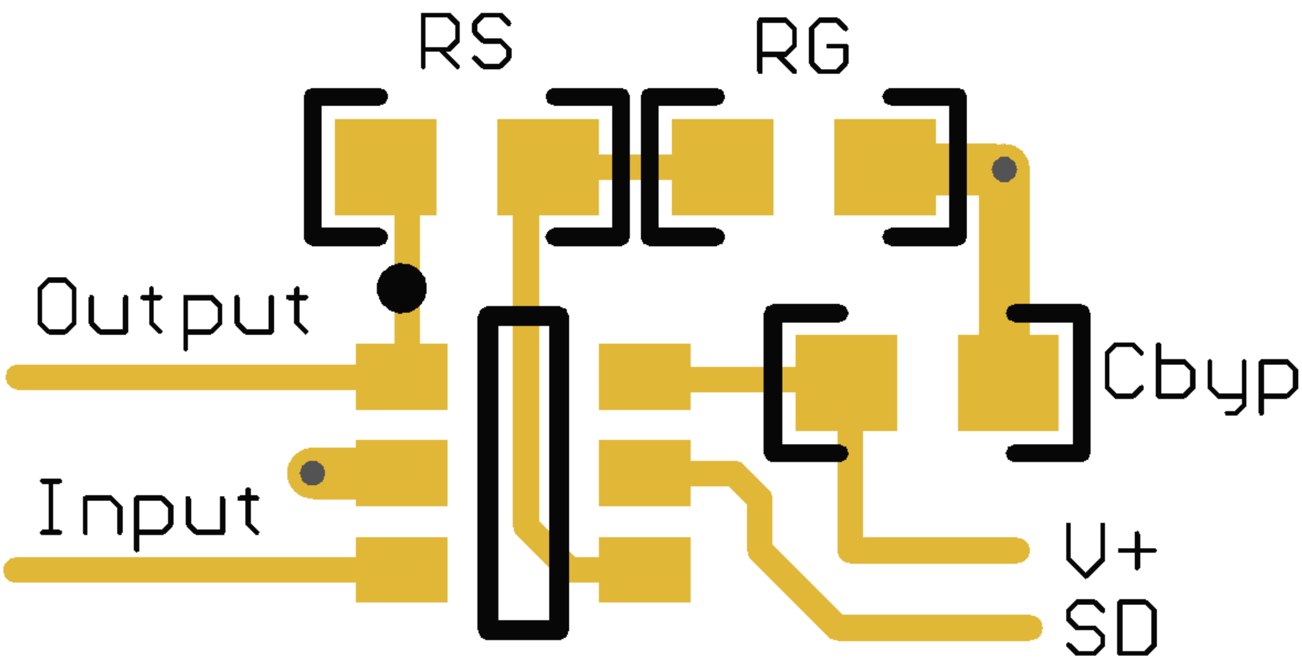

Figure 61. Typical SOT Layout

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For developmental support, see the following:

- LMV791 PSPICE Model, SNOM056
- LMV792 PSPICE Model, SNOM057
- TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti
- DIP Adapter Evaluation Module, http://www.ti.com/tool/dip-adapter-evm
- TI Universal Operational Amplifier Evaluation Module, http://www.ti.com/tool/opampevm
- TI Filterpro Software, http://www.ti.com/tool/filterpro

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *AN-31 Op Amp Circuit Collection*, SNLA140
- *Feedback Plots Define Op Amp AC Performance,* SBOA015 (AB-028)
- *Circuit Board Layout Techniques,* SLOA089
- *Op Amps for Everyone,* SLOD006
- *Capacitive Load Drive Solution using an Isolation Resistor,* TIPD128
- *Handbook of Operational Amplifier Applications,* SBOA092

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV791	Click here	Click here	Click here	Click here	Click here
LMV792	Click here	Click here	Click here	Click here	Click here

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV791MK/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AS1A	Samples
LMV791MKX/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AS1A	Samples
LMV792MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AX2A	Samples
LMV792MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	RoHS & Green	SN	Level-1-260C-UNLIM		AX2A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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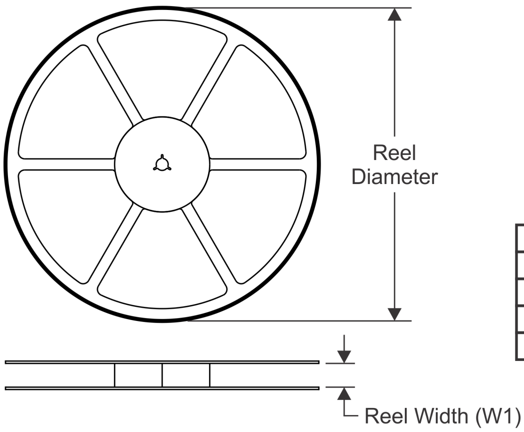
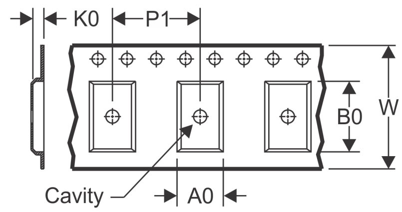
TAPE AND REEL INFORMATION

REEL DIMENSIONS

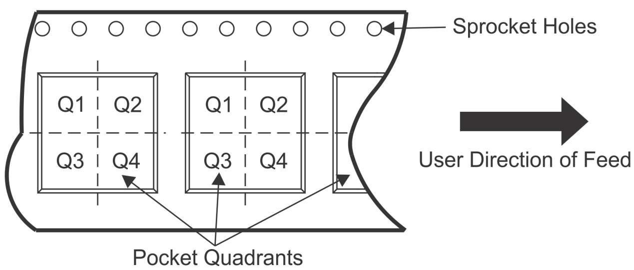


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

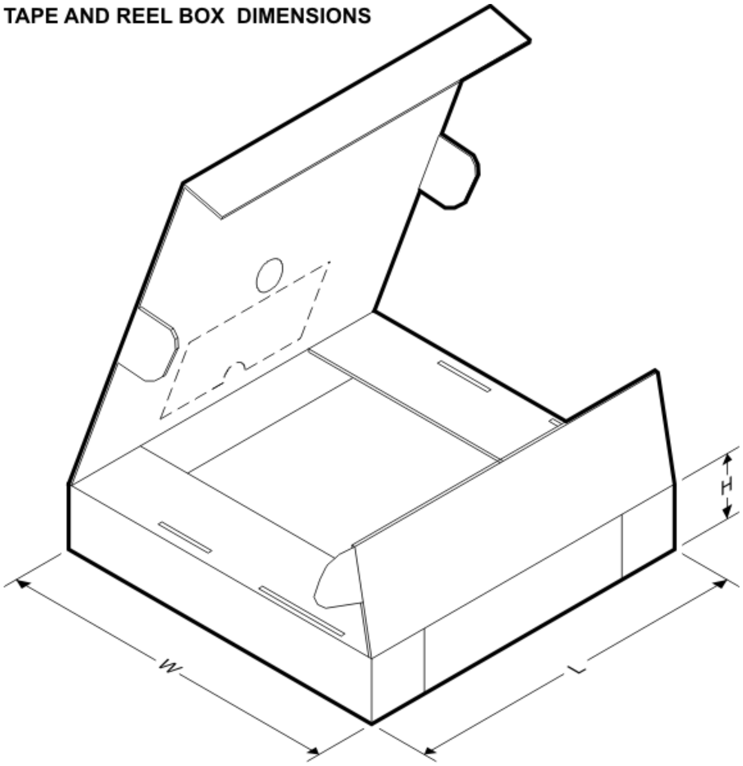
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

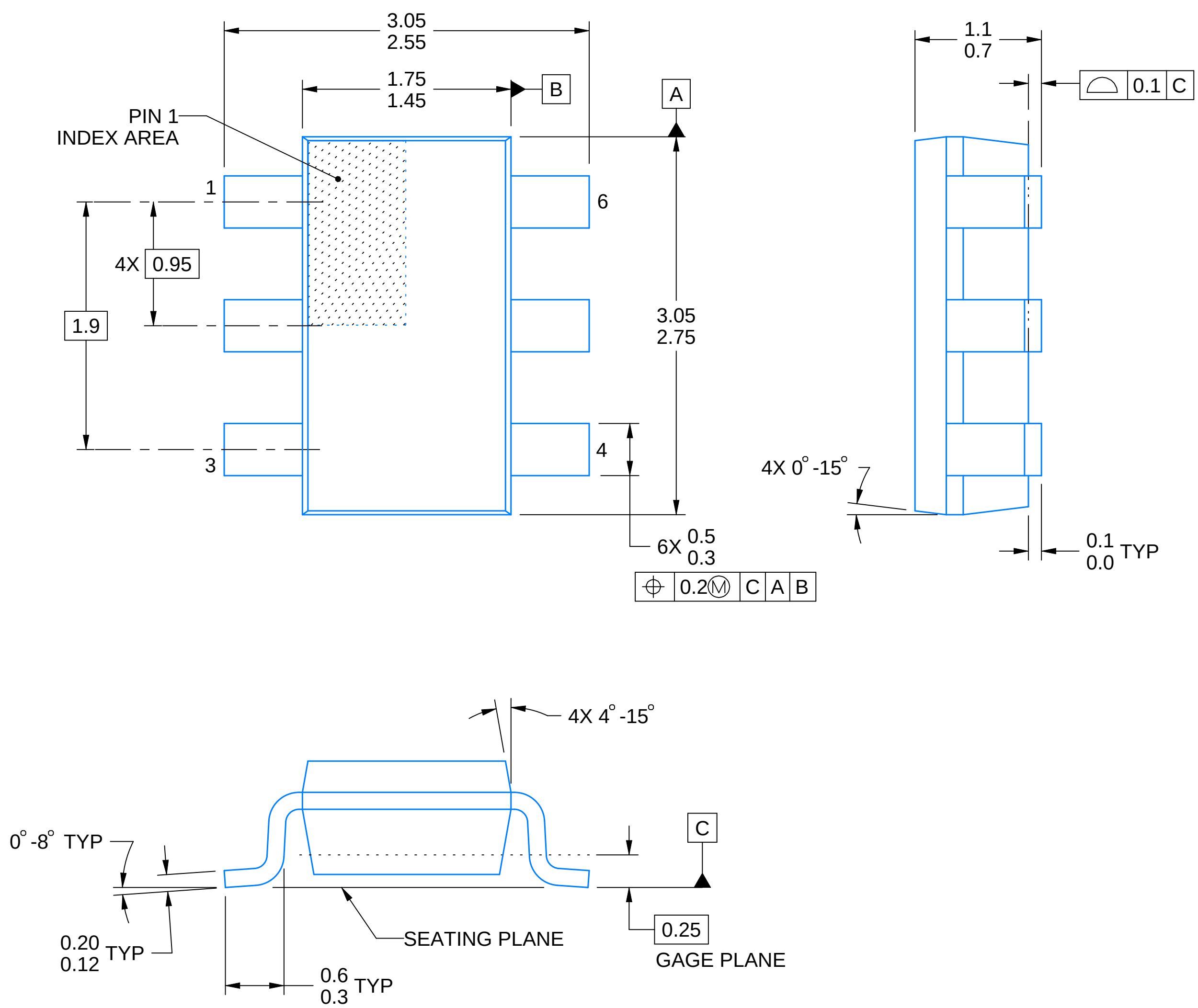
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV791MK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV791MKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV792MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV792MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

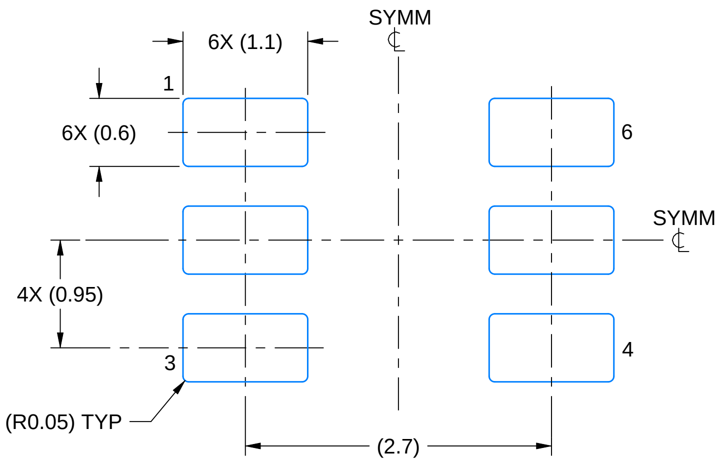
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV791MK/NOPB	SOT-23-THIN	DDC	6	1000	208.0	191.0	35.0
LMV791MKX/NOPB	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LMV792MM/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LMV792MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0



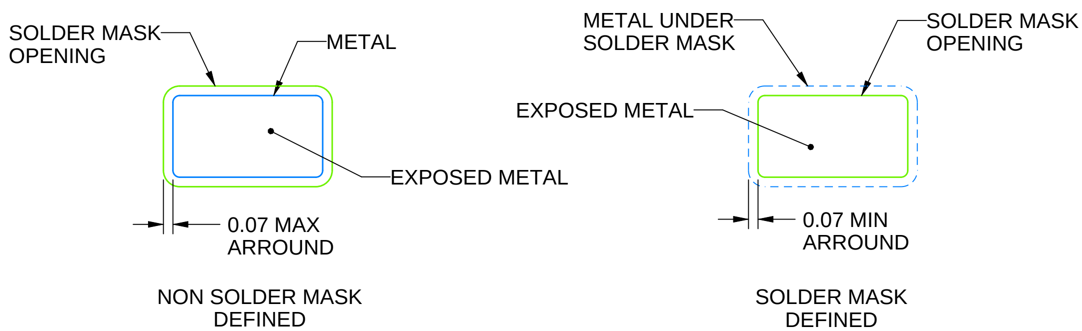
4214841/E 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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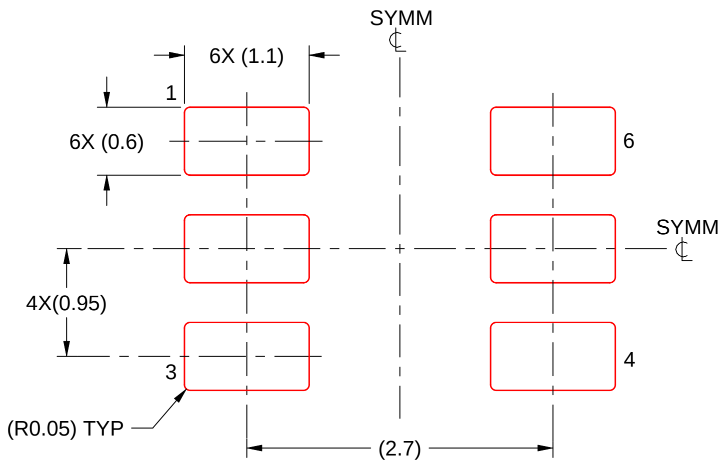
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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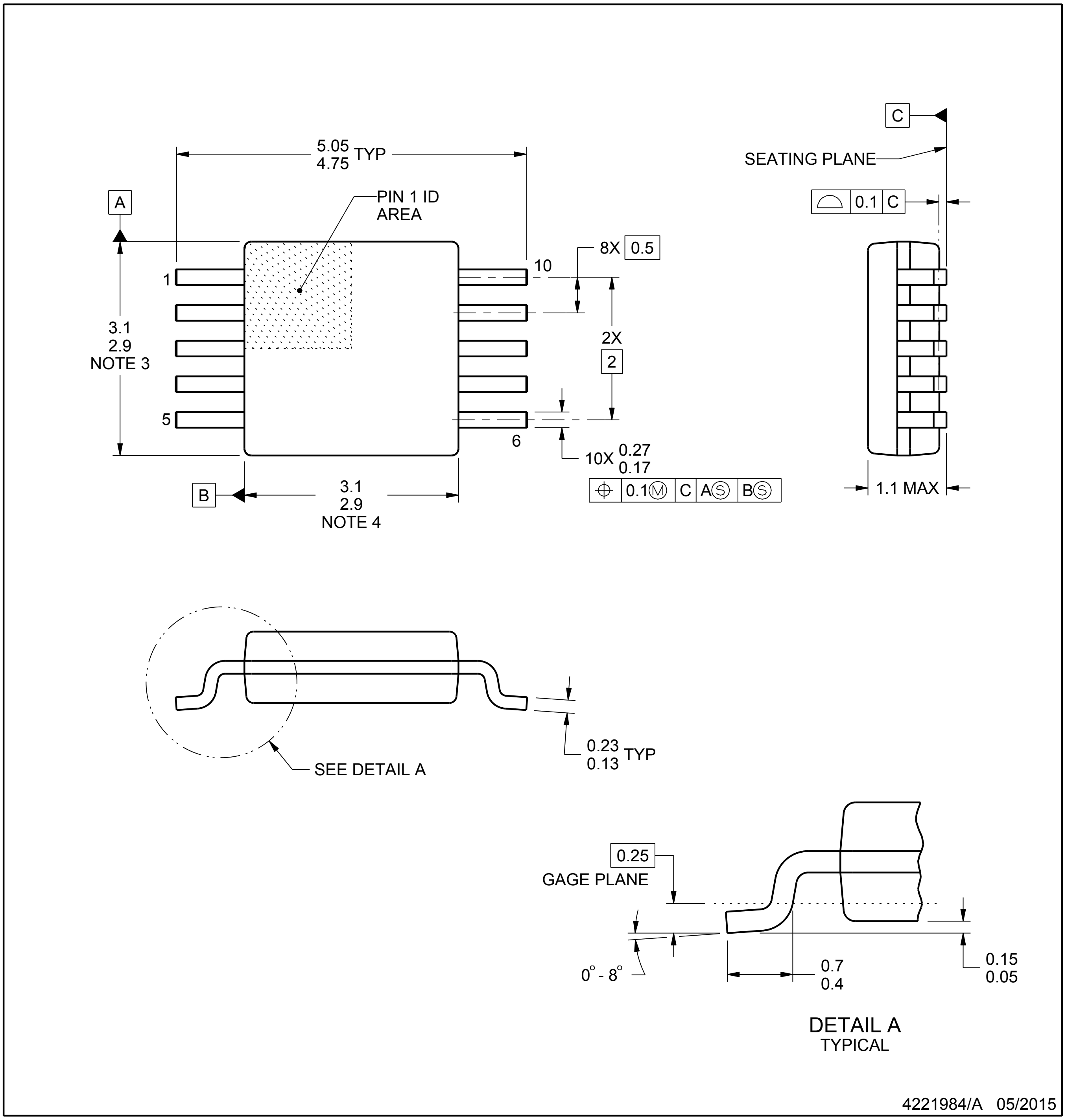
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



NOTES:

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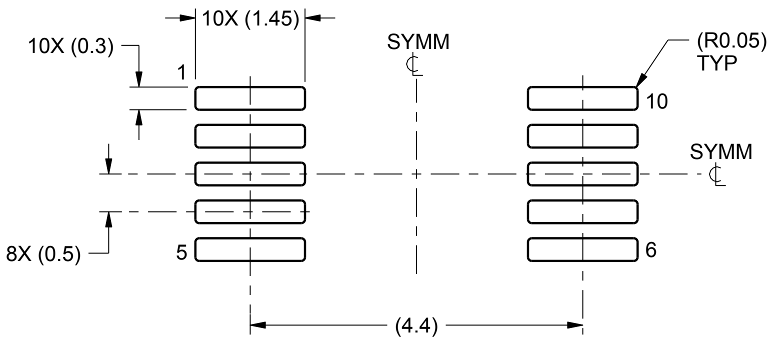
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
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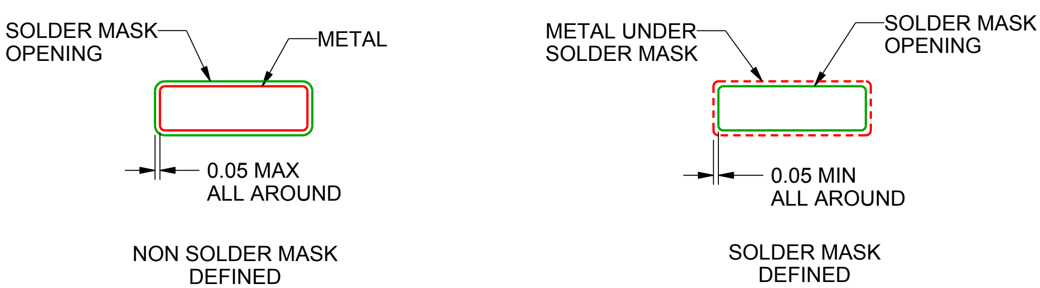

SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

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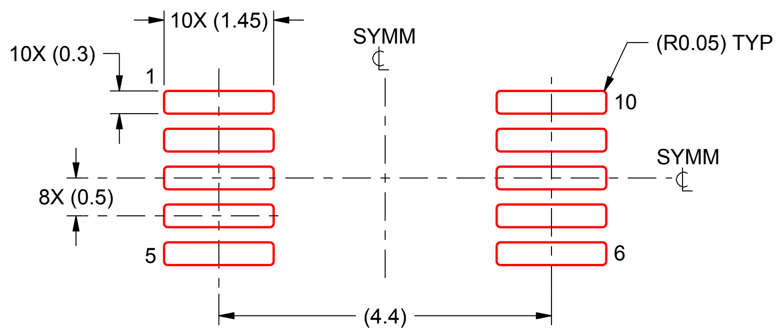

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

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9. Board assembly site may have different recommendations for stencil design.

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