2mbps-200mbps With Signal Loss Detection TTL / CMOS Limiting Amplifier

■ Description

LN1A345 limiting amplifier functions as data quantizer, the amplifier can accept a wide input voltage range and provides TTL/ CMOS output voltage. LN1A345 integrates a power detector, CMOS / TTL signal loss (LOS) output indicates the input power is dropped to the following programmable threshold. Squelch function of the data in the LOS state outputs remain in a static level. SW pin can control the level of high and low quiescent state. LN1A345 work at +5.0 V or +3.3 V single power supply, the working temperature range -40°C to +85°C, provides 16-pin TSSOP package.

■ Features

- High Sensitivity
- Wide bandwidth
- TTL / CMOS output
- Programmable signal loss detection
- Controlable the data output level Squelch level
- 3.3V, 5V compatible

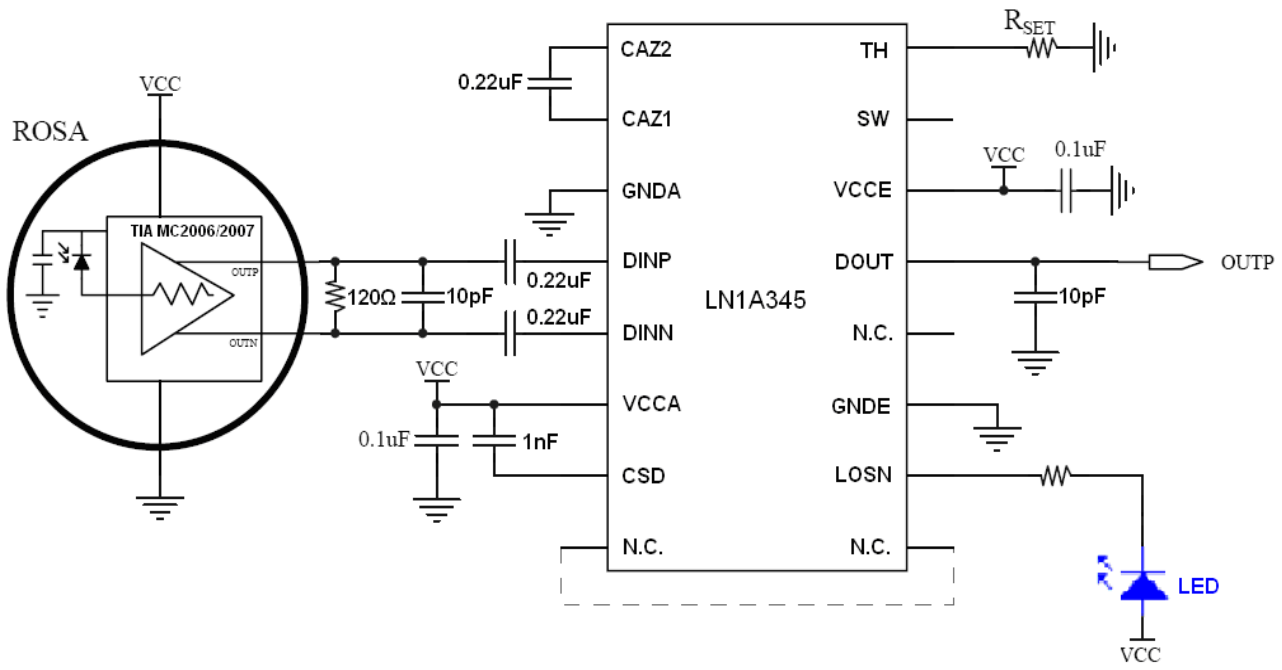
■ Package

- TSSOP-16

■ Applications

- 2Mbps-200Mbps PDH

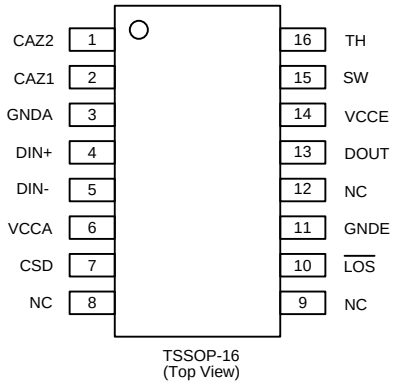
■Typical Operating Circuit



■ Recommended Operating Conditions

Parameter	Symbol	Maximum Rating	Unit
Supply Voltage	V_{cc}	3.0 to 5.5	V
Operating Temperature	T_A	-40 to +85	°C

■ Pin Configuration

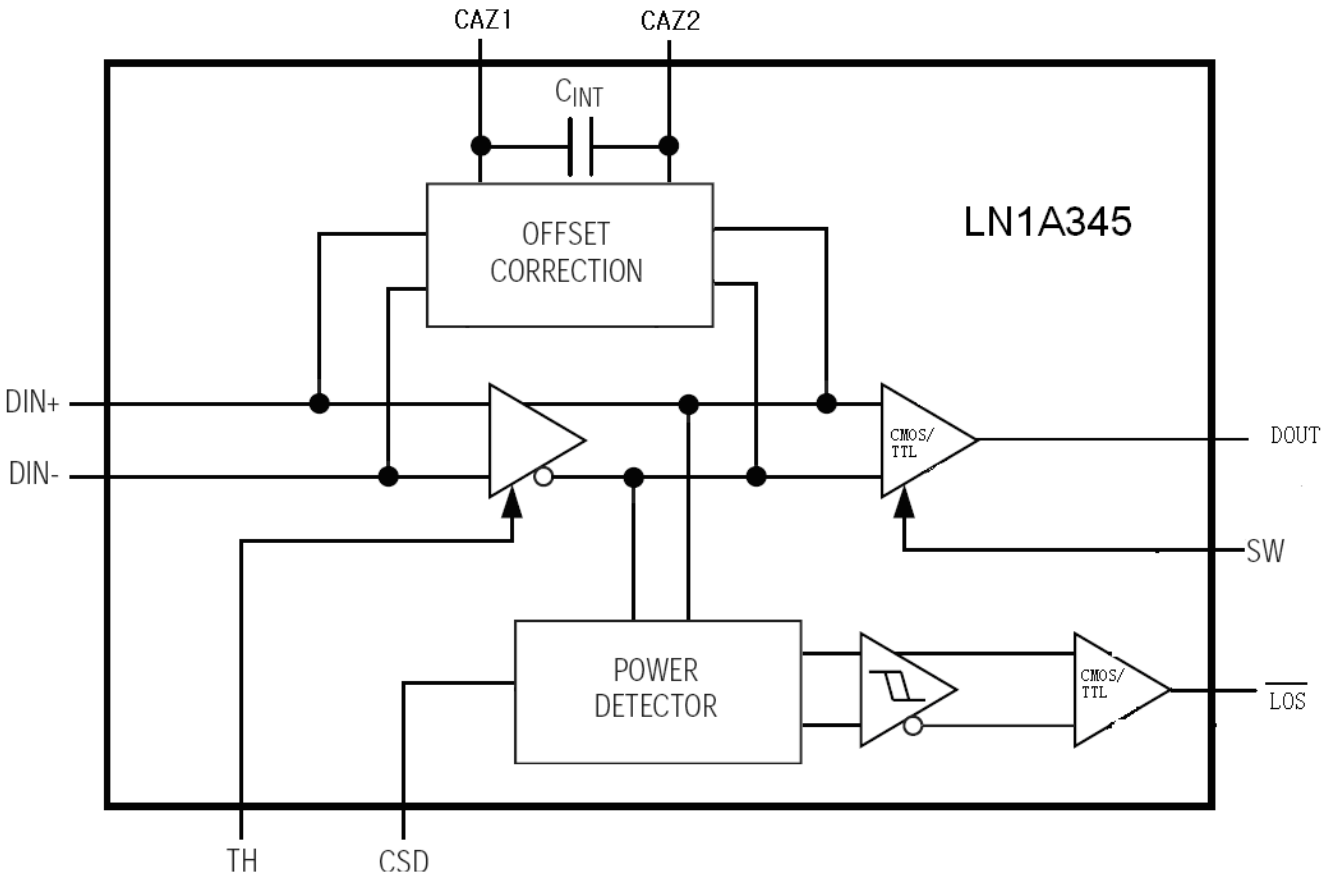


TSSOP-16
(Top View)

■ Pin Assignment

Pin Name	Number	I/o	Function	Pin Name	Number	I/O	Function
CAZ2	1	I	Capacitor of the offset correction loop. A capacitor connected between this pin and CAZ1 sets the time constant of the offset loop. The offset correction is disabled when the CAZ1 and CAZ2 pins are shorted together	CAZ1	2	I	See CAZ2
GNDA	3	-	Analog Ground	DIN+	4	I	Positive data input
DIN-	5	I	Negative data input	VCCA	6	-	+3V to +5.5V Analog Supply Voltage.
CSD	7	I	Level-detect filter capacitor pin. Connect a capacitor between this pin and VCC	N.C.	8	-	No Connection
N.C.	9	-	No Connection	$\overline{\text{LOS}}$	10	O	LOS signal complementary output
GNDE	11	-	Digital Ground	N.C.	12	-	N.C.
DOUT	13	O	Negative data output, CMOS /TTL level	VCCE	14	-	+3V to +5.5V Digital Supply Voltage. Must be at the same potential as the VCCA pin
SW	15	I	SW as the switch pin of high and low when the output is off. When SW is low, the output is high when off; when SW is high, the output is low when off. SW default is high	TH	16	I	Loss-of-Signal Threshold Pin. Resistor (RSET) to ground sets the LOS threshold.

■ Block Diagram



■ Absolute Maximum Rating

Parameter	Symbol	Maximum Rating	Unit
Supply voltage	V_{cc}	-0.3 to 6	V
Input differential voltage (Vin1,Vin2)	V_{in}	-0.3 to 6	V
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Pin temperature	T_{Lead}	300	°C
Junction temperature	T_{jmax}	150	°C
ESD Susceptibility	-	>2000	V

■ Electrical Specifications

(VCC= +4.5V to +5.5V, TA = -40°C to +85°C. Unless otherwise noted, typical values are at VCC = +5V/3.3V and TA = +25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply						
Quiescent Current	ICC	3.3V		18		mA
Quiescent Current	ICC	5V		21		mA
Input Specifications （Note1,2）						
Input Resistance	RIN			4		kΩ
Input Sensitivity RTH=100ohm	VIN-MIN	Single ended		0.3	1	mVP-P
		Differential		0.6	2	
Input Overload RTH=100ohm	VIN-MAX	Single ended		2		VP-P
		Differential		4		
Input-Referred Offset Voltage				8		μV
Input Common-Mode Voltage	VCMM			2.82@3.3		V
				4.28@5		
Output Specifications						
3.3V						
CMOS/TTL Output-Voltage High		I_{OH}=15.3mA	2.4			V
CMOS/TTL Output-Voltage Low		I_{OL}=10mA			0.2	V
Data Output Transition Time	tR	10% to 90% (Notes 1, 2,7)			2	ns
	tF	10% to 90% (Notes 1, 2,7)			1.2	ns
Duty Cycle					52%	
5V						
CMOS/TTL Output-Voltage High		I_{OH}=50mA	3.0			V
CMOS/TTL Output-Voltage Low		I_{OL}=10mA			0.2	V
Data Output Transition Time	tR	10% to 90% (Notes 1, 2)			2	ns
	tF	10% to 90% (Notes 1, 2)			1.2	ns
Duty Cycle					49%	
Transfer Characteristics						
3.3V						
Bandwidth		LA CORE	70	100	140	MHz
Low-Frequency Cutoff		CAZ = 0.22u	0.2	0.3	0.5	kHz
5V						
Bandwidth		LA CORE	70	105	150	MHz
Low-Frequency Cutoff		CAZ = 0.22u	0.3	0.4	0.6	
Loss-Of-Signal Specifications (Notes 2，6) +3.3V Supply						
LOS Sensitivity Range		100Ω ≤ RTH ≤ 732Ω	2		20	mVP-P
LOS Hysteresis		20log (VDEASSERT/VASSERT)	2	4	6	dB
Loss-Of-Signal Specifications (Notes 2，6) +5V Supply						
LOS Sensitivity Range		138Ω ≤ RTH ≤ 1050Ω	2		20	mVP-P
LOS Hysteresis		20log (VDEASSERT/VASSERT)	2	4	6	

Note 1: Rset=100Ω. 100Mbps PRBS, 3.3V

Note 2: Guaranteed by design and characterization.

Note 3: Noise is derived from BER measurement.

Note 4: MAX value is simulated with All case and worst case Mismatch.

Note5: PWD = [(width of wider pulse) - (width of narrower pulse)] / 2, measured with 156.25Mbps 0011 pattern.

Note6: Simulation case includes TEMP, MOSFET, SUPPLY and RESISTOR.

Note7: 10p loaded, 50Mbps 0101

■ Electrical Specifications

LN1A345 is composed of the gain stage, offset calibration, power detector, LOS indicator, and TTL / CMOS output buffers.

- **Data input**

Data input single-ended input impedance 4kΩ, provided by the internal DC bias. AC coupling capacitors required by the external data signals. General applications, the input coupling capacitor Cin is 0.22uF, to further increase the Cin and CAZ, can make LN1A345 work in very low frequency.

- **Gain and offset calibration**

The limiting amplifier provides the gain nearly 74dB (RTH = 100Ω). The large signal gain of the amplifier vulnerable to the impact of channel DC offset. For DC offset calibration, the amplifier introduces an internal feedback loop, through the DC offset correction, limiting amplifier greatly improved receiver sensitivity and power detector accuracy. Automatic zero external capacitance (CAZ), determine the DC offset calibration circuit time constant. CAZ = 0.22μF (recommended value), the signal path-3dB cutoff frequency is typically 0.4kHz.

- **power detector and LOS indicator**

RTH external resistor sets the first level of gain limiting amplifier. The detector gain setting power to judge the situation occurred LOS threshold. Power detection data signals through the rectifier and low pass filter implementation, rectification, filtering and signal re-programming the threshold voltage for comparison. 2dB hysteresis to prevent output of the input signal close to the LOS threshold appears chirp.

- **TTL / CMOS output**

LN1A345 with TTL / CMOS output, direct drive 74AHCT00 gate-level circuit. Squelch, the output to maintain a static level, and can be controlled by the SW level of the static level.

- **CMOS / TTL Output**

Output is CMOS / TTL compatible output. LOS detection of the signal driving LEDs. If the output does not need LOS, then the pin can no connect.

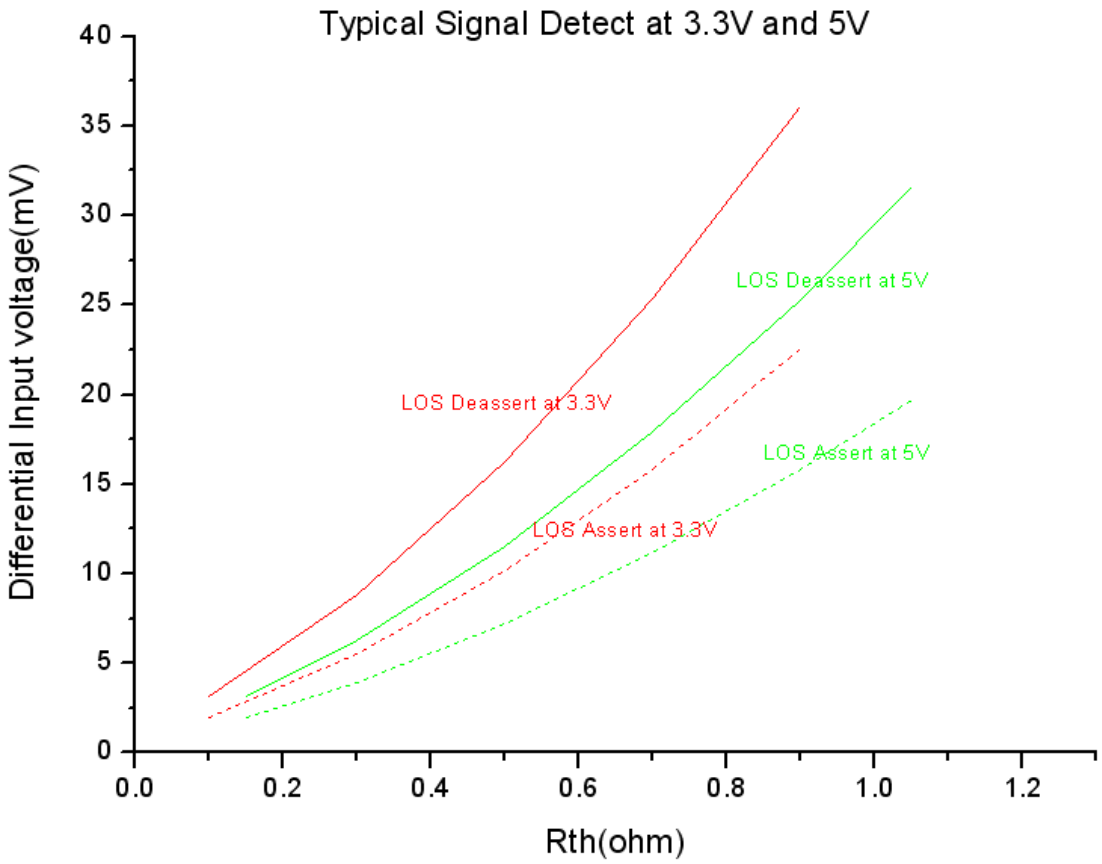
■ Application Information

- **Set LOS alarm / disarm the alarm level**

  RTH appropriate values can work in accordance with the typical characteristics of the Loss-Of-Signal Threshold vs. RTH curve to determine

- **LOS time constant**

  Power monitor low-pass filter contains a chip resistor (RSD) and an external capacitor (CSD). CSD capacitor value determines the time constant of the power monitor, the time constant decided LOS alarm / disarm the alarm time value can provide a long enough time constant to eliminate the error caused some changes in factors that trigger



LOS THRESHOLD vs. RTH

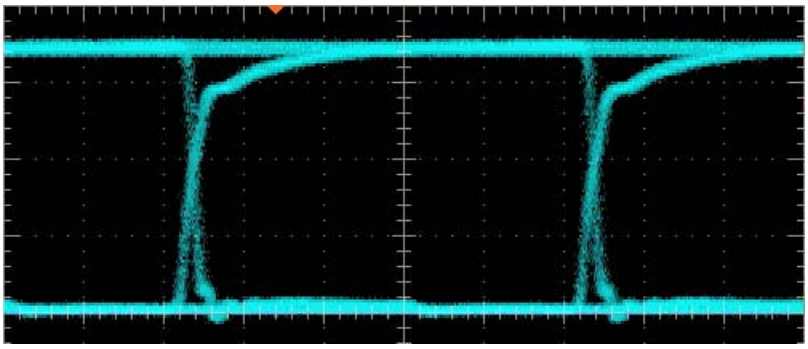
■ Typical Operating Characteristics

Test conditions: 1x9 Optical Module + ROSA + LDD + STARPAN-3 START BOARD

(STARPAN-3 START BOARD: pseudo-random code generator, LDD: Jiangsu Xin-zhi SC1D501, Wuhan Qi Sheng provide ROSA:-38dBm sensitivity, output: 50 ohms resistance to ground the oscilloscope)

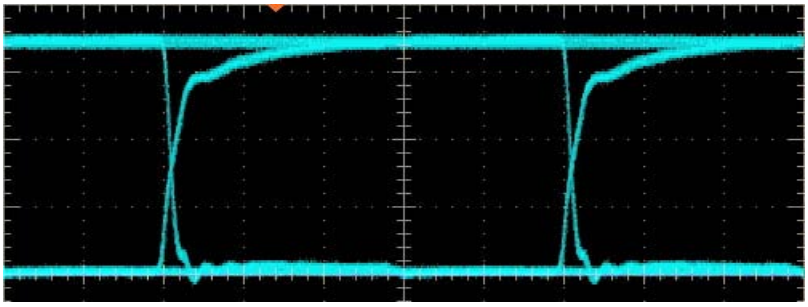
OUT EYE DIAGRAM

(VCC=3.3V，Optical Input =-38dBm，50Mbps)



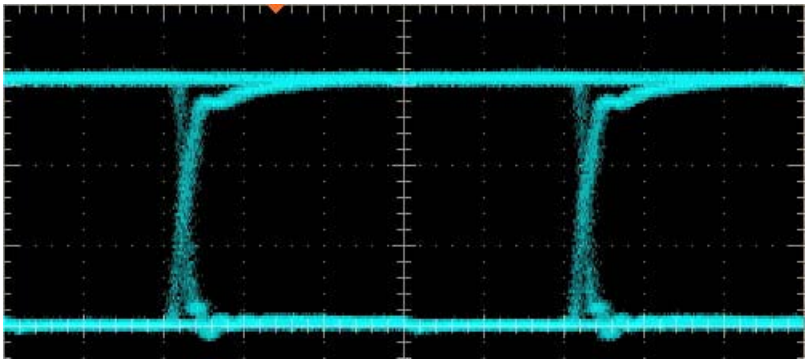
OUT EYE DIAGRAM

(VCC=3.3V，Optical Input =-10dBm，50Mbps)



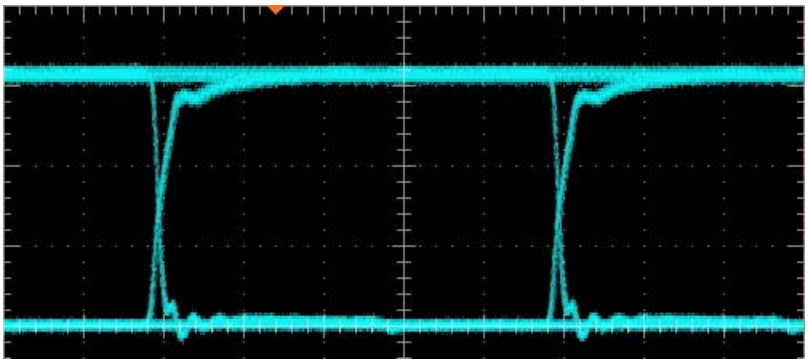
OUT EYE DIAGRAM

(VCC=5V，Optical Input =-38dBm，50Mbps)



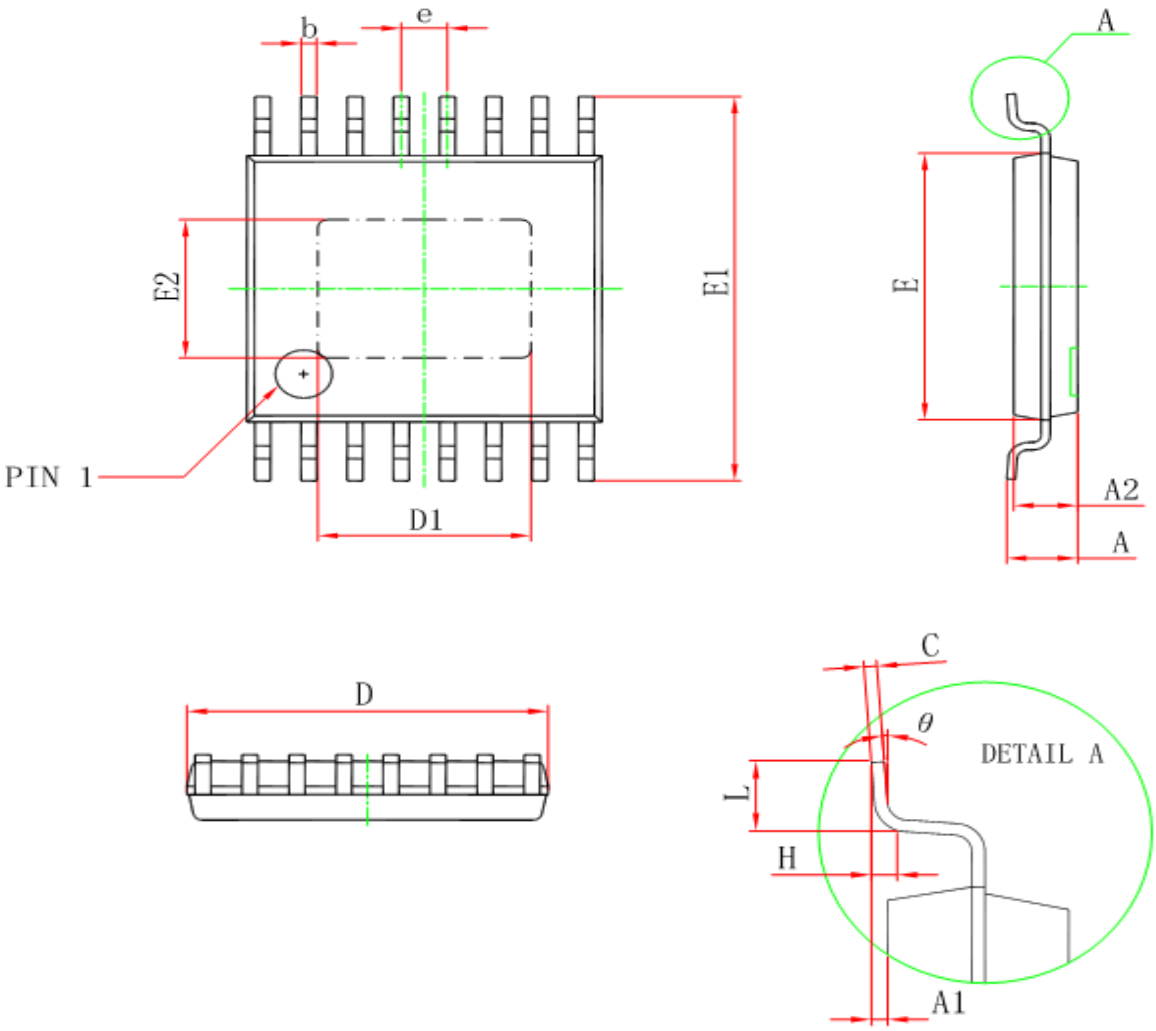
OUT EYE DIAGRAM

(VCC=5V，Optical Input =-10dBm，50Mbps)



■ Package Information

- **TSSOP-16/PP**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	4.900	5.100	0.193	0.201
D1	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
E2	2.200	2.400	0.087	0.094
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.02	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°