Sensorless CC/CV Step-Down DC/DC Converter

■ General Description

LN2065 is a wide input voltage, high efficiency step-down DC/DC converter that operates in either CV (Constant Output Voltage) mode or CC(Constant Output Current) mode. LN2065 provides up to 3.5A output current at 125kHz switching frequency.

LN2065 integrates control scheme to achieve high-accuracy constant current control without the expensive, high accuracy current sense resistor. It also integrates adaptive gate drive to achieve excellent EMI performance passing EN55022 Class B EMC standard without adding additional EMI components while maintaining high conversion efficiency.

Protection features include cycle-by-cycle current limit, thermal shutdown, and frequency foldback at short circuit.

LN2065 are available in ESOP package and require very few external devices for operation.

■ Applications

- Car Charger/ Adaptor
- General-Purpose CV/CC Power Supply
- Rechargeable Portable Devices

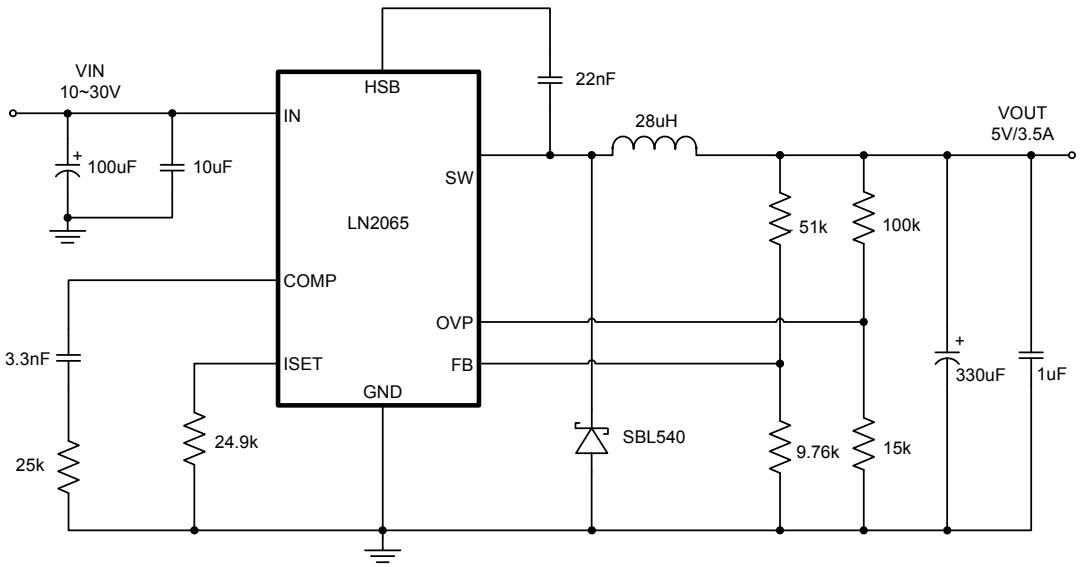
■ Features

- Up to 3.5A output current
- 125kHz Switching Frequency Eases EMI Design
- 91% Efficiency (Vout=5V@2.4A at Vin=12V)
- Resistor Programmable for Output Cable Drop Compensation
- Cycle-by-Cycle Current Limit, Output Over Voltage Protect, Thermal Shutdown, Input Under Voltage Lockout
- Integrated Soft Start
- ±7.5% CC Accuracy
- ±2% CV Accuracy
- High-Side Rdson 50mΩ

■ Package

- ESOP8

■ Typical Application



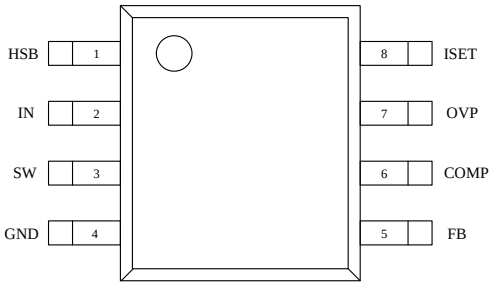
■ Ordering Information

LN2065 ①②

Item	Symbol	Description
①	Package	
	S	Packaging Types: ESOP8
②	Device Orientation	
	R	Embossed tape: Standard feed
	L	Embossed tape: Reverse feed

■ Pin Assignment

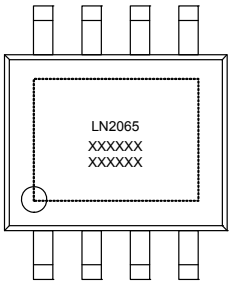
ESOP8
(TOP VIEW)



■ Pin Function

Pin	Name	Function
1	HSB	High Side Bias Pin. This provides power to the internal high-side MOSFET gate driver. Connect a 22nF capacitor from HSB pin to SW pin.
2	IN	Power Supply Input. Bypass this pin with a 10μF ceramic capacitor to GND, placed as close to the IC as possible.
3	SW	Power Switching Output to External Inductor.
4	GND	Ground. Connect this pin to a large PCB copper area for best heat dissipation. Return FB, COMP, and ISET to this GND, and connect this GND to power GND at a single point for best noise immunity.
5	FB	Feedback Input. The voltage at this pin is regulated to 800mV. Connect to the resistor divider between output and GND to set the output voltage.
6	COMP	Error Amplifier Output. This pin is used to compensate the converter.
7	OVP	OVP input. If the voltage at this pin exceeds 0.8V, the IC shuts down high side switch. There is a 2μA pull-up current at this pin.
8	ISET	Output Current Setting Pin. Connect a resistor from ISET to GND to program the output current.
	Exposed Pad	Heat Dissipation Pad. Connect this exposed pad to large ground copper area with copper and vias.

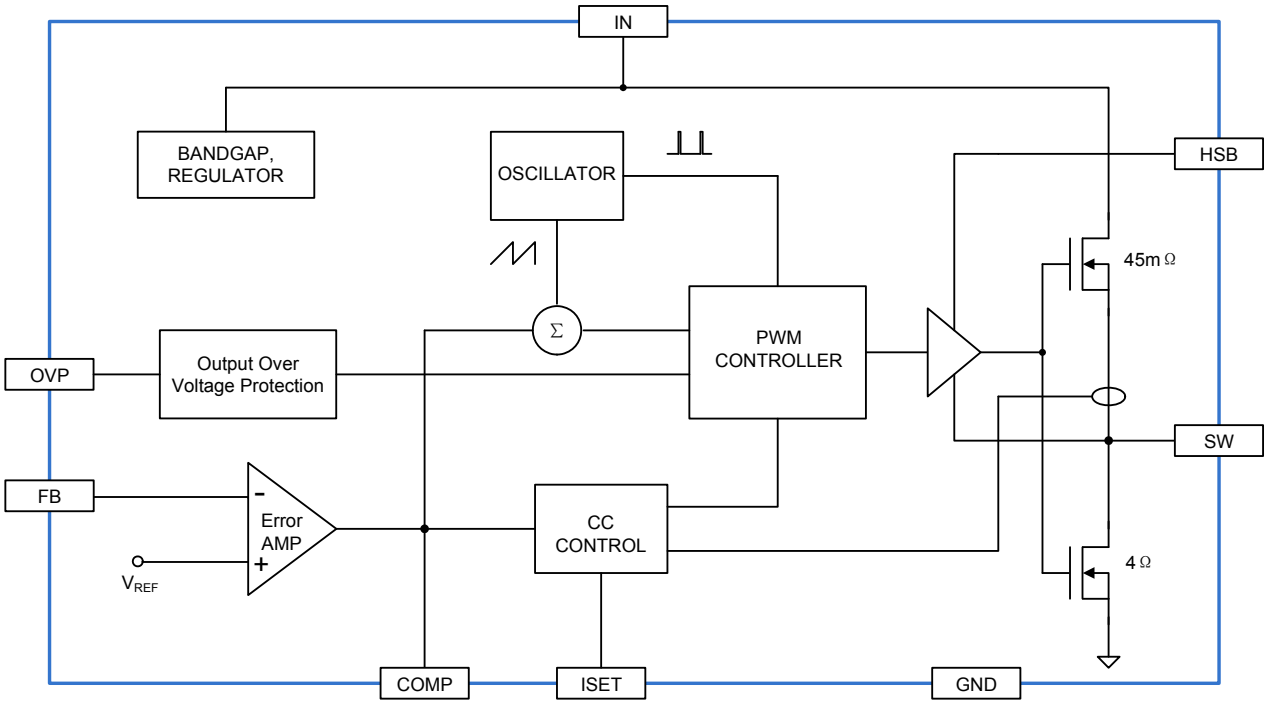
■ Marking Rule



ESOP8

The first row represents the product name LN2065. The second row represents the internal version. The third row represents the lot number, wafer number and other information.

■ Function Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Maximum Rating	Unit
IN to GND	Vin	-0.3 to 32	V
SW to GND		-1 to VIN+1	V
HSB to GND	V_{GATE}	VSW-0.3 to VSW+7	V
FB, ISET, COMP to GND	I_{VIN}	-0.3 to 6	V
Storage temperature range	T_{STG}	-40 to 150	℃
Operating junction temperature	T_J	-40 to 150	℃
ESD Human Model		4000	V

■ Electrical Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Input Voltage		10		30	V
Input Voltage Surge				32	V
VIN UVLO Turn-On Voltage	Input Voltage Rising	9.0	9.3	9.7	V
VIN UVLO Hysteresis	Input Voltage Falling		1.1		V
Standby Supply Current	VFB=1V		0.88	1.4	mA
Feedback Voltage		785	800	815	mV
Internal Soft-Start Time			500		μs
Error Amplifier Transconductance	VFB=VCOMP=0.8V ΔICOMP=±10μA		650		μA/V
Error Amplifier DC Gain			4000		V/V
Switching Frequency	VFB=0.8V		125		kHz
Foldback Switching Frequency	VFB=0V		18		kHz
Maximum Duty Cycle			85		%
Minimum On-Time			300		ns
COMP to Current Limit Transconductance	VCOMP=1.7V		3.47		A/V
Secondary Cycle-by-Cycle Current Limit			6.4		A
Slope Compensation	Duty=DMAX		3		A
ISET Voltage			1		V
ISET to IOUT DC Room Temp Current Gain	IOUT/ISET，RISET=25kΩ		100000		A/A
CC Controller DC Accuracy	RISET=24.9kΩ, VOUT=4.0V		3600		mA
OVP Pin Lock Voltage	OVP Pin Voltage Rising		0.833		V
OVP Pin Unlock Voltage	OVP Pin Voltage Falling		0.764		V
High-Side Switch ON-Resistance	Not Include Bonding Wire		45		mΩ
Thermal Shutdown Temperature	Temperature Rising		151		℃
Thermal Shutdown Temperature Hysteresis	Temperature Falling		22		℃

■ Application Information

● CV/CC Loop Regulation

As seen in Function Block Diagram, the LN2065 is a peak current mode pulse width modulation (PWM) converter with CC and CV control. The converter operates as follows:

A switching cycle starts when the falling edge of the Oscillator clock output causes the High-Side Power Switch to turn on and the Low-Side Power Switch to turn off. With the SW side of the inductor now connected to IN, the inductor current ramps up to store energy in the magnetic field. The inductor current level is measured by the Current Sense Amplifier and added to the Oscillator ramp signal. If the resulting summation is higher than the COMP voltage, the output of the PWM Comparator goes high. When this happens or when Oscillator clock output goes high, the High-Side Power Switch turns off.

At this point, the SW side of the inductor swings to a diode voltage below ground, causing the inductor current to decrease and magnetic energy to be transferred to output. This state continues until the cycle starts again. The High-Side Power Switch is driven by logic using HSB as the positive rail. This pin is charged to VSW+5V when the Low-Side Power Switch turns on. The COMP voltage is the integration of the error between FB input and the internal 0.8V reference. If FB is lower than the reference voltage, COMP tends to go higher to increase current to the output. Output current will increase until it reaches the CC limit set by the ISET resistor. At this point, the device will transition from regulating output voltage to regulating output current, and the output voltage will drop with increasing load. The Oscillator normally switches at 125kHz. However, if FB voltage is less than 0.6V, then the switching frequency decreases until it reaches a typical value of 18kHz at VFB = 0.15V.

● Over Voltage Protection

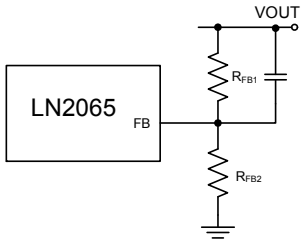
The LN2065 has an OVP pin. If the voltage at this pin exceeds 0.8V, the IC shuts down high-side switch. There is a 2μA pull-up current at this pin.

● Thermal Shutdown

The LN2065 disables switching when its junction temperature exceeds 151℃ and resumes when the temperature has dropped by 22℃.

● Output Voltage Setting

The figure shows the connections for setting the output voltage.

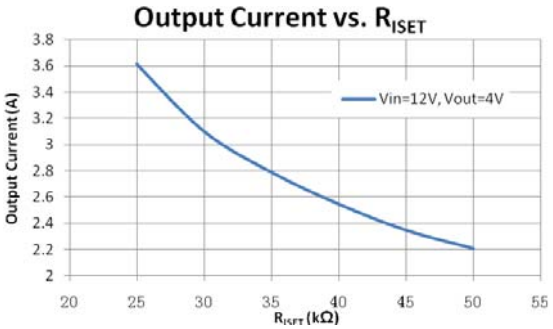


Select the proper ratio of the two feedback resistors R_{FB1} and R_{FB2} based on the output voltage. Adding a capacitor in parallel with R_{FB1} helps the system stability. Typically, use R_{FB2}≈10kΩ and determine RFB1 from the following equation:

$$R_{FB1} = R_{FB2}\left(\frac{V_{OUT}}{0.8V} - 1\right)$$

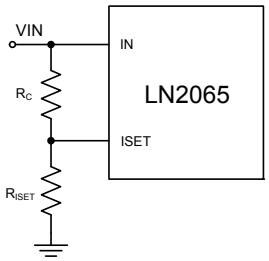
● CC Current Setting

LN2065 constant current value is set by a resistor connected between the ISET pin and GND. The CC output current is linearly proportional to the current flowing out of the ISET pin. The voltage at ISET is roughly 1V and the current gain from ISET to output is roughly 100000 (100mA/1μA). To determine the proper resistor for a desired current, please refer to figure below.



● CC Current Line Compensation

When operating at constant current mode, the current limit increase slightly with input voltage. For wide input voltage applications, a resistor R_C may be added to compensate line change and keep output high CC accuracy, as shown figure below.



- **Inductor Selection**

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value.

Higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{LOADMAX} \times K_{RIPPLE}}$$

Where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, $I_{LOADMAX}$ is the maximum load current, and K_{RIPPLE} is the ripple factor. Typically, choose K_{RIPPLE}=30% to correspond to the peak-to-peak ripple current being 30% of the maximum load current.

With a selected inductor value the peak-to-peak inductor current is estimated as:

$$I_{LPK-PK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times V_{IN} \times f_{SW}}$$

The peak inductor current is estimated as:

$$I_{LPK} = I_{LOADMAX} + \frac{1}{2} I_{LPK-PK}$$

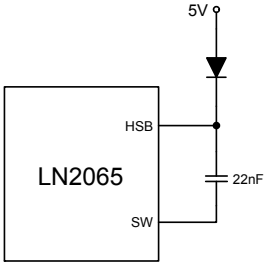
The selected inductor should not saturate at I_{LPK}. The maximum output current is calculated as:

$$I_{OUTMAX} = I_{LIM} - \frac{1}{2} I_{LPK-PK}$$

I_{LIM} is the internal current limit, which is typically 5.4A, as shown in Electrical Characteristics Table.

- **External High Voltage Bias Diode**

It is recommended that an external High Voltage Bias diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The High Voltage Bias diode can be a low cost one such as IN4148 or BAT54, as figure shown below.



This diode is also recommended for high duty cycle operation and high output voltage applications.

- **Input Capacitor**

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 10μF. The best choice is the ceramic type, however, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and G pins of the IC, with the shortest traces possible. In the case of tantalum or electrolytic types, they can be further away if a small parallel 0.1μF ceramic capacitor is placed right next to the IC.

- **Output Capacitor**

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{OUTMAX} \times K_{RIPPLE} \times R_{ESR} + \frac{V_{IN}}{28 \times f_{SW}^{\ 2} LC_{OUT}}$$

Where I_{OUTMAX} is the maximum output current,

K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR of the output capacitor, f_{SW} is the switching frequency, L is the inductor value, and C_{OUT} is the output capacitance. In the case of ceramic output capacitors, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic capacitors, the ripple is dominated by R_{ESR} multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

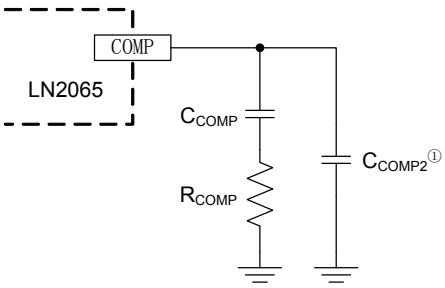
For ceramic output capacitor, typically choose a capacitance of about 22μF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50mΩ ESR.

- **Rectifier Diode**

Use a Schottky diode as the rectifier to conduct current when the High-Side Power Switch is off. The Schottky diode must have current rating higher than the maximum output current and a reverse voltage rating higher than the maximum input voltage.

- **Stability Compensation**

The feedback loop of the IC is stabilized by the components at the COMP pin, as shown in figure below.



NOTE ①: C_{COMP2} is needed only for high ESR output capacitor

The DC loop gain of the system is determined by the following equation:

$$A_{VDC} = \frac{0.8V}{I_{OUT}} \times A_{VEA} \times G_{COMP}$$

The dominant pole P1 is due to C_{COMP}:

$$f_{P1} = \frac{G_{EA}}{2\pi A_{VEA} C_{COMP}}$$

The second pole P2 is the output pole:

$$f_{P2} = \frac{I_{OUT}}{2\pi V_{OUT} C_{OUT}}$$

The first zero Z1 is due to R_{COMP} and C_{COMP}:

$$f_{Z1} = \frac{1}{2\pi R_{COMP} C_{COMP}}$$

And finally, the third pole is due to R_{COMP} and C_{COMP2} (if C_{COMP2} is used):

$$f_{P3} = \frac{1}{2\pi R_{COMP} C_{COMP2}}$$

The following steps should be used to compensate the IC:

STEP 1. Set the cross over frequency at 1/10 of the switching frequency via R_{COMP}:

$$R_{COMP} = \frac{2\pi V_{OUT} C_{OUT} f_{SW}}{10 G_{EA} G_{COMP} \times 0.8V}$$
$$= 5.17 \times 10^7 V_{OUT} C_{OUT} .....(\Omega)$$

STEP 2. Set the zero fZ1 at 1/4 of the cross over frequency. If R_{COMP} is less than 15kΩ, the equation for C_{COMP} is:

$$C_{COMP} = \frac{2.83 \times 10^5}{R_{COMP}} .....(F)$$

If R_{COMP} is limited to 15kΩ, then the actual cross over frequency is 6.58 / ($V_{OUT}C_{OUT}$). Therefore:

$$C_{COMP} = 6.45 \times 10^{-6} V_{OUT} C_{OUT} .....(F)$$

STEP 3. If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the cross over frequency, an additional compensation capacitor C_{COMP2} is required. The condition for using C_{COMP2} is:

$$R_{ESRCOUT} \geq \left(Min \frac{1.77 \times 10^{-6}}{C_{OUT}}, 0.06 \times V_{OUT} \right) .....(\Omega)$$

And the proper value for C_{COMP2} is:

$$C_{COMP2} = \frac{C_{OUT} R_{ESRCOUT}}{R_{COMP}}$$

Though C_{COMP2} is unnecessary when the output

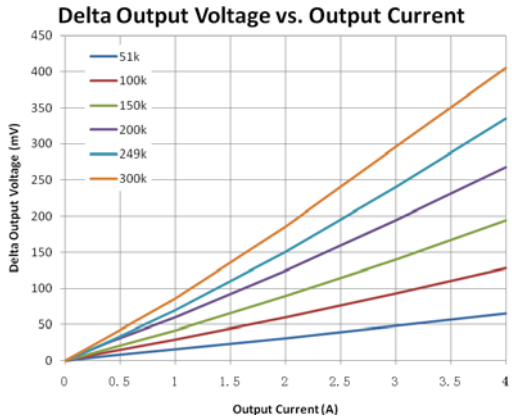
capacitor has sufficiently low ESR, a small value C_{COMP2} such as 100pF may improve stability against PCB layout parasitic effects.

- **CC Loop Stability**

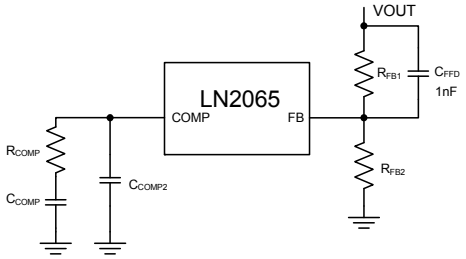
The constant-current control loop is internally compensated over the 2000mA-3500mA output range. No additional external compensation is required to stabilize the CC current.

- **Output Cable Resistance Compensation**

To compensate for resistive voltage drop across the charger's output cable, the LN2065 integrates a simple, user-programmable cable voltage drop compensation using the impedance at the FB pin. Use the curve in Figure 6 to choose the proper feedback resistance values for cable compensation. R_{FB1} is the high side resistor of voltage divider.



In the case of high R_{FB1} used, the frequency compensation needs to be adjusted correspondingly. As show in Figure 7, adding a capacitor in paralleled with R_{FB1} or increasing the compensation capacitance at COMP pin helps the system stability.



- **PC Board Layout Guidance**

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

1）Arrange the power components to reduce the AC loop size consisting of CIN, IN pin, SW pin and the schottky diode.

2）Place input decoupling ceramic capacitor CIN as close to IN pin as possible. CIN is connected power GND with vias or short and wide path.

3）Return FB, COMP and ISET to signal GND pin, and connect the signal GND to power GND at a single point for best noise immunity. Connect exposed pad to power ground copper area with copper and vias.

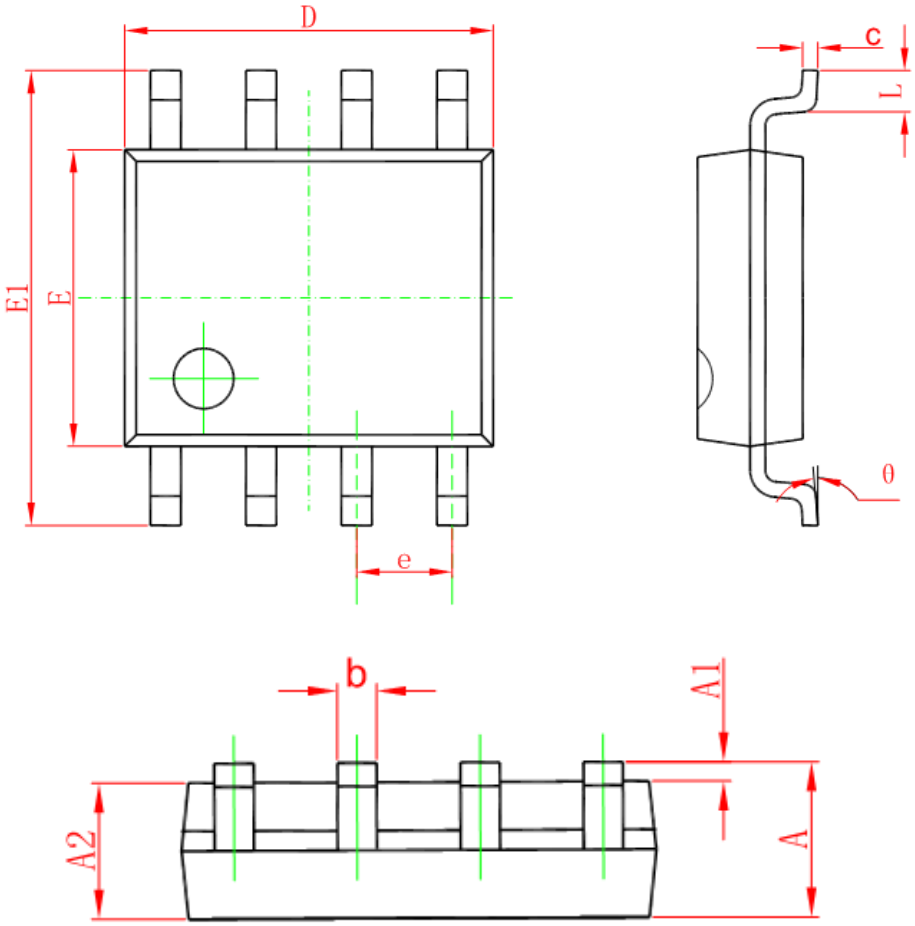
4）Use copper plane for power GND for best heat dissipation and noise immunity.

5）Place feedback resistor close to FB pin.

6）Use short trace connecting HSB-C_{HSB}-SW loop.

■ Package Information

- ESOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°