澎湃驅動力 源於力生美

LN3C69

HIGH PERFORMANCE CURRENT MODE PWM CONTROLLER

FEATURES

- LiiSemi Proprietary Cycle Turning Technology for Improved EMI Performance.
- Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design
- Audio Noise Free Operation
- External Programmable PWM Switching Frequency and Over Temperature Protection (OTP)
- Internal Synchronized Slope Compensation
- Low VDD Startup Current and Low Operating Current
- Leading Edge Blanking on Current Sense Input
- VDD Over Voltage Clamp and Under Voltage Lockout with Hysteresis (UVLO)
- Gate Output Maximum Voltage Clamp (18V)
- Line Input Compensated Over Universal Input Voltage Range.
- Cycle-by-Cycle Over-current Threshold Setting For Constant Output Power Limiting Over Universal Input Voltage Range.
- Overload Protection (OLP)

APPLICATIONS

- Offline AC/DC flyback converter
- Battery Charger
- Power Adaptor
- NoteBook Power Supplies
- Open-frame SMPS

GENERAL DESCRIPTION

LN3C69 is is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications in less than 70W range. PWM switching frequency at normal operation is externally programmable and trimmed to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved. VDD low startup current and low operating current contribute to a reliable power on startup design with LN3C69. A large value resistor could thus be used in the startup circuit to minimize the standby power. The internal slope compensation improves system large signal stability and reduces the possible sub-harmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense input removes the signal glitch due to snubber circuit diode reverse recovery and thus greatly reduces the external component count and system cost in the design. LN3C69 offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), over temperature protection (OTP), VDD over voltage clamp and under voltage lockout (UVLO). The Gate-drive output is clamped to maximum 18V to protect the power MOSFET. Excellent EMI performance is achieved with LiiSemi proprietary Cycle Turning technique together with soft switching control at the totem pole gate drive output.

Tone energy at below 22kHz is minimized in the design and audio noise is eliminated during operation. LN3C69 is offered in SOP8 and DIP8 packages.

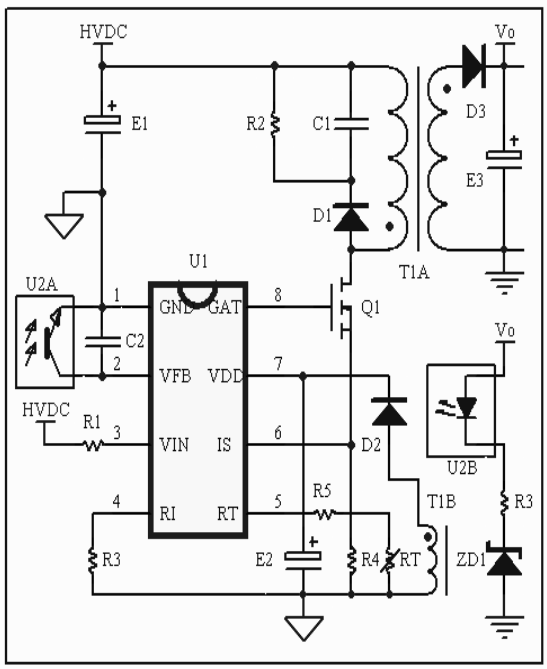


Fig1. *典型連接*

BLOCK DIAGRAM

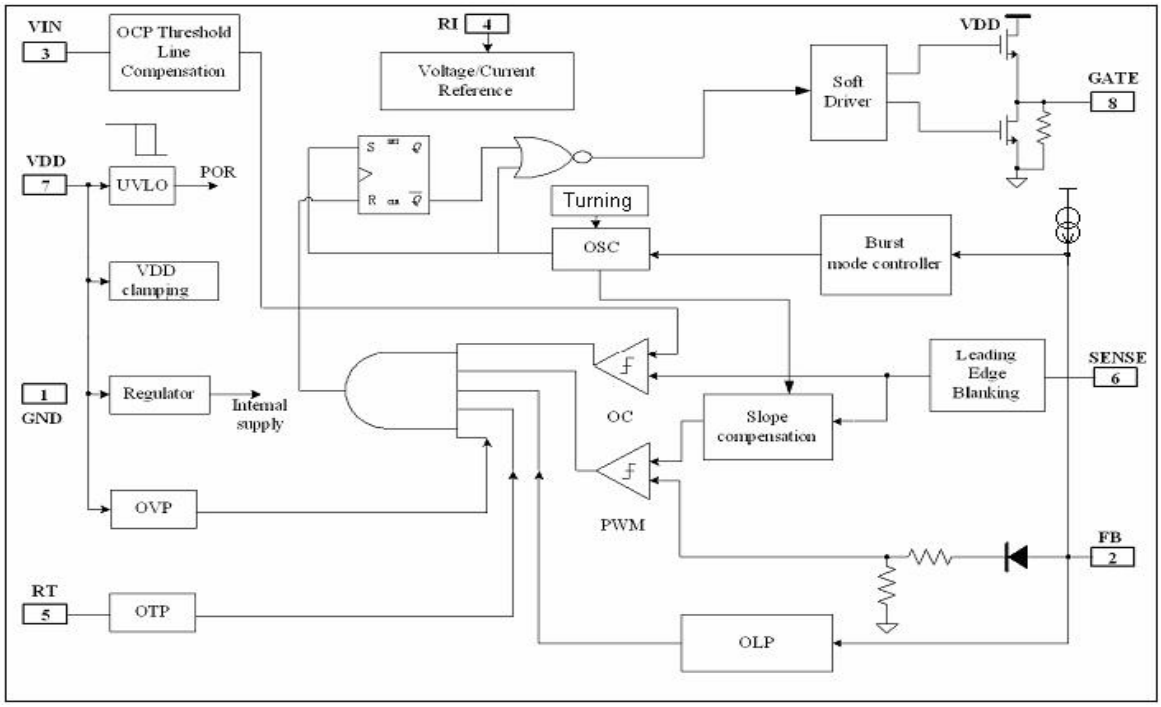


Fig2. 内部框图

Pin Configuration

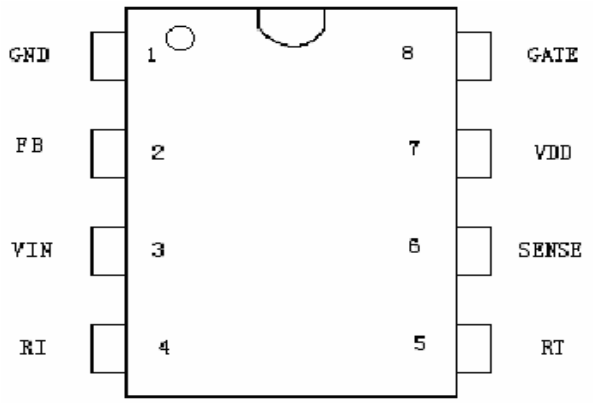


Fig3. 引腳定義

PIN ASSIGNMENTS

Pin No.	Name	Function	Description
1	GND	P	Ground
2	FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and SENSE pin input.
3	VIN	I	Connected through a large value resistor to rectified line input for Startup IC supply and line voltage sensing.
4	RI	I	Internal Oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.
5	RT	I	Temperature sensing input pin. Connected through a NTC resistor to GND.
6	SENSE	I	Current sense input pin. Connected to current sensing resistor node.
7	VDD	P	Chip DC power supply pin
8	GATE	O	Totem-pole drive output for the power MOSFET.

ABSOLUTE MAXIMUM RATINGS *

Item	Parameter	UNIT
VDD DC Supply Voltage	28	V
VDD Clamp Voltage	28	V
VDD DC Clamp Current	10	mA
VFB Input Voltage	-0.3 to 7	V
VSENSE Input Voltage to Sense Pin	-0.3 to 7	V
VRI Input Voltage to RI Pin	-0.3 to 7	V
Min/Max Operating Junction Temperature TJ	-20 to 150	℃
Min/Max Storage Temperature Tstg	-55 to 160	℃
ESD INFORMATION:		
HBM Human Body Model	3.0	KV
MM Machine Model	250	V

Note: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operat ion of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not im plied. Exposure to absolute maximum-rated conditions for ex tended periods may affect device reliability.

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min	Type	Max	Unit
VDD	VDD Supply Voltage	12		25	V
RI	RI Resistor Value	24		31	KΩ
TA	Operating Ambient Temperature	-20		85	℃

ELECTRICAL CHARACTERISTICS (TA = 25℃, VDD=15V, RI=24KΩ if not otherwise noted)

Supply Voltage (VDD)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{QS}	VDD Start up Current	VDD=15V,RI=24K,Measure Leakage current into VDD		6	20	uA
I_Q	Operation Current	VDD=15V,RI=24KΩ,VFB=3V		2.0		mA
V_{START}	UVLO Threshold Voltage	FB=0	15.5	16.5	17.5	V
V_{STOP}			9.5	10.5	11.5	V
OVP(ON)*	VDD Over Voltage Protection on		23.5	25	26.5	V
OVP(OFF)*	VDD Over Voltage Protection off		21.5	23	24.5	V
OVP_Hys*	OVP Hysteresis	OVP(ON)-OVP(OFF)		2		V
VDD_CL	VDD Zener Voltage	IVDD=10mA		28		V

Feedback Input Section(FB Pin)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
A_{VCS}	PWM Input Gain	VFB / Vcs		2.8		V/V
V_{FB}	V_{FB} Open Loop Voltage	V_{FB}=Open		5.9		V
I_{FB_S}	FB short current	FB=0 , FB short to GND		0.8		mA
VTH_{MIN}	Zero Duty FB Threshold Voltage				0.95	V
VTH_BM	Burst Mode FB Threshold Voltage			1.7		V
VTH_{MAX}	Power Limiting FB Threshold Voltage			4.4		V
TD_{MAX}	Power limiting Debounce Time			80		mS
Z_{FB}	FB Input Impedance			7.2		KΩ

Current Sense Input(Sense Pin)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{LEB}	Leading edge blanking			250		nS
Z_{CS}	CS Input Impedance			30		KΩ
T_{OCP}	OCP Delay	CL=1nF at Gate		120		nS
VTH_{OCP1}	OCP Threshold Voltage	I_vin=0	0.85	0.90	0.95	V
VTH_{OCP2}	OCP Threshold Voltage	I_vin=150uA		0.81		V

Oscillator

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{OSC}	Normal Oscillation Frequency		60	65	70	kHz
ΔF_{OSC_T}	Frequency Temperature Stability	TA=-20℃ to 100 ℃		2		%

ΔF_{OSC}_V	Frequency Voltage Stability	VDD = 12-25V		2		%
RI	Operating RI Range		12	24	60	KΩ
V_{RI}	RI open voltage			2		V
D_{MAX}	Maximum Duty Cycle		75	80	85	%
F_{OSC}_min	Burst Mode Base Frequency			22		kHz

Gate Drive Output

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OL}	Output Low Level	Io = -20 mA			0.3	V
V_{OH}	Output High Level	Io = 20 mA	11			V
V_O_CL	Output Clamp Voltage	VDD=20V		18		V
T_r	Output Rising Time	CL = 1nF		120		nS
T_f	Output Falling Time	CL = 1nF		50		nS

Over Temperature Protection

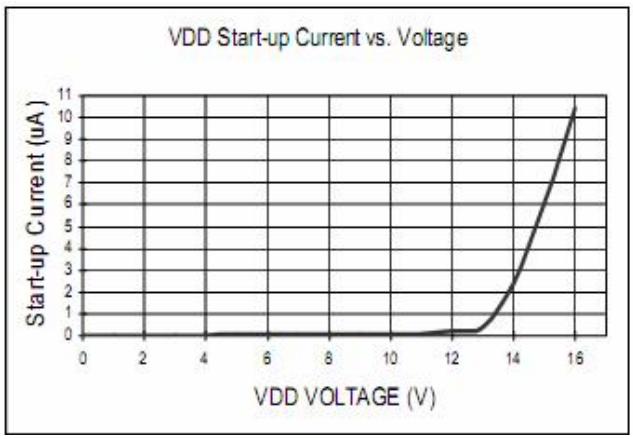
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_RT	Output Current of RT			70		uA
VTH_OTP	OTP Threshold Voltage		1.015	1.065	1.115	V
VTH_OTP_off	OTP Recovery Threshold Voltage			1.165		V
TD_OTP	OTP De-bounce Time			100		uS
V_RT_Open	RT Pin Open Voltage			3.5		V

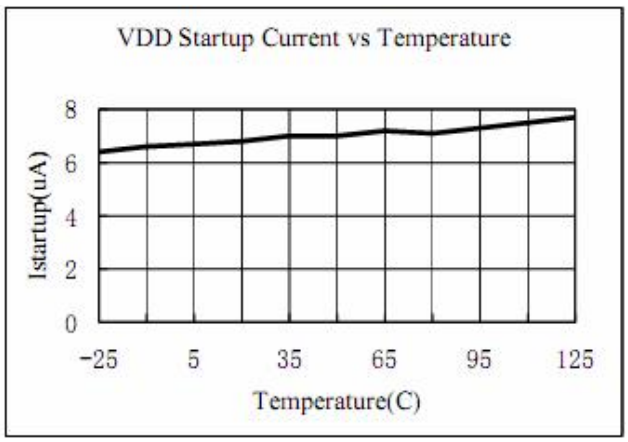
Cycle Turning[+]

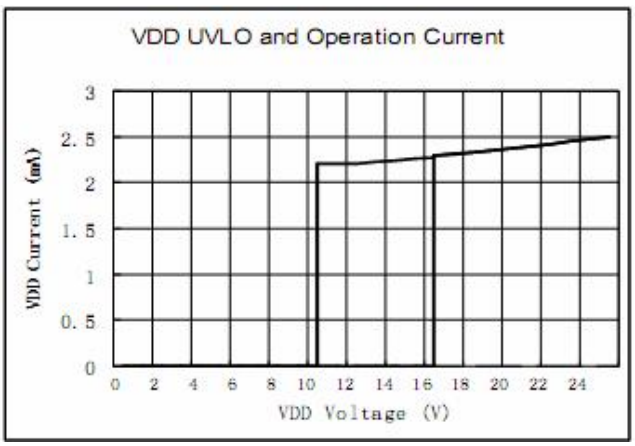
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ΔF_{OSC}	Cycle Turning range		-2		+2	kHz
T_{CT}	Cycle Turning Time			30		mS

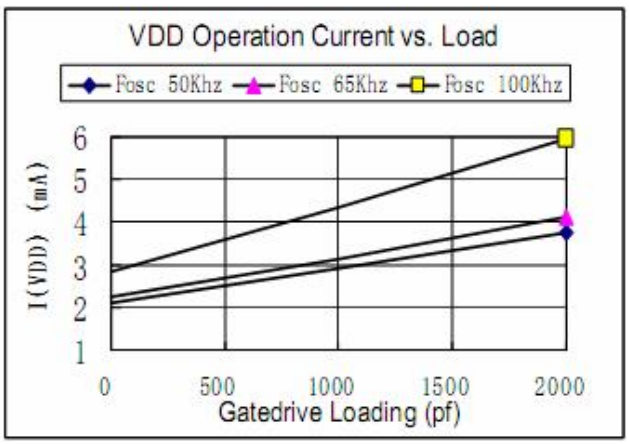
CHARACTERIZATION PLOTS

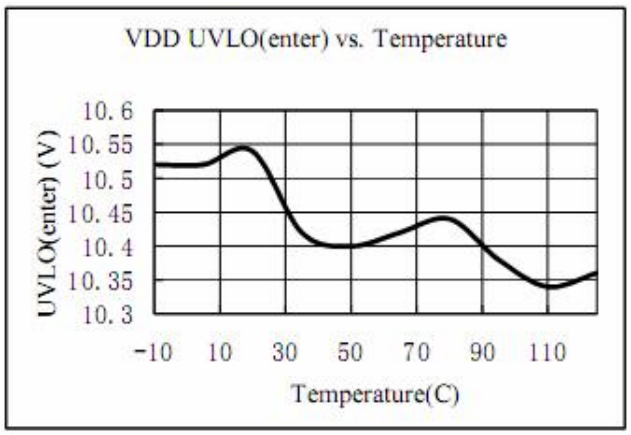
(VDD = 15V, RI = 24 KΩ, TA = 25℃ condition applies if not otherwise noted.)

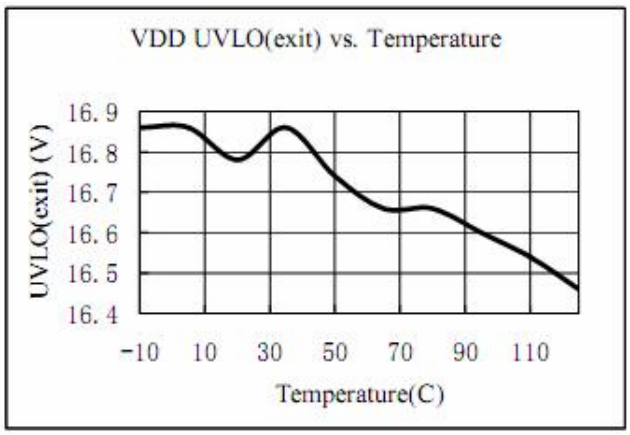


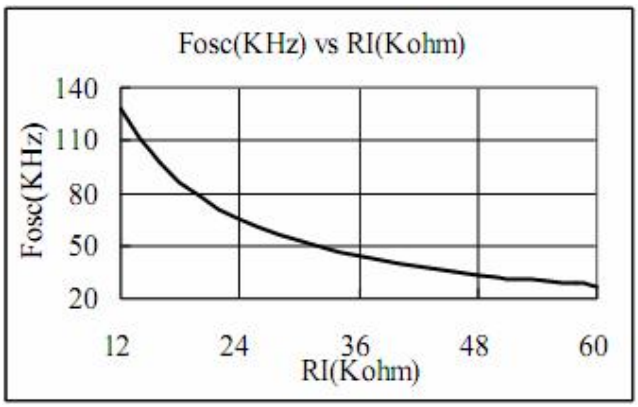


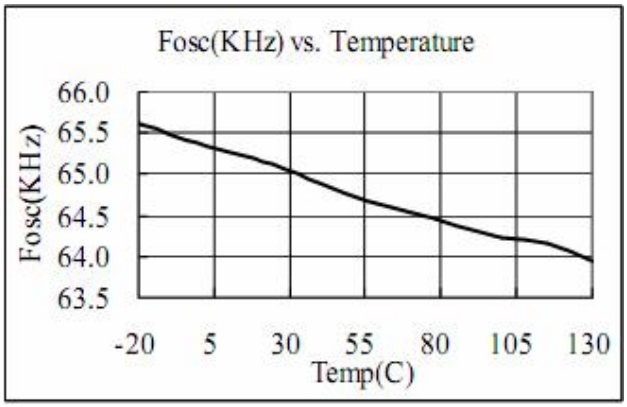


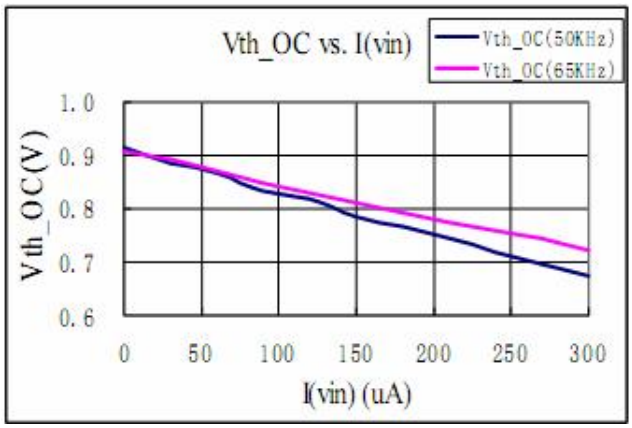


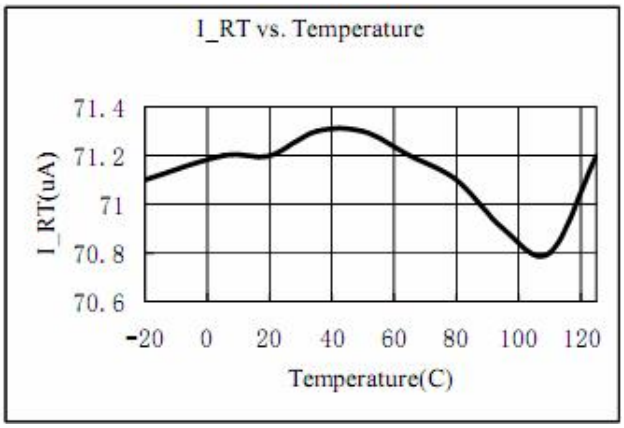

VDD UVLO(enter) vs. Temperature
UVLO(enter) (V)
10.6
10.55
10.5
10.45
10.4
10.35
10.3
-10 10 30 50 70 90 110
Temperature(C)


VDD UVLO(exit) vs. Temperature
UVLO(exit) (V)
16.9
16.8
16.7
16.6
16.5
16.4
-10 10 30 50 70 90 110
Temperature(C)


Fosc(KHz) vs RI(Kohm)
Fosc(KHz)
140
110
80
50
20
12 24 36 48 60
RI(Kohm)


Fosc(KHz) vs. Temperature
Fosc(KHz)
66.0
65.5
65.0
64.5
64.0
63.5
-20 5 30 55 80 105 130
Temp(C)


Vth_OC vs. I(vin)
Vth_OC(50KHz)
Vth_OC(65KHz)
Vth_OC(V)
1.0
0.9
0.8
0.7
0.6
0 50 100 150 200 250 300
I(vin) (uA)


I_RT vs. Temperature
I_RT(uA)
71.4
71.2
71
70.8
70.6
-20 0 20 40 60 80 100 120
Temperature(C)

OPERATION DESCRIPTION

The LN3C69 is a highly integrated PWM controller IC optimized for offline flyback converter applications in sub 70W power range. The extended burst mode control greatly reduces the standby power consumption and helps the design easily meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of LN3C69 is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet provides reliable startup in application. For AC/DC adaptor with universal input range design, a 2 M startup resistor could be used together with a VDD capacitor to provide a fast startup and low power dissipation solution.

Operating Current

The Operating current of LN3C69 is low at 2.0mA. Good efficiency is achieved with LN3C69 low operating current together with extended burst mode control features.

Cycle Turning+ for EMI improvement

The Cycle Turning+ (switching frequency modulation) is implemented in LN3C69. The oscillation frequency is modulated with a random source so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore reduces system design challenge.

Extended Burst Mode Operation

At zero load or light load condition, majority of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. LN3C69 self adjusts the switching mode according to the loading condition. At from no load to light/medium load condition, the FB input drops below burst mode threshold level. Device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend. The frequency control also eliminates the audio noise at any loading conditions.

Oscillator Operation

A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation within the specified RI in Kohm range at nominal loading operational condition.

$$Fosc = \frac{1560}{RI(K\Omega)}(\text{kHz})$$

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in LN3C69 current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to Snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Gate Drive

LN3C69 Gate is connected to an external MOSFET gate for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI. A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 18V clamp is added for MOSFET gate protection at higher than expected VDD input.

Protection Controls

Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP) and over voltage clamp, Under Voltage Lockout on VDD (UVLO).

With LIISEMI Proprietary technology, the OCP threshold tracks PWM Duty cycles and is line voltage compensated to achieve constant output power limit over the universal input voltage range with recommended reference design.

At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the output power MOSFET. Device restarts when VDD voltage drops below UVLO limit.

VDD is supplied by transformer auxiliary winding output. It is clamped when VDD is higher than threshold value. The power MOSFET is shut down when VDD drops below UVLO limit and device enters power on start-up sequence thereafter.

A NTC resistor in series with a regular resistor should connect between RT and GND for temperature sensing and protection. NTC resistor value becomes lower when the ambient temperature rises. With the fixed internal current IRT flowing through the resistors, the voltage at RT pin becomes lower at high temperature. The internal OTP circuit is triggered and shutdown the MOSFET when the sensed input voltage is lower than VTH_OTP.

TYPICAL APPLICATION

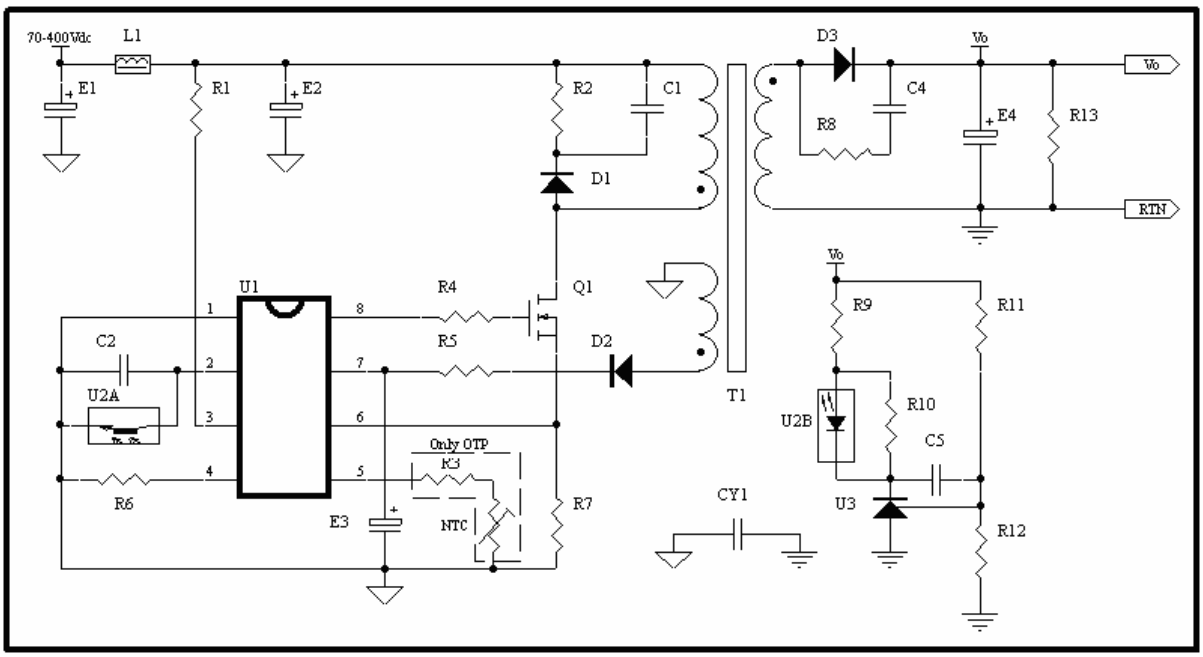
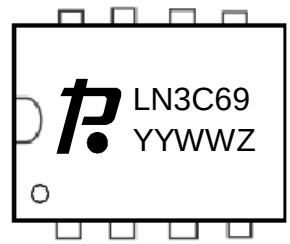


Fig4. *典型应用图*

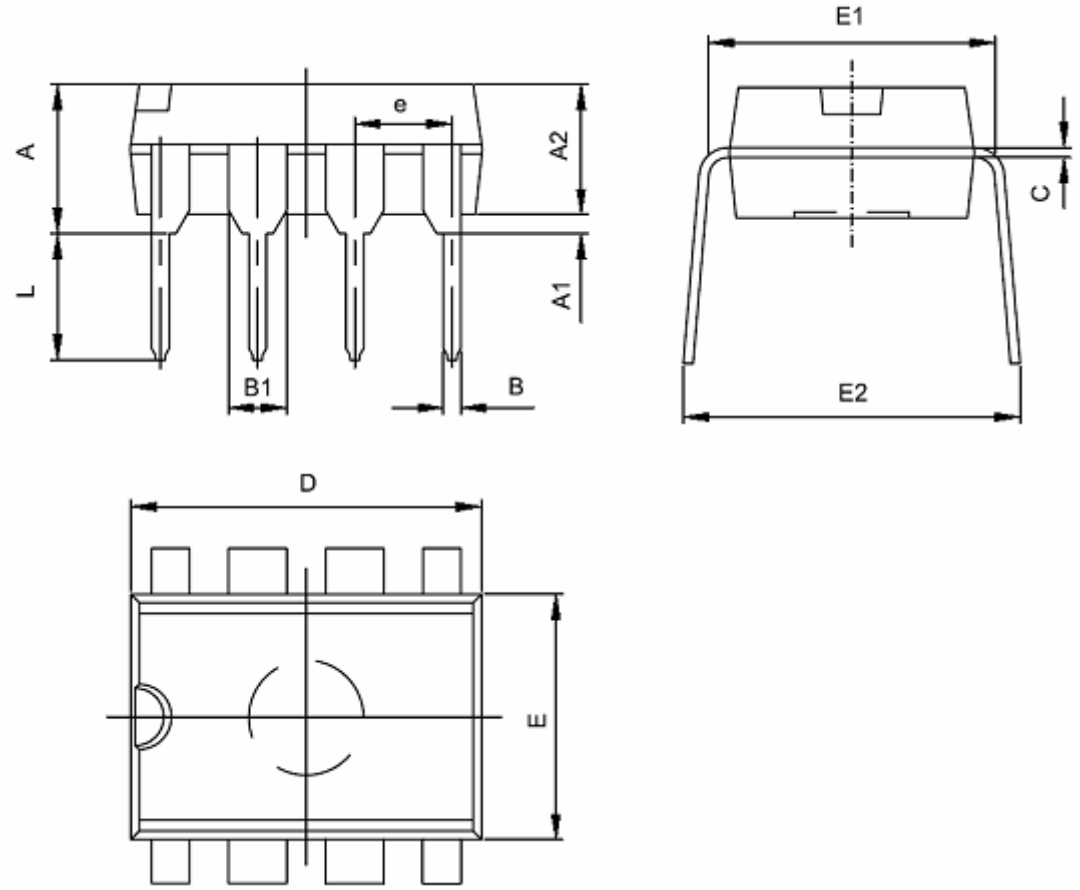
MARKING INFORMATION



Model & DateCode Information:
Single-line mode: **05YYWWZ**
Dual-line mode: **LN3C69**
YYWWZ
YY: Year Code, 01-99 **à** 2001-2099
WW: Week Code, 01-52 Week
Z: Other Information(Optional)

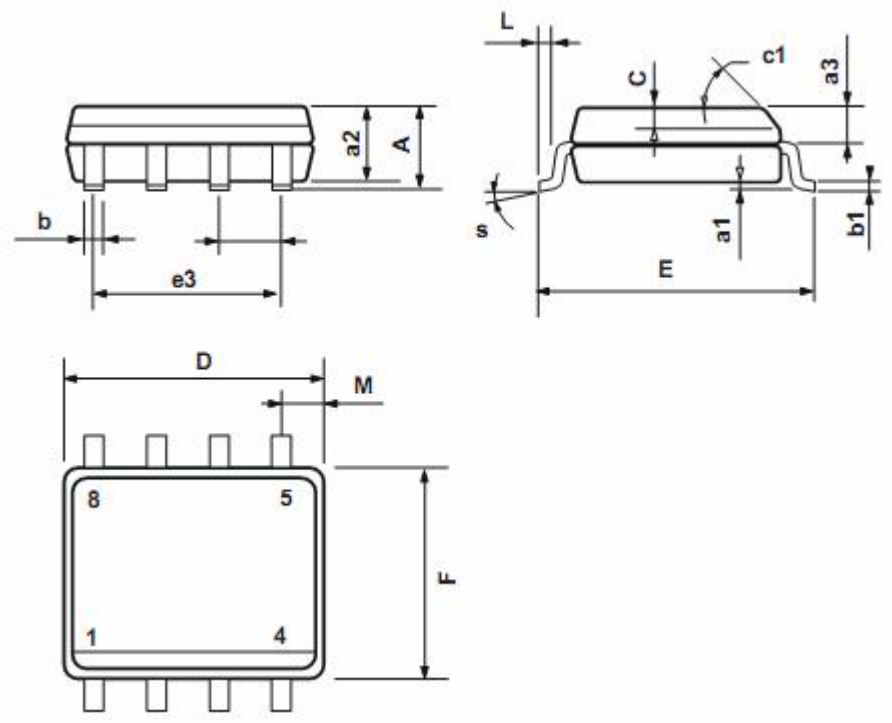
PACKAGE MECHANICAL DATA

8-Pin Plastic DIP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.360	0.560	0.014	0.022
B1	1.524(TYP)		0.060(TYP)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.620(TYP)		0.300(TYP)	
e	2.540(TYP)		0.100(TYP)	
L	3.000	3.600	0.118	0.142
E2	8.200	9.400	0.323	0.370

8-Pin Plastic Micropackage SO8



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

ORDERING INFORMATION

Part Name	T.R.Rating	Description	Packing
LN3C69D	90℃/W	DIP8	50PCS/TUBE
LN3C69M	150℃/W	SOP8	100PCS/TUBE
LN3C69DP	90℃/W	DIP8,With OVP	50PCS/TUBE
LN3C69MP	150℃/W	SOP8,With OVP	100PCS/TUBE

文檔修改記錄

版本	說明	作者	日期
A	初版發布	James	20100510

聲 明 IMPORTANT NOTICE