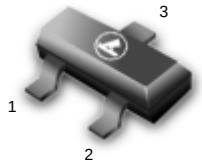
30V N-Channel Enhancement-Mode MOSFET

V_{DS}= 30V
$R_{DS(ON)}$, V_{gs}@10V, I_{ds}@6 A = 38mΩ
$R_{DS(ON)}$, V_{gs}@4.5V, I_{ds}@5A = 52mΩ

LN4812LT1G
S-LN4812LT1G



SOT– 23 (TO–236AB)

Features

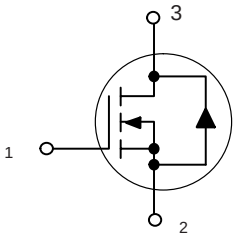
Advanced trench process technology
High Density Cell Design For Ultra Low On-Resistance
High Power and Current Handling Capability
S- Prefix for Automotive and Other Applications Requiring
Unique Site and Control Change Requirements; AEC-Q101
Qualified and PPAP Capable.

▼ Simple Drive Requirement

▼ Small Package Outline

▼ Surface Mount Device

N - Channel



Ordering Information

Device	Marking	Shipping
LN4812LT1G S-LN4812LT1G	N48	3000/Tape&Reel
LN4812LT3G S-LN4812LT3G	N48	10000/Tape&Reel

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter		Limit	Unit
V_{DS}	Drain-Source Voltage		30	V
V_{GS}	Gate-Source Voltage		± 20	
I_D	Continuous Drain Current		6	A
I_{DM}	Pulsed Drain Current [1)]		30	
P_D	Maximum Power Dissipation	TA = 25°C	1.4	W
		TA = 75°C	0.8	
T_J, T_{stg}	Operating Junction and Storage Temperature Range		-55 to 150	°C
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		50	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance (PCB mounted) [2)]		90	

Note: 1. Repetitive Rating: Pulse width limited by the maximum junction temperature
2. 1-in^2 2oz Cu PCB board
3. Guaranteed by design; not subject to production testing

LN4812LT1G , S-LN4812LT1G

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Static						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250uA	30			V
$R_{DS(on)}$	Drain-Source On-State Resistance	V_{GS} = 4.5V, I_D = 5A		35.0	52.0	mΩ
$R_{DS(on)}$	Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 6A		22.0	38.0	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} =V_{GS}, I_D = 250uA	1	1.5	3	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V			1	uA
I_{GSS}	Gate Body Leakage	V_{GS} = ± 20V, V_{DS} = 0V			± 100	nA
g_{fs}	Forward Transconductance	V_{DS} = 5V, I_D = 6.9A		15.4		S
Dynamic[3)]						
Q_g	Total Gate Charge	V_{DS} = 15V, I_D = 8.5A V_{GS} = 10V		13	20	nC
Q_{gs}	Gate-Source Charge			4.2		
Q_{gd}	Gate-Drain Charge			3.1		
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15V, R_L = 15Ω I_D = 1A, V_{GEN} = 10V R_G = 6Ω		9		ns
t_r	Turn-On Rise Time			14		
$t_{d(off)}$	Turn-Off Delay Time			30		
t_f	Turn-Off Fall Time			5		
C_{iss}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V f = 1.0 MHz		610		pF
C_{oss}	Output Capacitance			100		
C_{rss}	Reverse Transfer Capacitance			77		
Source-Drain Diode						
I_S	Max. Diode Forward Current				3	A
V_{SD}	Diode Forward Voltage	I_S = 1A, V_{GS} = 0V			1.3	V

Note: Pulse test: pulse width <= 300us, duty cycle<= 2%

LN4812LT1G , S-LN4812LT1G

TYPICAL ELECTRICAL CHARACTERISTICS

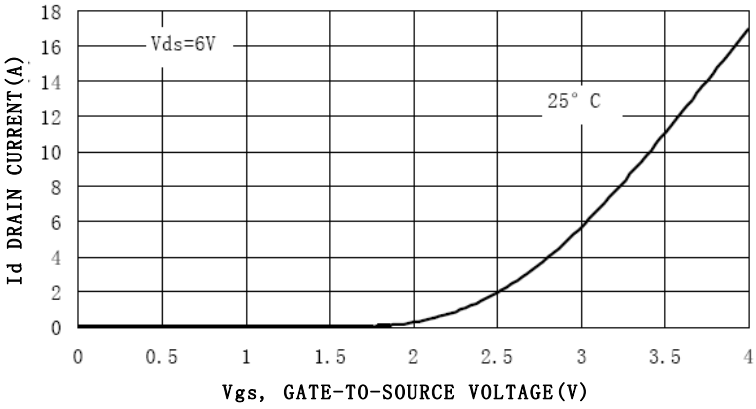


Figure 1. Transfer Characteristics

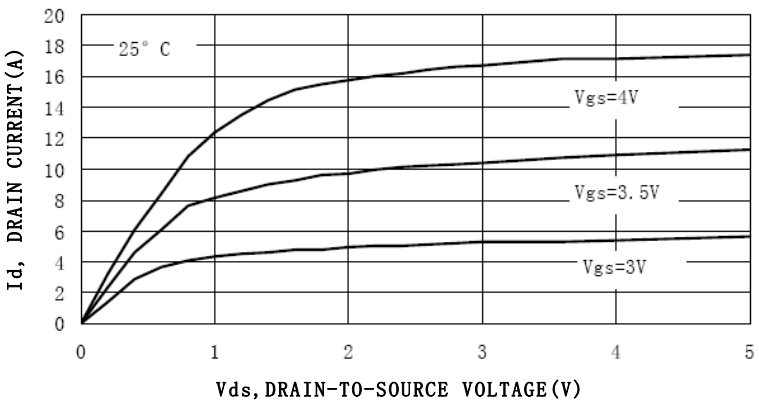


Figure 2. On–Region Characteristics

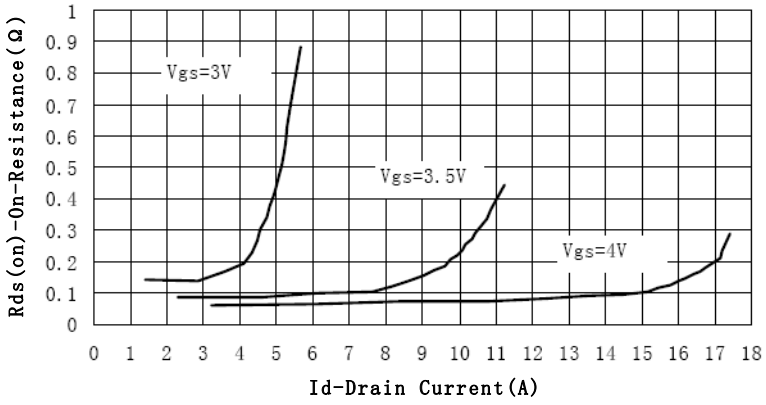


Figure 3. On–Resistance versus Drain Current

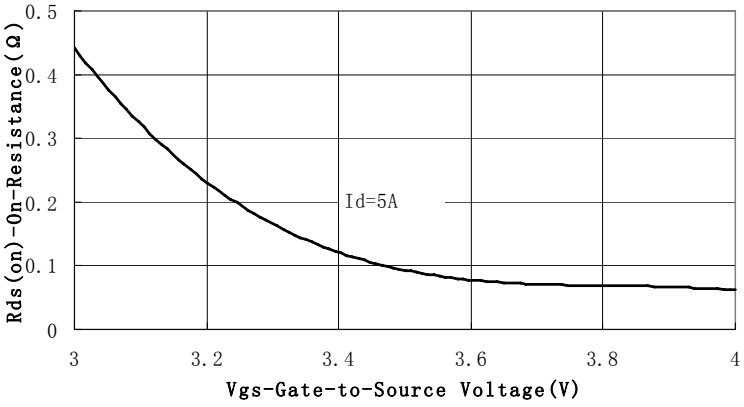
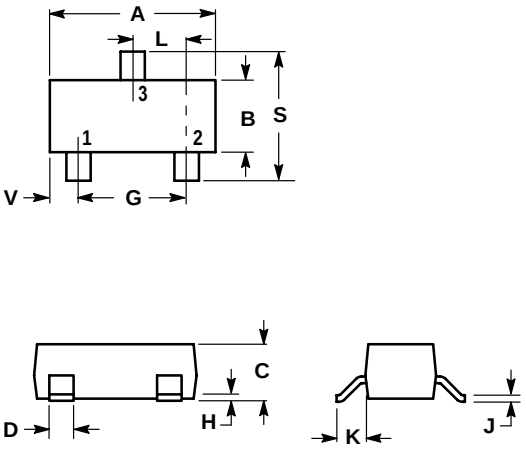


Figure 4. On-Resistance vs. Gate-to-Source Voltage

LN4812LT1G , S-LN4812LT1G

SOT–23



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M,1982
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60