25mW Cap-Free Stereo Headphone Amplifier

■ GENERAL DESCRIPTION

The LN4822 stereo headphone driver is designed for portable equipment where board space is at a premium. Differential stereo inputs and built-in resistors set the device gain, further reducing external component count. Gain is selectable at -6 dB, 0 dB, 3 dB or 6 dB. The amplifier drives 25 mW into 16Ω speakers from a single 2.3 V supply. The LN4822 provides a constant maximum output power independent of the supply voltage, thus facilitating the design for prevention of acoustic shock.

The LN4822 features fully differential inputs to reduce system noise pickup between the audio source and the headphone amplifier. The high power supply noise rejection performance and differential architecture provides increased RF noise immunity. For single-ended input signals, connect INL+ and INR+ to ground.

The device has built-in pop suppression circuitry to completely eliminate disturbing pop noise during turn-on and turn-off. The amplifier outputs have short-circuit and thermal-overload protection along with ±8 kV HBM ESD protection.

The LN4822 operates from a single 2.3 V to 5.5 V supply with 3.3 mA of typical supply current. Shutdown mode reduces supply current to less than 1 µA.

■ FEATURES

- Charge-Pump Eliminates Need for DC-Blocking Capacitors:
  --Outputs biased at o V
  --Excellent Low Frequency Fidelity
- Active Click and Pop Suppression
- 3.3 mA Typical Supply Current
- Fully Differential or Single-Ended Inputs
  --Built-In Resistors Reduces Component Count
  --Improves System Noise Performance
- Constant Maximum Output Power from 2.3 V to 5.5 V Supply
  --Simplifies Design to Prevent Acoustic Shock
- Improved RF Noise Immunity
- High Power Supply Noise Rejection
  --100 dB PSRR at 217 Hz
  --90 dB PSRR at 10 kHz
- Wide Power Supply Range: 2.3 V to 5.5 V
- Gain Settings: – 6 dB, 0 dB, 3 dB, and 6 dB
- Short-Circuit and Thermal-Overload Protection
- ±8 kV HBM ESD Protected Outputs
- Small Package Available
  --16-Pin, 3 mm × 3 mm Thin QFN

■ APPLICATIONS

- Smart Phones/Cellular Phones
- Notebook Computers
- Portable DVD Player
- Personal Digital Assistants(PDAs)
- Electronic Dictionaries
- Digital Still Cameras
- Potable Gaming

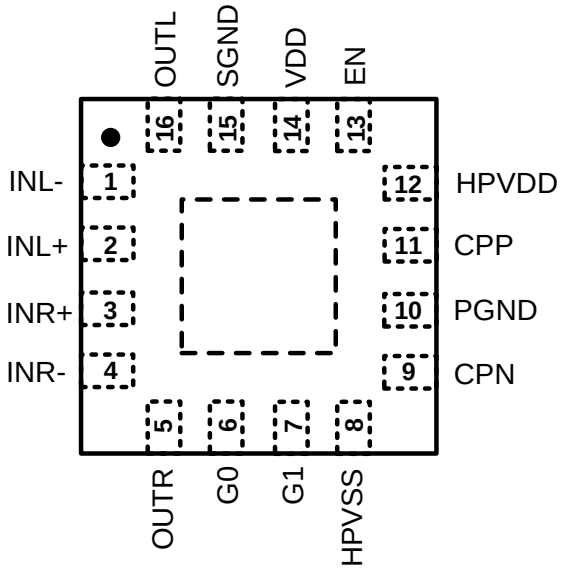
■ ORDERING INFORMATION

LN4822 X X

- Device Orientation:
  R:Embossed Tape: Standard Feed
  L:Embossed Tape: Reverse Feed
- Package:
  Q:QFN3*3-16

Ordering Number	Package Type	Shipping Package
LN4822QR	QFN3*3-16L	3,000 Units/ Tape & Reel

■ PIN CONFIGURATION & MARK INFORMATION

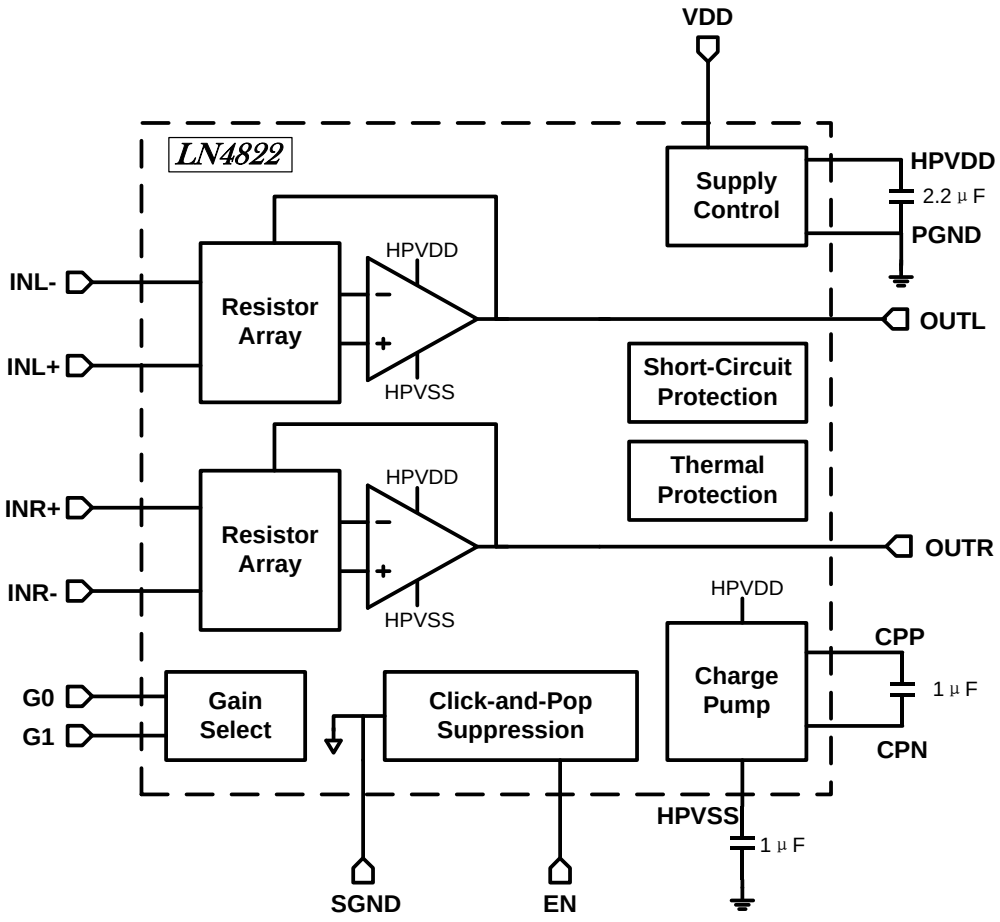


Pin Function Description:

Name	Number	I/O	Function Description
INL-	1	I	Inverting left input for differential signals; left input for single-ended signals
INL+	2	I	Non-inverting left input for differential signals. Connect to ground for single-ended input applications
INR+	3	I	Non-inverting right input for differential signals. Connect to ground for single-ended input applications
INR-	4	I	Inverting right input for differential signals; right input for single-ended signals
OUTR	5	O	Right headphone amplifier output. Connect to right terminal of headphone jack
G0	6	I	Gain select
G1	7	I	Gain select
HPVSS	8	O	Charge pump output and negative power supply for output amplifiers; connect 1 μF

			capacitor to GND
CPN	9	P	Charge pump negative flying cap. Connect to negative side of 1 μF capacitor between CPP and CPN
PGND	10	P	Ground
CPP	11	P	Charge pump positive flying cap. Connect to positive side of 1 μF capacitor between CPP and CPN
HPVDD	12	P	Positive power supply for headphone amplifiers. Connect to a 2.2 μF capacitor. Do not connect to VDD
EN	13	I	Amplifiers enable. Connect to logic low to shutdown; connect to logic high to activate
VDD	14	P	Positive power supply for LN4822
SGND	15	I	Amplifier reference voltage. Connect to ground terminal of headphone jack
OUTL	16	O	Left headphone amplifier output. Connect to left terminal of headphone jack
Thermal Pad	—	P	Solder the exposed metal pad on the LN4822 QFN package to the landing pad on the PCB. Connect the landing pad to ground or leave it electrically unconnected (floating).

■ FUNCTION BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3—6.0	V
Input Voltage（INR+、INR-、INL+、INL-）	V_{IN}	HPVSS-0.3—HPVDD+0.3	V
Power Output	—	Internal limit	
Junction Temperature	—	-150	℃
Storage Temperature	Tstg	-65—150	℃
ESD Susceptibility	—	8000	V

■ ELECTRICAL CHARACTERISTICS

(VDD = 3.6V，RL=16Ω，Unless otherwise specified. Limits apply for TA = 25 ℃.)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Unit
V_{PVDD}	Supply voltage		2.3		5.5	V
I_Q	Quiescent Current	EN=PVDD, No load	2	3.3	5	mA
P_O	Output Power per Channel	THD=1%, f=1kHz, R_L=16Ω		35		mW
		THD=1%, f=1kHz, R_L=32Ω		25		
I_{SD}	Shutdown Current	EN=0V, PVDD=2.5V to 5.5V		0.1	1	μA
V_{IH}	EN High level input voltage		1.4			V
V_{IL}	EN Low level input voltage				0.6	V
V_{GH}	G0,G1 High level input voltage		1.4			V
V_{GL}	G0,G1 Low level input voltage				0.6	V
V_{OS}	Output Offset voltage			1	3	mV
AV	Closed-loop voltage gain	G0=0V, G1=0V		-6		dB
		G0=PVDD,G1=0V		0		dB
		G0=0V,G1=PVDD		3		dB
		G0=PVDD,G1=PVDD		6		dB
PSRR	Power supply rejection ratio	Input f=1KHz,Vpp=200mV		75		dB
THD+N	Total Harmonic distortion plus noise	Po=20mW,f=1kHz		0.03		%
SNR	Signal to noise ratio	Po=20mW into 16Ω		100		dB
En	Noise output voltage	A-weighted		10		uVrms
CS	Crosstalk	Po=15mW,f=1kHz		80		dB
F_{OSC}	Charge-pump switching frequency		1.2	1.5	1.8	MHz

Ton	Start-up time	EN from low to high		0.4		ms
OTP	Thermal shutdown	Threshold		150		℃
OTPH	Thermal shutdown Hysteresis	Hysteresis		30		℃

■ APPLICATION INFORMATION

GAIN CONTROL

The LN4822 has four gain settings which are controlled with pins G0 and G1.The following table gives an overview of the gain function.

G0 Voltage	G1 Voltage	GAIN
≤0.6 V	≤0.6 V	-6 dB
≥1.4 V	≤0.6 V	0 dB
≤0.6 V	≥1.4 V	3 dB
≥1.4 V	≥1.4 V	6 dB

INPUT COUPLING CAPACITORS

Input coupling capacitors block any DC bias from the audio source and ensure maximum dynamic range. Input coupling capacitors also minimize LN4822 turn-on pop to an inaudible level.

The input capacitors are in series with LN4822 Internal input resistors, creating a high-pass filter. The following Equation calculates the high-pass filter corner frequency.

$$f_C = \frac{1}{2\pi R_{IN} C_{IN}}$$

The input impedance, R_{IN}, is dependent on device gain. Larger input capacitors decrease the corner frequency. See the following table for input impedance values.

G0 Voltage	G1 Voltage	R_{IN}
≤0.6 V	≤0.6 V	26.4KΩ
≥1.4 V	≤0.6 V	19.8KΩ
≤0.6 V	≥1.4 V	16.5KΩ
≥1.4 V	≥1.4 V	13.2KΩ

For a given high-pass cut off frequency, the minimum input coupling capacitor is found as:

$$C_{IN} = \frac{1}{2\pi f_C R_{IN}}$$

Example: Design for a 20Hz corner frequency with a LN4822 gain of +6dB. The input impedance table gives R_{IN} as 13.2KΩ. The C_{IN} Equation shows the input coupling capacitors must be at least 0.6μF to achieve a 20Hz high-pass corner frequency. Choose a 0.68μ F standard value capacitor for each LN4822 input.

CHARGE PUMP FLYING CAPACITOR, HPVDD CAPACITOR AND HPVSS CAPACITOR

The LN4822 uses a built-in charge pump to generate a positive and negative voltage supply for the headphone amplifiers. The charge pump flying capacitor connects between CAP+ and CAP-. It transfers charge to generate the positive and negative supply voltage. The HPVDD capacitor or HPVSS capacitor must be at least equal in or larger than value to the flying capacitor to allow maximum charge transfer. Use low equivalent-series-resistance (ESR) ceramic capacitors to maximize charge pump efficiency. Typical values are 1uF for the HPVDD, HPVSS and flying capacitors.

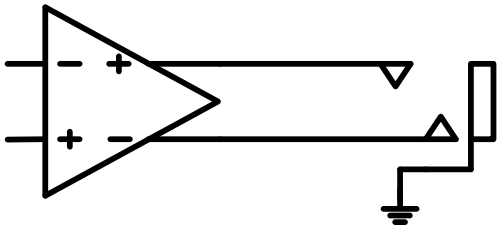
POWER SUPPLY DECOUPLING CAPACITORS

The LN4822 true-cap-free headphone amplifier requires adequate power supply decoupling to ensure that output noise and total harmonic distortion (THD) remain low. Use good low equivalent-series-resistance (ESR) ceramic capacitors. Place a 2.2μ F capacitor within 5 mm of the PVDD pin. Reducing the distance between the decoupling capacitor and PVDD minimizes parasitic inductance and resistance, improving LN4822 supply rejection performance. Use 0402 or smaller size capacitors if possible.

POWER SUPPLY SEQUENCING

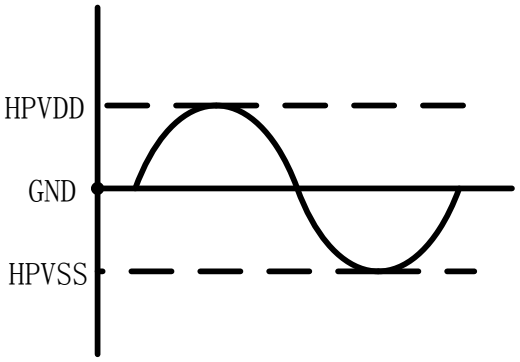
Use input coupling capacitors to ensure inaudible turn-on pop. Activate the LN4822 after all audio

sources have been activated and their output voltages have settled. On power-down, deactivate the LN4822 before deactivating the audio input source. The EN pin Controls device shutdown: Set to 0.6V or lower to deactivate the LN4822; set to 1.4V or higher to activate.



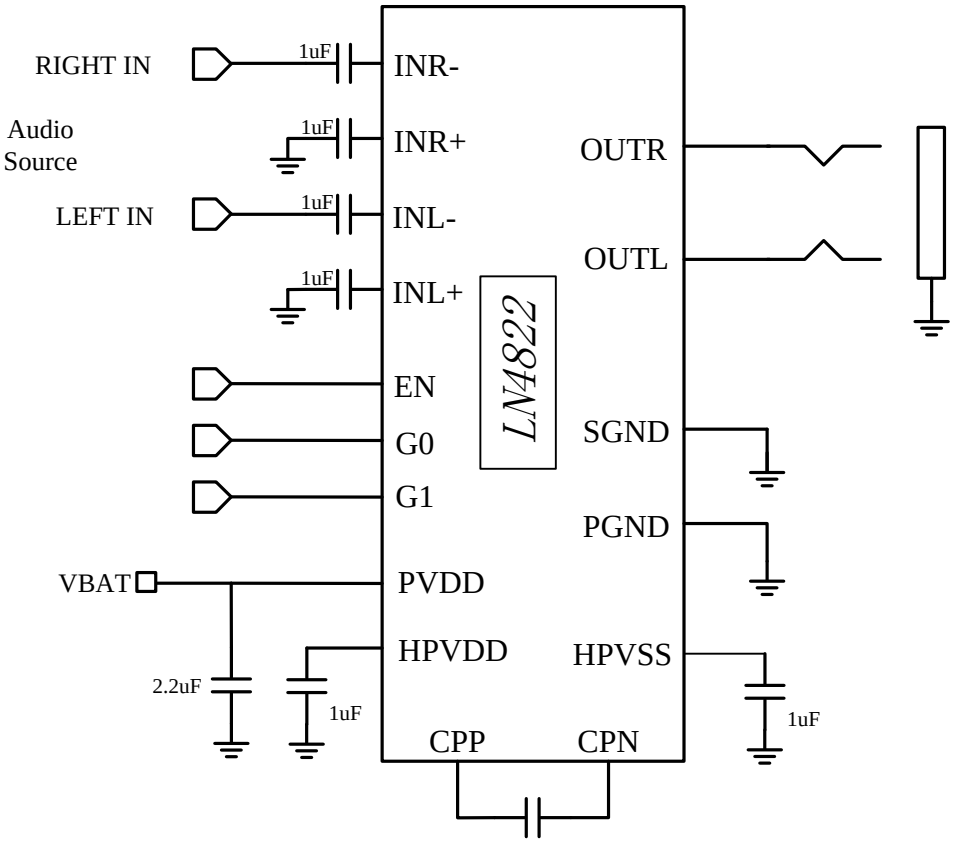
TRUE-CAP-FREE HEADPHONE AMPLIFIERS

The True-Cap-Free amplifier architecture operates from a single supply voltage and uses two internal charge pumps to generate a positive supply and a negative supply rail for the headphone amplifier. The output voltages are centered around 0V and are capable of positive and negative voltage swings as shown in the following drawing.



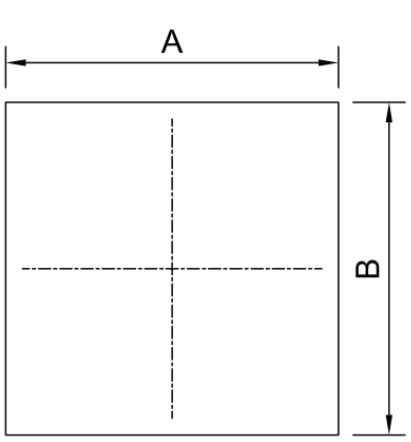
True-Cap-Free amplifiers require no output dc-blocking capacitors. The headphone connector shield pin connects to ground and will interface with headphones and non-headphone accessories. The LN4822 is a True-Cap-Free amplifier.

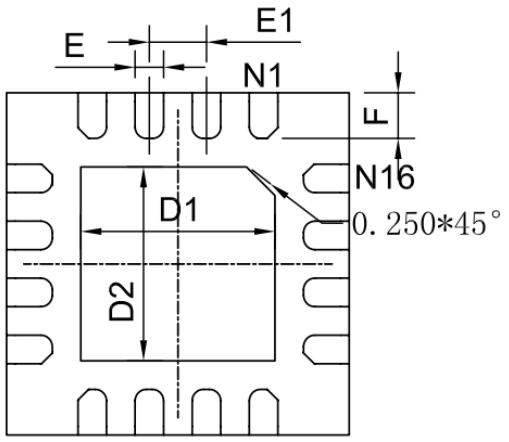
■ Typical Application Circuit

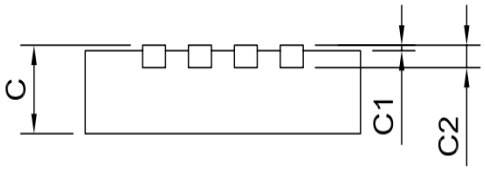


■ Package Information

QFN3*3-16L







DIMENSION 尺寸 / LABEL 标注	MIN（mm）最小（mm）	MAX（mm）最大（mm）	DIMENSION 尺寸 / LABEL 标注	MIN（mm）最小（mm）	MAX（mm）最大（mm）
A	3. 0±0. 1		D1	1. 70TYP	
B	3. 0±0. 1		D2	1. 70TYP	
C	0. 70	0. 80	E	0. 250TYP	
C1	0~0. 050		E1	0. 500TYP	
C2	0. 203TYP		F	0. 400TYP	