16-bit constant current LED sink driver

■ General Description

LN5024 is designed for LED displays. As an enhancement of its predecessor, LN5024 exploits Precision Drive™ technology to enhance its output characteristics. LN5024 contains a serial buffer and data latches which convert serial input data into parallel output format. At LN5024 output stage, sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs within a large range of Vf variations. LN5024 provides users with great flexibility and device performance while using LN5024 in their system design for LED display applications, e.g. LED panels. Users may adjust the output current from 3 mA to 45 mA through an external resistor, Rext, which gives users flexibility in controlling the light intensity of LEDs. LN5024 guarantees to endure maximum 17V at the output port. The high clock frequency, 25MHz, also satisfies the system requirements of high volume data transmission.

■ Features

- 16 constant-current output channels
- Constant output current invariant to load voltage change
- Excellent output current accuracy:
- Between channels: <±3% (max.), and between ICs: <±6% (max.)
- Output current adjusted through an external resistor
- Constant output current range: 3-45 mA
- 25MHz clock frequency
- Schmitt trigger input
- Supply voltage 3.3V/5V

■ Package

- LN5024SR:SOP24
- LN5024DR:DIP24
- LN5024PR:SSOP24（0.635-D1.4）
- LN5024FR:SSOP24（1.0-D1.50）

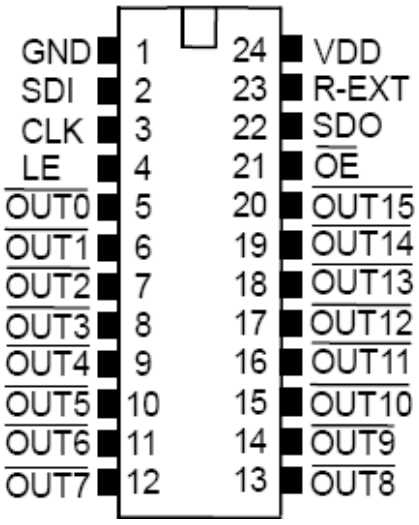
■ Applications

- White LED Backlighting
- LCD Display Supply
- Horse race lamp

■ Ordering Information

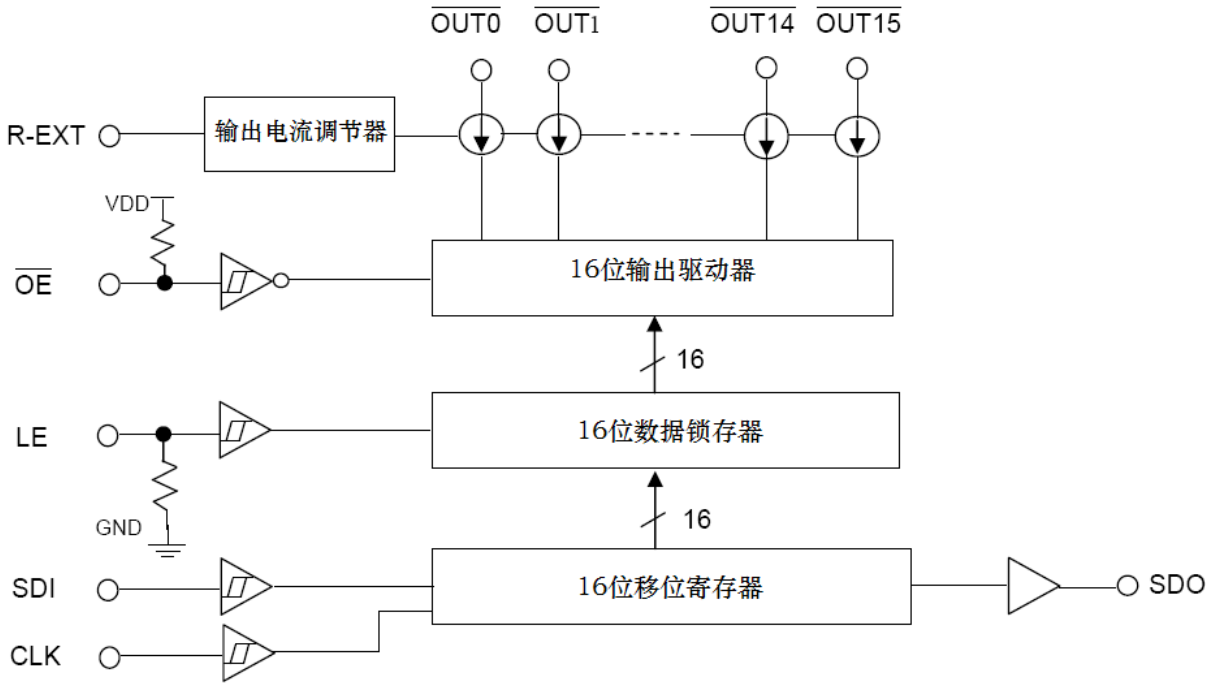
Model	Package
LN5024DR	P-DIP24-300-2.54
LN5024SR	SOP24-300-1.27
LN5024PR	SSOP24（0.635-D1.40）
LN5024FR	SSOP24（1.0-D1.50）

■ Pin Configuration



Pin Number	Pin Name	Pin Function
1	GND	Power Ground
2	SDI	Serial data input
3	CLK	Serial clock input
4	LE	Data latch enable (Active HIGH)
5～20	$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant output
21	$\overline{OE}$	Current output enable (Active LOW)
22	SDO	Serial data output
23	R-EXT	External resistor connection terminal
24	VDD	5V Power Input

■ Block Diagram



■ Absolute Maximum Ratings

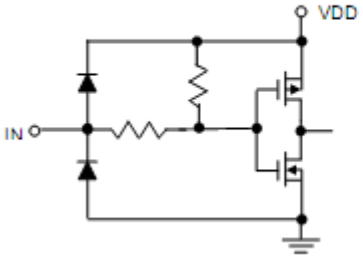
(T_A=25℃)

Parameter	Symbol		Absolute maximum ratings	Units
Power supply voltage	V_{DD}		GND-0.3～7	V
Input voltage	V_{IN}		-0.3~VDD+0.3	V
Output voltage	V_{OUT}		-0.5~20	V
Output current	I_{OUT}		70	mA
GND current	I_{GND}		1.0	A
Data clock frequency	Fclk		25	MHz
Operating temperature range	Topr		-40~85	℃
Storage temperature range	Tstg		-65~150	℃
Lead temperature(Soldering,10 sec)	Tref		260	℃
Power Dissipation（On PCB board）	P_D	DIP24	2.3	W
		SOP24	2.1	
		SSOP24(0.635-D1.4)	1.4	
		SSOP24(1.0-D1.5)	1.9	
Package Thermal Resistance $R_{th(j-a)}$（On PCB board）	P_D	DIP24	53.8	℃/W
		SOP24	49.8	
		SSOP24(0.635-D1.4)	88.5	
		SSOP24(1.0-D1.5)	66.7	

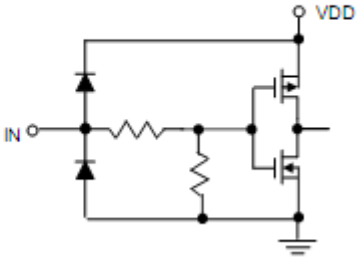
Caution: The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Equivalent Circuits of Inputs and Outputs

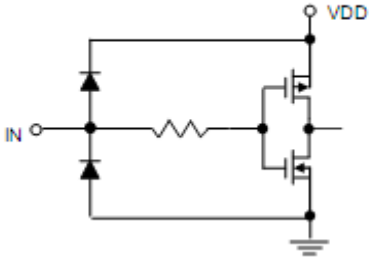
$\overline{OE}$ terminal



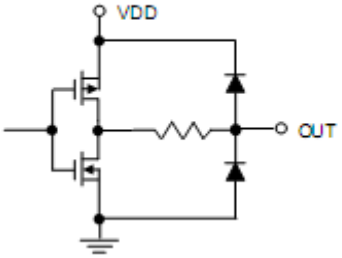
LE terminal



CLK, SDI terminal



SDO terminal



■ Electrical Characteristics

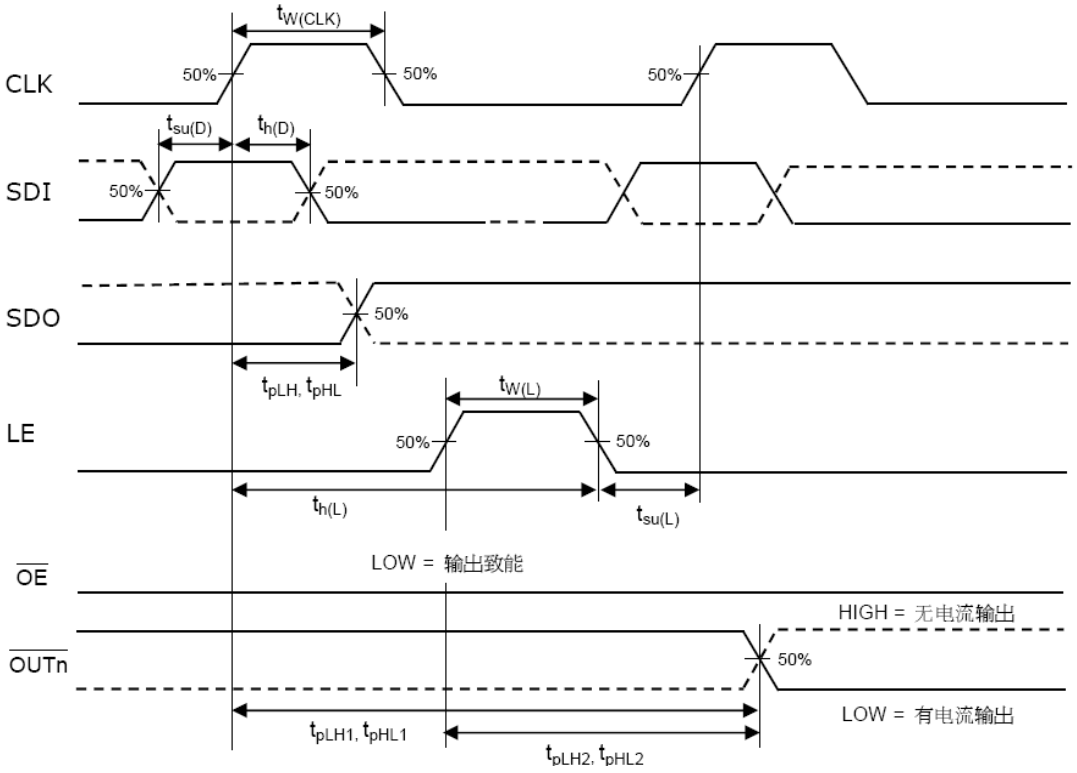
VDD=5V (Ta=25℃,except specify)

Parameter	Symbol	Test Condtion	Min.	Typ.	Max.	Units
Power supply voltage	V_{DD}		4.5	5	5.5	V
Supply current	Idd（off）1	Rext not connect, $\overline{OUT0}$ ~ $\overline{OUT15}$ =off	-	3.6	5.5	mA
	Idd（off）2	Rext=1.24K, $\overline{OUT0}$ ~ $\overline{OUT15}$ =off	-	4	6.5	mA
	Idd（off）3	Rext=620, $\overline{OUT0}$ ~ $\overline{OUT15}$ =off	-	6	9.0	mA
	Idd（on）1	Rext=1.24K	-	4.5	7	mA
	Idd（on）2	Rext=620	-	6.5	9.5	mA
Undervoltage lockout threshold	V_{UVLO}		-	2.5	-	V
Output voltage	V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$	0.4	-	17.0	V
Output current	I_{OUT}	$\overline{OUT0}$ ~ $\overline{OUT15}$	3	-	45	mA
	I_{SDO}	SDO	-0.9	-	0.9	mA
Input voltage	V_{IH}		$0.8V_{DD}$	-	V_{DD}	V
	V_{IL}		GND	-	$0.3V_{DD}$	
Output current	Iout	Vds=1.0V，Rext=1240Ω	-	15	-	mA
		Vds=1.0V，Rext=620Ω	-	30	-	mA
Current matching	$I_{OUT-OUT-ERR}$	10mA<Iout<40mA Vds=1.0V	-	±1	±3	%
Current accurcy	I_{ERR}	3mA<Iout<45mA ,Vds=1.0V	-	±3	±6	%
Current linearity	$I_{LINEAR-VDS}$	1.0V<VDS<3V	-	±0.1	±0.5	%
	$I_{LINEAR-VDD}$	4.5V<VDD<5.5V	-	±1	±2.5	%
PULL-Up resistance	R_{IN-UP}	OE	300K	600K	1200K	Ω
PULL-Down resistance	$R_{IN-DOWN}$	LE	300K	600K	1200K	Ω
Input clock frequency	F_{CLK}	When IC concatenation	-	-	25M	Hz
Minimum pulse width	$t_{W-CLK-LE}$	CLK、LE	20	-	-	nS
	t_{W-OE}	OE	200	-	-	nS
SDI setup time	t_{su}		5			nS
SDI hold time	t_h		10			nS
Delay time	t_{PLH}，t_{PHL}		-	100	200	nS
CLK edge time	t_f ,t_r	Climb time and fall time	-	-	500	nS

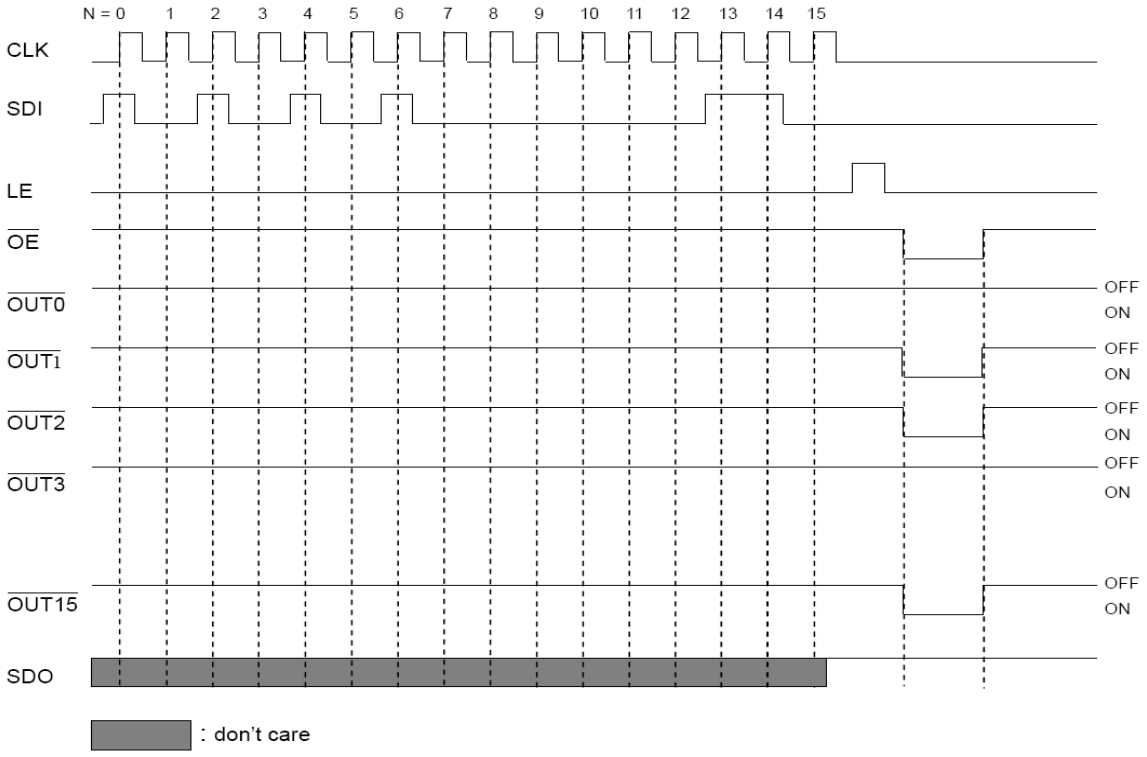
VDD=3.3V (Ta=25℃,except specify)

Parameter	Symbol	Test Condtion	Min.	Typ.	Max.	Units
power supply voltage	V_{DD}		3.0	3.3	3.5	V
Supply current	Idd（off）1	Rext not connect, $\overline{OUT0}$ ~ $\overline{OUT15}$ =off	-	1.5	4	mA
	Idd（off）2	Rext=1.86K, $\overline{OUT0}$ ~ $\overline{OUT15}$ =off	-	3.5	6.5	mA
	Idd（off）3	Rext=750, $\overline{OUT0}$ ~ $\overline{OUT15}$ =off	-	5.5	8.5	mA
	Idd（on）1	Rext=1.86K	-	3.5	6	mA
	Idd（on）2	Rext=750	-	5.5	8.5	mA
Undervoltage lockout threshold	V_{UVLO}		-	2.5	-	V
Output voltage	V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$	0.4	-	17.0	V
Output current	I_{OUT}	$\overline{OUT0}$ ~ $\overline{OUT15}$	3	-	30	mA
	I_{SDO}	SDO	-0.9	-	0.9	mA
Input voltage	V_{IH}		0.8VDD	-	VDD	V
	V_{IL}		GND	-	0.3VDD	
Output current	Iout	Vds=1.0V，Rext=1240Ω	-	10	-	mA
		Vds=1.0V，Rext=620Ω	-	25	-	mA
Current matching	$I_{OUT-OUT-ERR}$	10mA<Iout<40mA Vds=1.0V	-	±1	±3	%
Current accurcy	I_{ERR}	3mA<Iout<45mA ,Vds=1.0V	-	±3	±6	%
Current linearity	$I_{LINEAR-VDS}$	1.0V<VDS<3V	-	±0.1	±0.5	%
	$I_{LINEAR-VDD}$	4.5V<VDD<5.5V	-	±1	±2.5	%
PULL-Up resistance	R_{IN-UP}	OE	300K	600K	1200K	Ω
PULL-Down resistance	$R_{IN-DOWN}$	LE	300K	600K	1200K	Ω
Input clock frequency	F_{CLK}	When IC concatenation	-	-	25M	Hz
Minimum pulse width	$t_{W-CLK-LE}$	CLK、LE	40	-	-	nS
	t_{W-OE}	OE	300	-	-	nS
SDI setup time	t_{su}		10			nS
SDI hold time	t_h		20			nS
Delay time	t_{PLH}，t_{PHL}		-	150	300	nS
CLK edge time	tf ,tr	Climb time and fall time	-	-	500	nS

■ Timing Waveforms



■ Timing Diagram



■ Truth Table

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}$ … $\overline{OUT7}$ … $\overline{OUT15}$	SDO
↑	H	L	D_n	$\overline{D_n}$ ……. $\overline{D_{n-7}}$ ….. $\overline{D_{n-15}}$	D_{n-15}
↑	L	L	D_{n+1}	不变	D_{n-14}
↑	H	L	D_{n+2}	$\overline{D_{n+2}}$ ….. $\overline{D_{n-5}}$ …. $\overline{D_{n-13}}$	D_{n-13}
↓	X	L	D_{n+3}	$\overline{D_{n+2}}$ …. $\overline{D_{n-5}}$ …. $\overline{D_{n-13}}$	D_{n-13}
↓	X	H	D_{n+3}	使LED不亮	D_{n-13}

■ Application Information

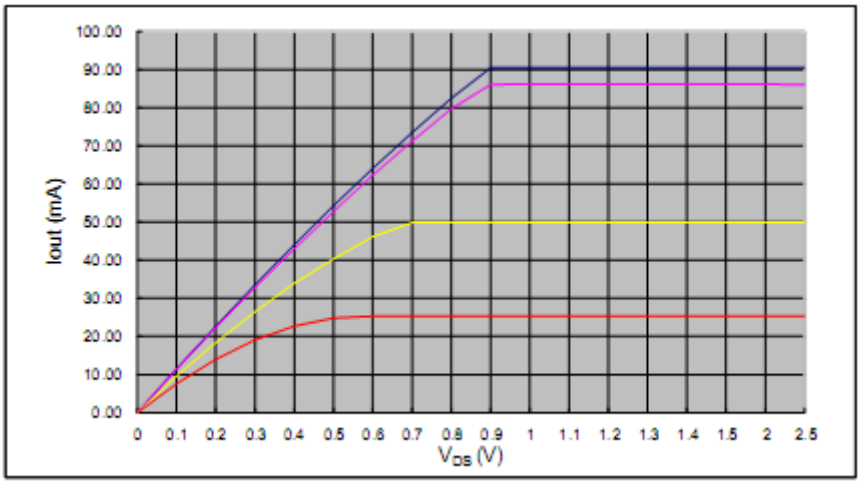
Constant Current

In LED display application, LN5024 provides nearly no variations in current from channel to channel and from IC to IC. This can be achieved by:

$$I_{OUT} = \frac{V_{R-EXT}}{R_{EXT}} \times 15, \quad V_{R-EXT} = 1.26V$$

1) The maximum current variation between channels is less than ±3%, and that between ICs is less than ±6%.

2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages (Vf). This performs as a perfection of load regulation.

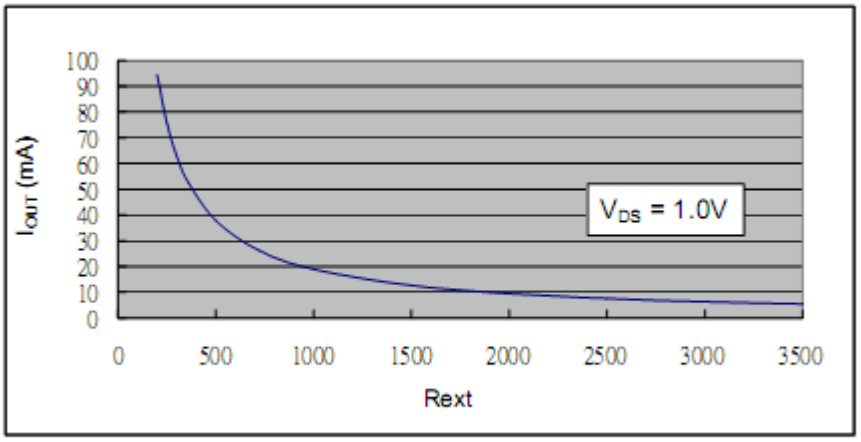


Adjusting Output Current

The output current of each channel (I_{OUT}) is set by an external resistor, Rext. The relationship between Iout and Rext is shown in the following figure.

Also, the output current can be calculated from the equation: $V_{R\text{-}EXT}$ = 1.26V； I_{OUT} = ($V_{R\text{-}EXT}$ / Rext) x 15

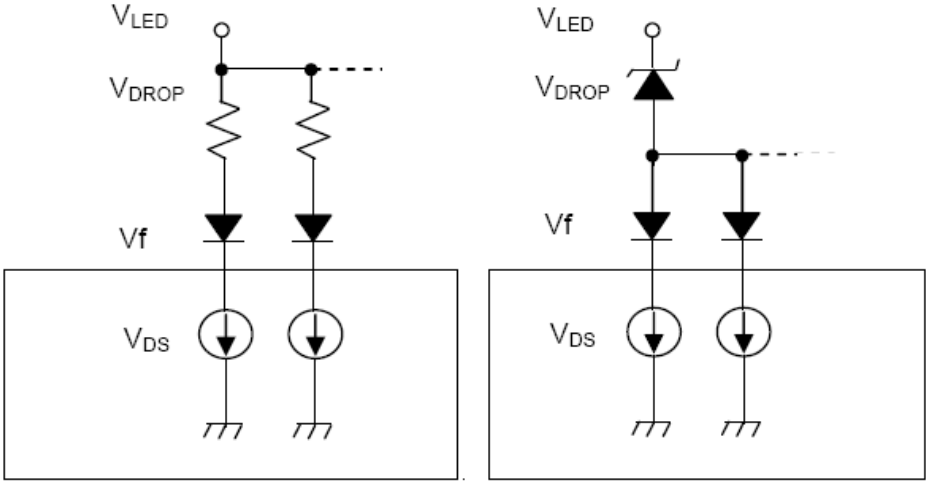
where Rext is the resistance of the external resistor connected to $R_{\text{-}EXT}$ terminal and $V_{R\text{-}EXT}$ is the voltage of $R_{\text{-}EXT}$ terminal. The magnitude of current (as a function of Rext) is around 150mA at 1260Ω and 30mA at 630Ω.



Resistance of the external resistor, R_{ext}, in Ω

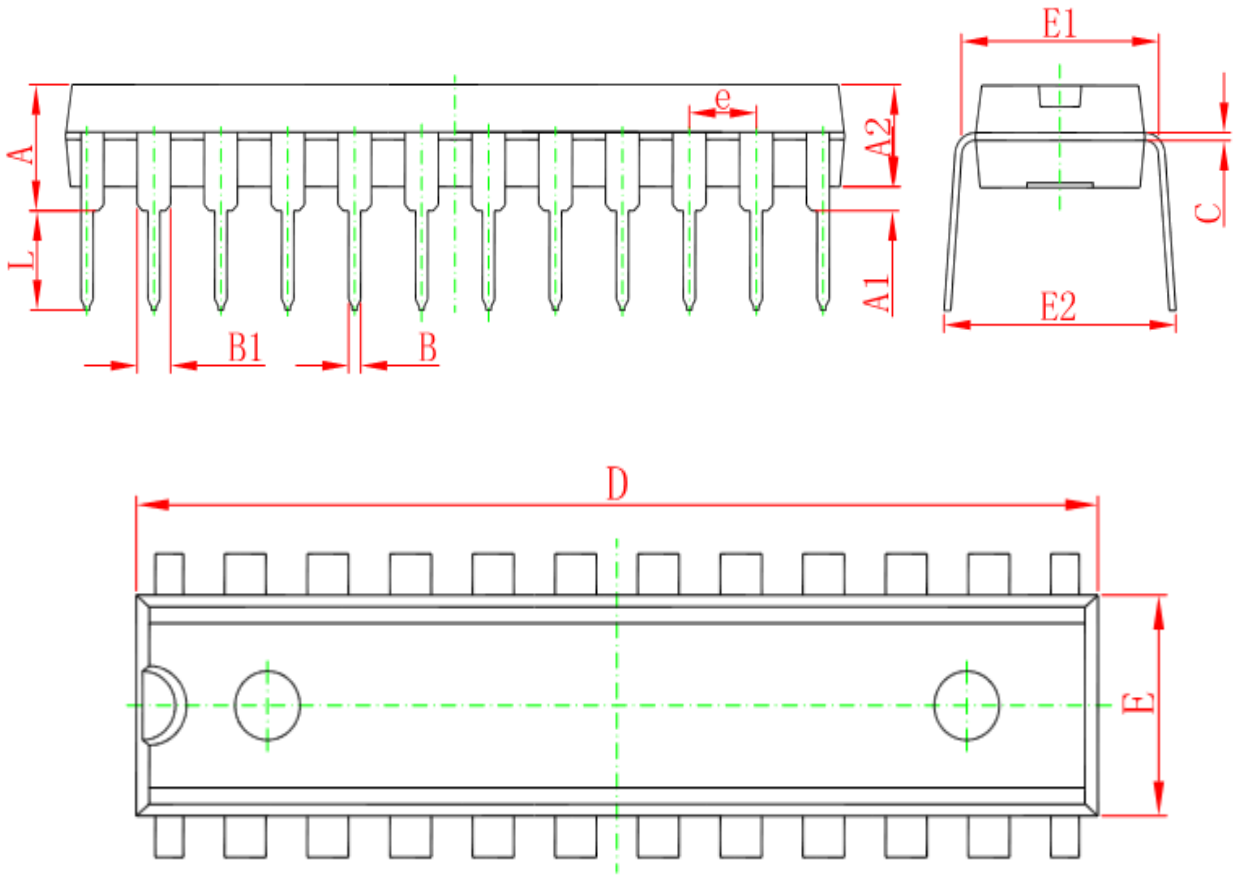
Load Supply Voltage (VLED)

LN5024 are designed to operate with V_{DS} ranging from 0.4V to 1.0V considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D(act)} > P_{D(max)}$ when V_{LED}= 5V and $V_{DS} = V_{LED} – Vf$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}. A voltage reducer lets $V_{DS} = (V_{LED} – Vf) – V_{DROP}$. Resistors or Zener diode can be used in the applications as shown in the following figures.



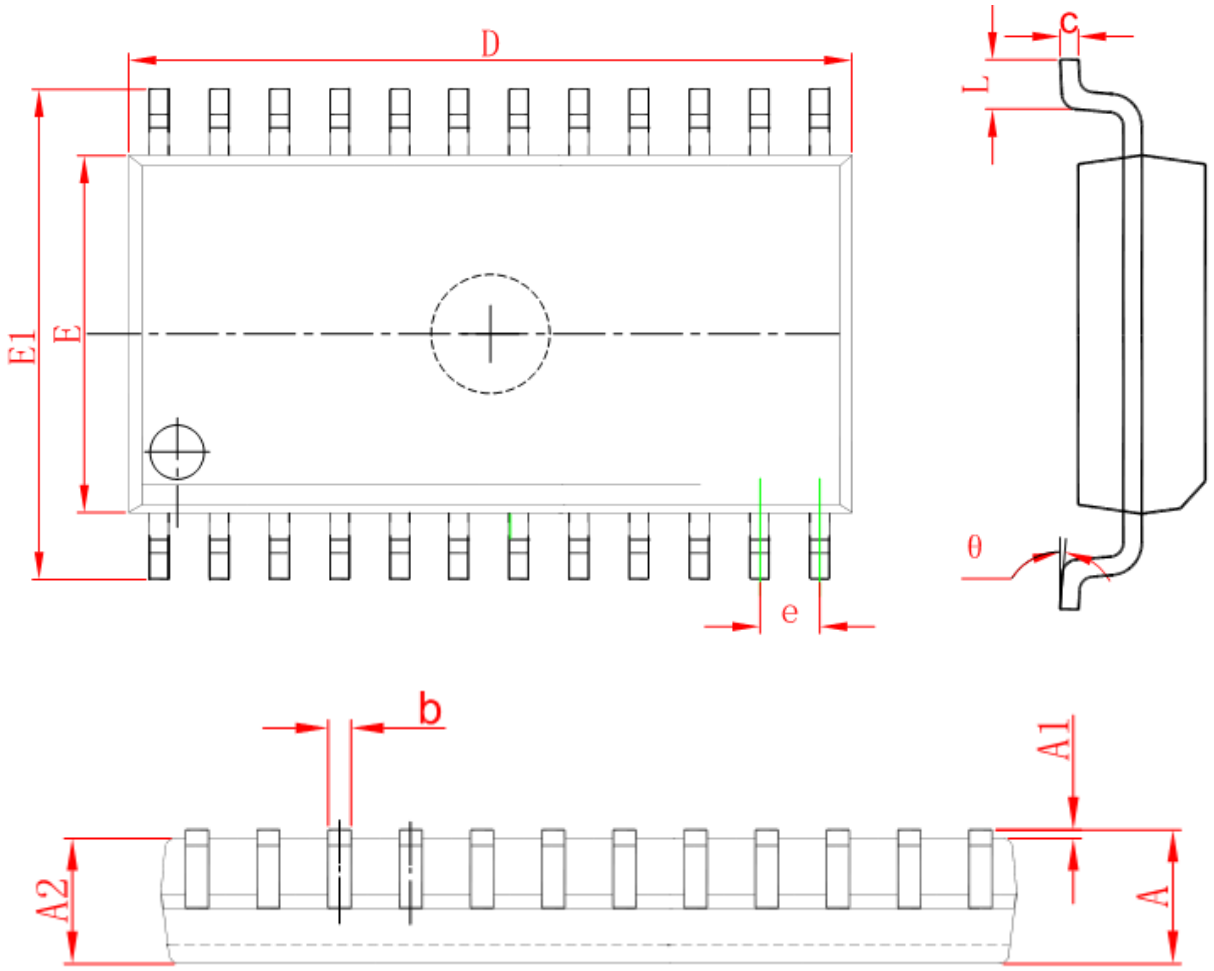
■ Package Information

- **DIP24(LN5024DR)**



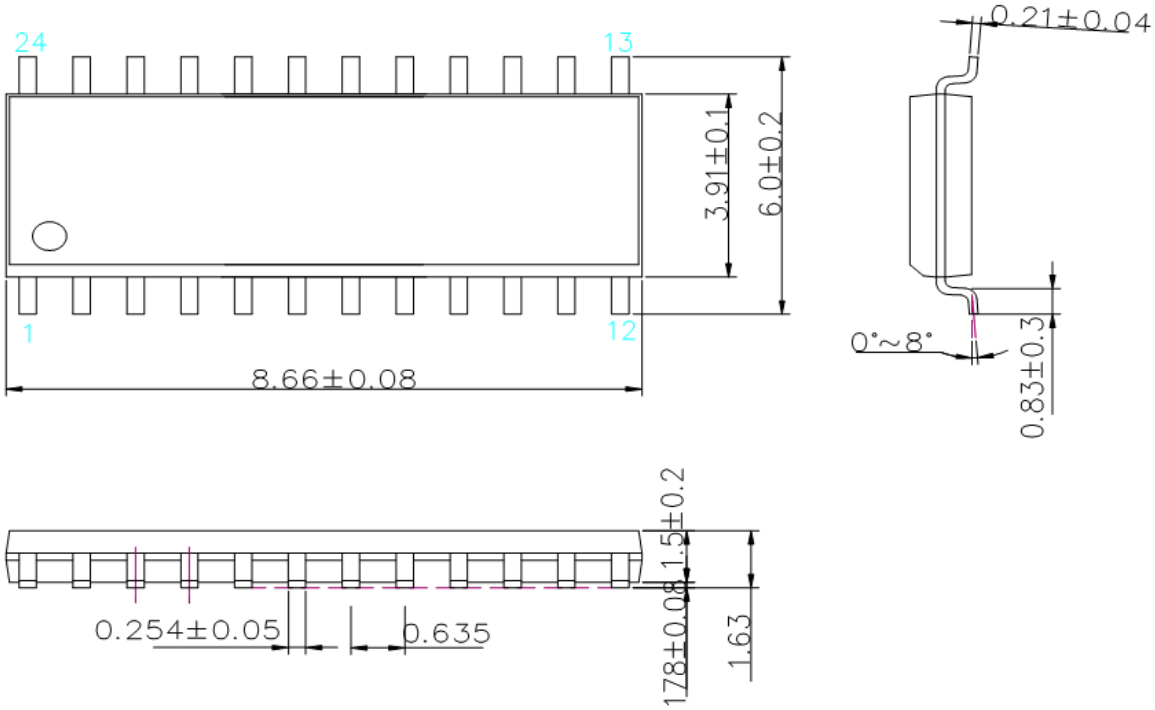
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.270 (BSC)		0.050 (BSC)	
C	0.204	0.360	0.008	0.014
D	29.250	29.850	1.152	1.175
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

- **SOP24（LN5024CR）**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.100	2.500	0.083	0.098
b	0.330	0.510	0.013	0.020
c	0.204	0.330	0.008	0.013
D	15.200	15.600	0.598	0.614
E	7.400	7.600	0.291	0.299
E1	10.210	10.610	0.402	0.418
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

- **SSOP24（0.635-D1.4）（LN5024PR）**



- **SSOP24（1.0-D1.5）（LN5024FR）**