Voltage Detectors With Adjustable Delay Circuit External

■ General Description

The LN802 is a cost-effective system supervisor Integrated Circuit (IC) designed to monitor VCC in digital and mixed signal systems and provide a warning signal when the system power supply is out of working range, and a reset signal to the host processor when necessary.

It features low supply current. CMOS output configurations is available. Delay time can be set by a external capacitor.

■ Features

Precision VCC Monitor for 1.63,1,93,2.63V, 2.93V, 3.08V, 4.00V ,4.38V and4.63V

Highly Accurate: ±2%

■ Ordering Information

Low Power Consumption : typical 3μA

Operating Voltage Range: 1V ~ 6.0V

Detect Voltage Temperature Characteristics: ±100ppm/℃ (TYP.)

Output Configuration: CMOS

■ Applications

Microprocessor reset circuitry

Memory battery back-up circuits

Power-on reset circuits

Power failure detection

System battery life and charge voltage monitors

Delay circuitry

LN802 ①②③④⑤⑥⑦

| Designator	Description	Symbol	Description
①	Output Configuration	C	CMOS output
②③④	Detect Voltage	263	2.63V
		293	2.93V
		308	3.08V
		400	4.00V
		438	4.38V
		463	4.63V
⑤	Detect Accuracy	1	Within ± 1.0%
		2	Within ± 2.0%
⑥	Package	K	SOT-343L
⑦	Device Orientation	R	Embossed tape, standard feed
		L	Embossed tape, reverse feed

■ PIN Assignment

SOT-343L
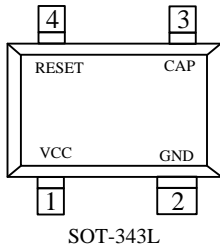
PIN NO.	SYMBOL	DESCRIPTION
1	RESET	Output.Active High
2	VCC	Power
3	GND	Ground
4	N.C.	No Connected
5	CAP	Delay Timer set Pin

■ Marking

SOT-343
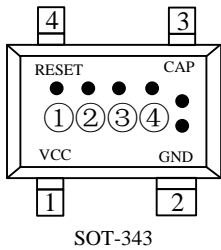
① ② represent the Output type and Voltage threshold.

CMOS(LN802C series)

SYMBOL	OUTPUT TYPE	VDET(V)
CA	CMOS	4.63
CB	CMOS	4.38
CC	CMOS	4.00
CD	CMOS	3.08
CE	CMOS	2.93
CF	CMOS	2.63
CG	CMOS	1.93
CH	CMOS	1.63

③：Represent the Accurate of the VDET.

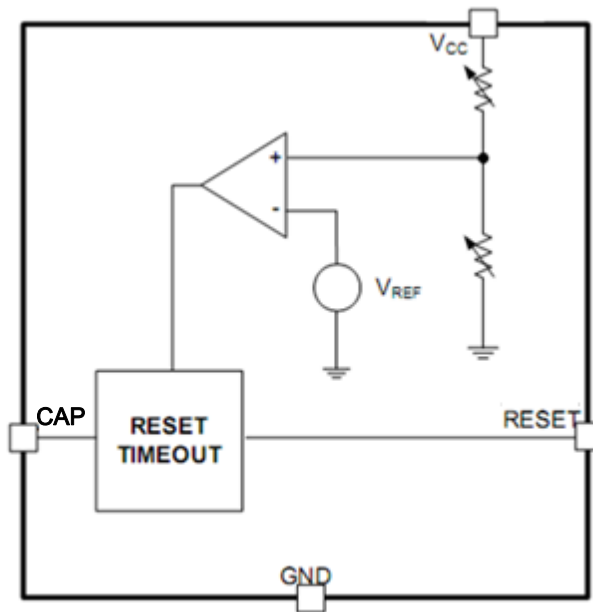| SYMBOL	ACCURATE
2	±2%

④ Represent the lot No

Note: six "." represent the information of product quality

■ Typical Application Circuit
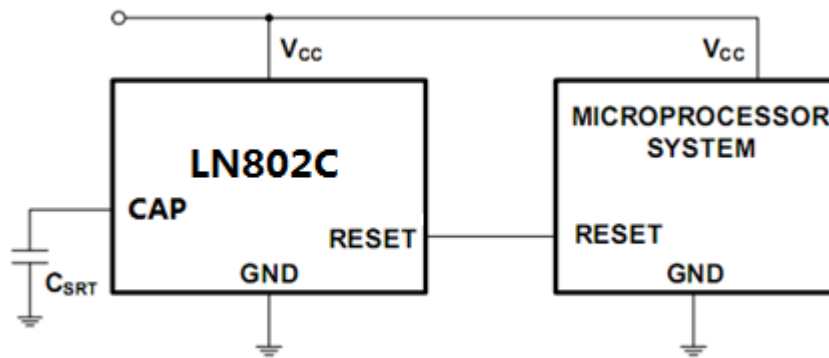
■ Function Block Diagram

■ Absolute Maximum Ratings

Parameter		Symbol	Maximum Rating	Unit
Input Supply Voltage		V_{CC}	6	V
Output Current		I_{RESET}	30	mA
Output Voltage	CMOS	V_{RESET}	VSS -0.3 ~ VIN + 0.3	V
Power Dissipation	SOT-23-5L	Pd	350	mW
Operating Temperature Range		Topr	-30~+85	℃
Storage Temperature Range		Tstg	-40~+125	℃

■ Electrical Characteristics

| Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Detect Voltage	VDF		VDF(T) x 0.98	VDF(T)	VDF(T) x 1.02	V
Hysteresis Range	VHYS		-	4*VDF	-	mV
Supply Current	ISS	VIN = 5V		3.0	5.0	μA
Operating Voltage	VCC	VDF= 2.63V to 4.63V	0.7		6	V
Output Current	I_{RESET}	NMOS VCC=6V		30		mA
		PMOS VCC=6V		-30		
Detect Voltage Temperature Characteristics	ΔVDF ΔTopr· VDF			±100		ppm/℃

■ Operational Explanation

CMOS output(the 4th is the most important)

① When a voltage higher than the release voltage (VDR) is applied to the voltage input pin (VCC), the voltage will gradually fall. When a voltage higher than the detect voltage (VDF) is applied to VIN, output (RESRT) will be equal to the ground voltage.

② When VCC falls below VDF, RESET will be equal to the VIN voltage.

③ When VCC falls to a level below that of the minimum operating voltage (VMIN) output will become unstable.

④ When VCC rises above the VSS level (excepting levels lower than minimum operating voltage), RESET will be equal to VSS until VCC reaches the VDR level.

⑤ Although VCC will rise to a level higher than VDR, RESET maintains VIN voltage level via the delay circuit.

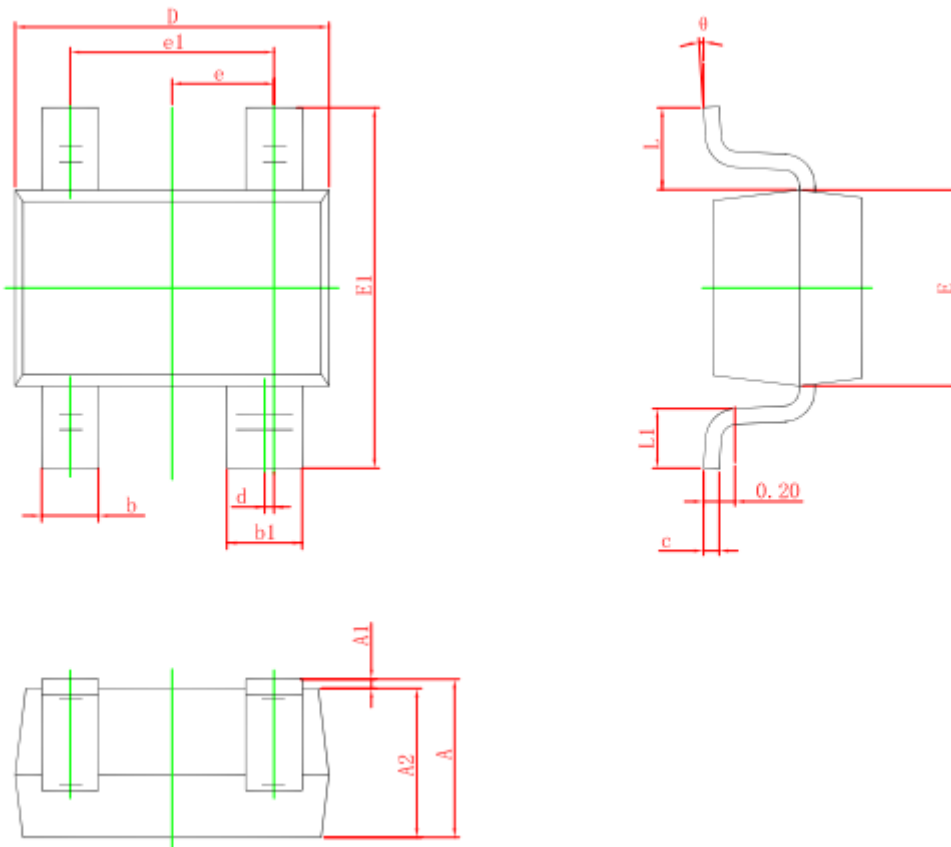⑥ Following transient delay time, VSS will be output at RESET.

Notes:

Timing Chart
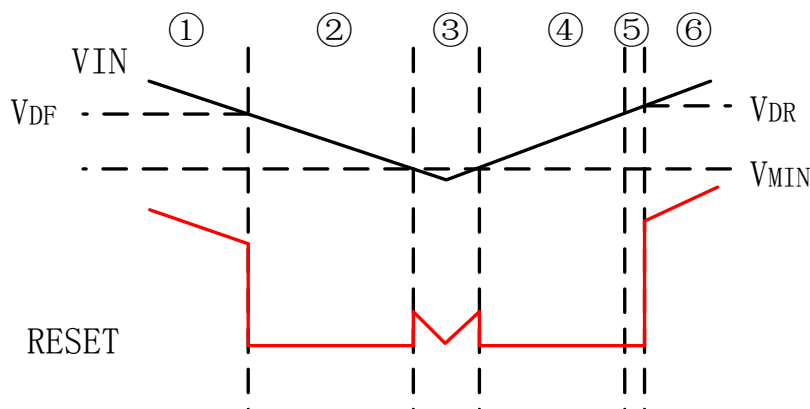
Delay time can be set by external capacitor

$Tdly=3.8 \times 10^{-6} \times C_{SR.}$

■ **Package Information**

● **SOT-343L**

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.250	0.400	0.010	0.016
b1	0.350	0.500	0.014	0.020
c	0.080	0.150	0.003	0.006
d	0.050 TYP.		0.002 TYP.	
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 TYP.		0.026 TYP.	
e1	1.200	1.400	0.047	0.055
L	0.525 REF.		0.021 REF.	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°