Voltage Detectors With Delay Circuit Built-In

■ General Description

The LN809 is a cost-effective system supervisor Integrated Circuit (IC) designed to monitor VCC in digital and mixed signal systems and provide a warning signal when the system power supply is out of working range, and a reset signal to the host processor when necessary. No external components are required.

It features low supply current. Both CMOS and N-channel open drain output configurations are available. Since the delay circuit is built-in, peripherals are unnecessary and high density mounting is possible.

■ Features

- Precision VCC Monitor for 2.63V, 2.93V, 3.08V, 4.00V ,4.38V and4.63V
- Highly Accurate: ± 1%, ± 2%
- Low Power Consumption : lower than 1.5μA
- Operating Voltage Range: 0.7V ~ 6.0V
- Detect Voltage Temperature Characteristics: ± 100ppm/℃(TYP.)
- Built-In Delay Circuit (typ): Typical Values 50ms 100ms 200ms 400ms optional
- Output Configuration: N-channel open drain or CMOS

■ Applications

- Microprocessor reset circuitry
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure detection
- System battery life and charge voltage monitors
- Delay circuitry

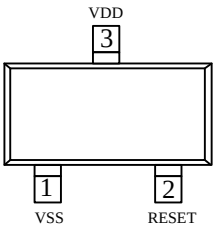
■ Ordering Information

LN809 ①②③④⑤⑥⑦

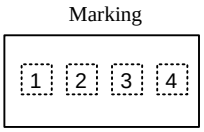
Designator	Description	Symbol	Description
①	Output Configuration	C	CMOS output
		N	N-ch open drain output
② ③	Detect Voltage	26	2.63V
		29	2.93V
		30	3.08V
		40	4.00V
		43	4.38V
		46	4.63V
④	Output Delay	1	70ms-150ms
		2	330ms-500ms
		4	150ms-270ms
		5	30ms-80ms
⑤	Detect Accuracy	1	Within ± 1.0%
		2	Within ± 2.0%
⑥	Package	M	SOT-23-3L
		V	SOT-23-3B
⑦	Device Orientation	R	Embossed tape, standard feed
		L	Embossed tape, reverse feed

■ Package

- **SOT-23-3L/B**



SOT-23-3
(TOP VIEW)



■ Marking

①② Represents integer of detect voltage and output configuration

CMOS output (LN809C series)

Mark	Configuration	Voltage(V)
C1	CMOS	4.63
C2	CMOS	4.38
C3	CMOS	4.00
C4	CMOS	3.08
C5	CMOS	2.93
C6	CMOS	2.63

N-channel open drain (LN809N series)

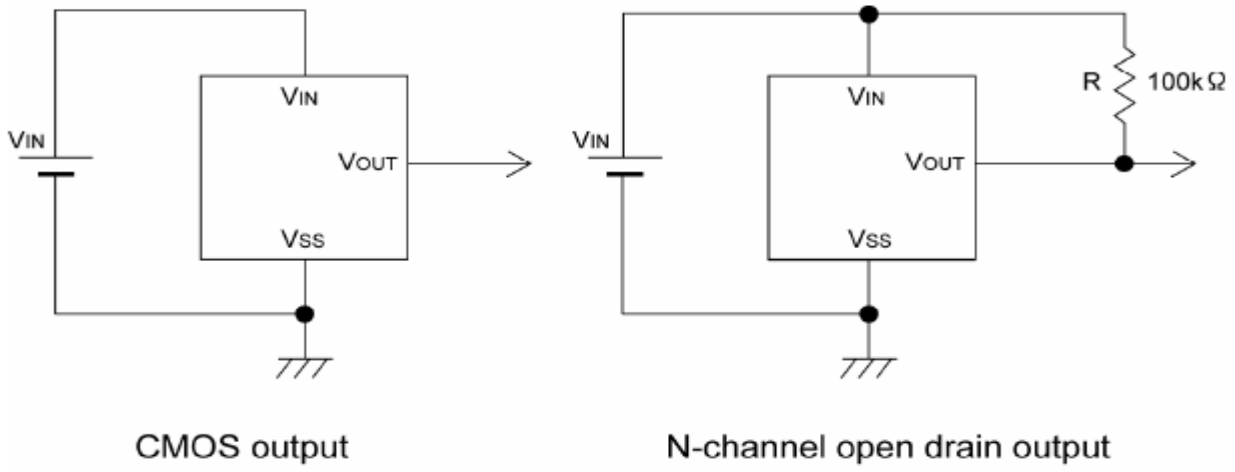
Mark	Configuration	Voltage(V)
N1	N-ch	4.63
N2	N-ch	4.38
N3	N-ch	4.00
N4	N-ch	3.08
N5	N-ch	2.93
N6	N-ch	2.63

③ Represents delay time

Mark	Delay Time
5	70ms-150ms
8	330ms-500ms
6	150ms-270ms
7	30ms-80ms

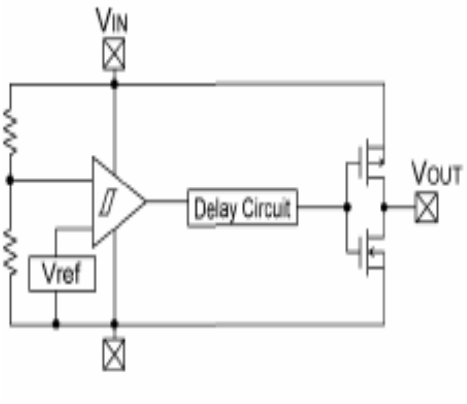
④ Represents assembly lot number (Based on internal standards)

■ Typical Application Circuit

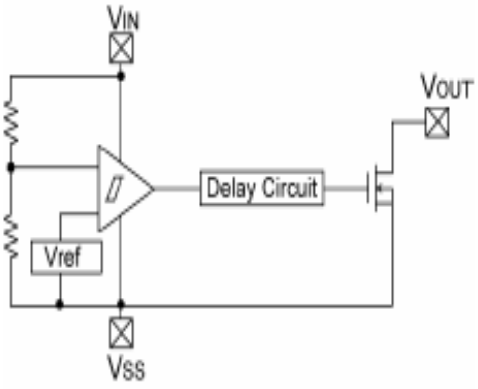


■ Function Block Diagram

(1) CMOS output



(2) N-channel open drain output



■ Absolute Maximum Ratings

Parameter		Symbol	Maximum Rating	Unit
Input Supply Voltage		V_{IN}	6	V
Output Current		IOUT	30	mA
Output Voltage	CMOS	VOUT	VSS -0.3 ~ VIN + 0.3	V
	N-ch open drain		VSS -0.3 ~ 6	
Power Dissipation	SOT-23-3	Pd	150	mW
Operating Temperature Range		Topr	-30～+85	℃
Storage Temperature Range		Tstg	-40～+125	℃

■ Electrical Characteristics

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Detect Voltage	VDF			VDF(T) x 0.98	VDF(T)	VDF(T) x 1.02	V
Hysteresis Range	VHYS			VDF x 0.002	VDF x 0.005	VDF x 0.008	V
Supply Current	ISS	VIN = 1.5V			1.0	1.2	μA
		VIN = 2.0V			1.0	1.3	
		VIN = 3.0V			1.1	1.3	
		VIN = 4.0V			1.1	1.3	
		VIN = 5.0V			1.2	1.5	
Operating Voltage	VIN	VDF= 2.63V to 4.63V		0.7		6	V
Output Current	IOUT	N-ch VDF =0.5V	VIN = 1.5V		2		mA
			VIN = 2.0V		7		
			VIN = 3.0V		10		
			VIN = 4.0V		11		
			VIN = 5.0V		13		
		CMOS, P-ch VDF=2.63V VIN = 6.0V			-10		
Detect Voltage Temperature Characteristics	ΔVDF ΔTopr· VDF				±100		ppm/℃
Transient Delay Time (VDR → VOUT inversion)	TDLY	LN809***1***		70		150	ms
		LN809***2***		330		500ms	ms
		LN809***4***		150		270	ms
		LN809***5***		30		80	ms

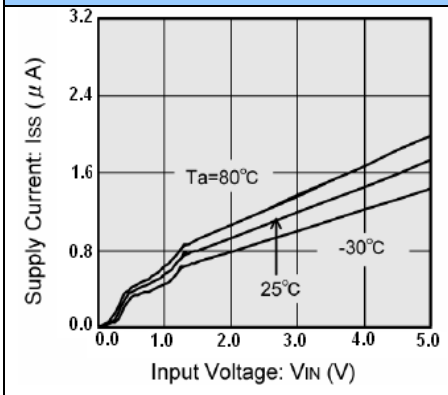
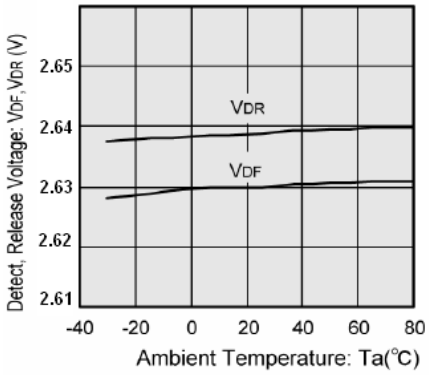
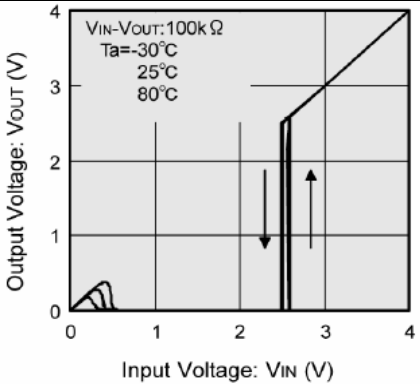
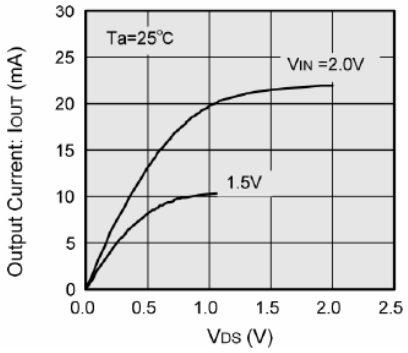
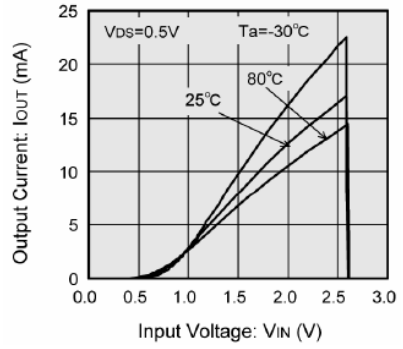
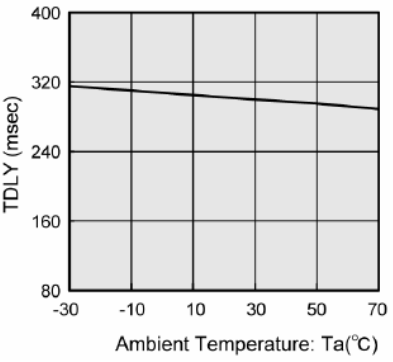
VDF (T): Setting detect voltage value

Release Voltage: VDR = VDF + VHYS

Note: The power consumption during power-start to output being stable (release operation) is 2μA greater than it is after that period (completion of release operation) because of delay circuit through current.

■ Typical Performance Characteristics

product for Test: VDF=2.63V

Supply Current vs. Input Voltage	Detect Voltage, Release Voltage vs. Ambient Temperature	Output Voltage vs. Input Voltage
		
N-Channel Driver Output Current vs. VDS	**N-Channel Driver Output Current vs. Input Voltage**	**Ambient Temperature vs. Transient Delay Time**
		

■ Operational Explanation

- **CMOS output(the 4th is the most important)**

① When a voltage higher than the release voltage (VDR) is applied to the voltage input pin (VIN), the voltage will gradually fall. When a voltage higher than the detect voltage (VDF) is applied to VIN, output (VOUT) will be equal to the input at VIN.

Note that high impedance exists at VOUT with the N-channel open drain configuration. If the pin is pulled up, VOUT will be equal to the pull up voltage.

② When VIN falls below VDF, VOUT will be equal to the ground voltage (VSS) level (detect state). Note that this also applies to N-channel open drain configurations.

③ When VIN falls to a level below that of the minimum operating voltage (VMIN) output will become unstable. Because the output pin is generally pulled up with N-channel open drain configurations, output will be equal to pull up voltage.

④ When VIN rises above the VSS level (excepting levels lower than minimum operating voltage), VOUT will be equal to VSS until VIN reaches the VDR level. But if the rising rate is fast enough, VOUT is equal to the pull up voltage.

⑤ Although VIN will rise to a level higher than VDR, VOUT maintains ground voltage level via the delay circuit.

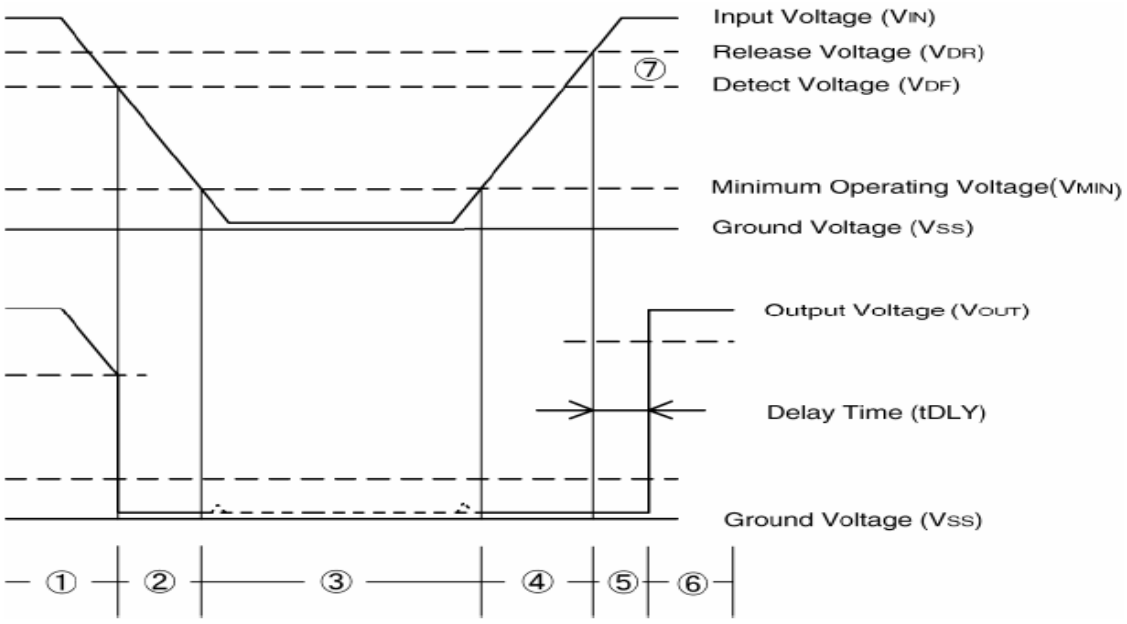
⑥ Following transient delay time, VIN will be output at VOUT. Note that high impedance exists with the N-channel open drain configuration and that voltage will be dependent on pull up.

Notes:

1. The difference between VDR and VDF represents the hysteresis range.

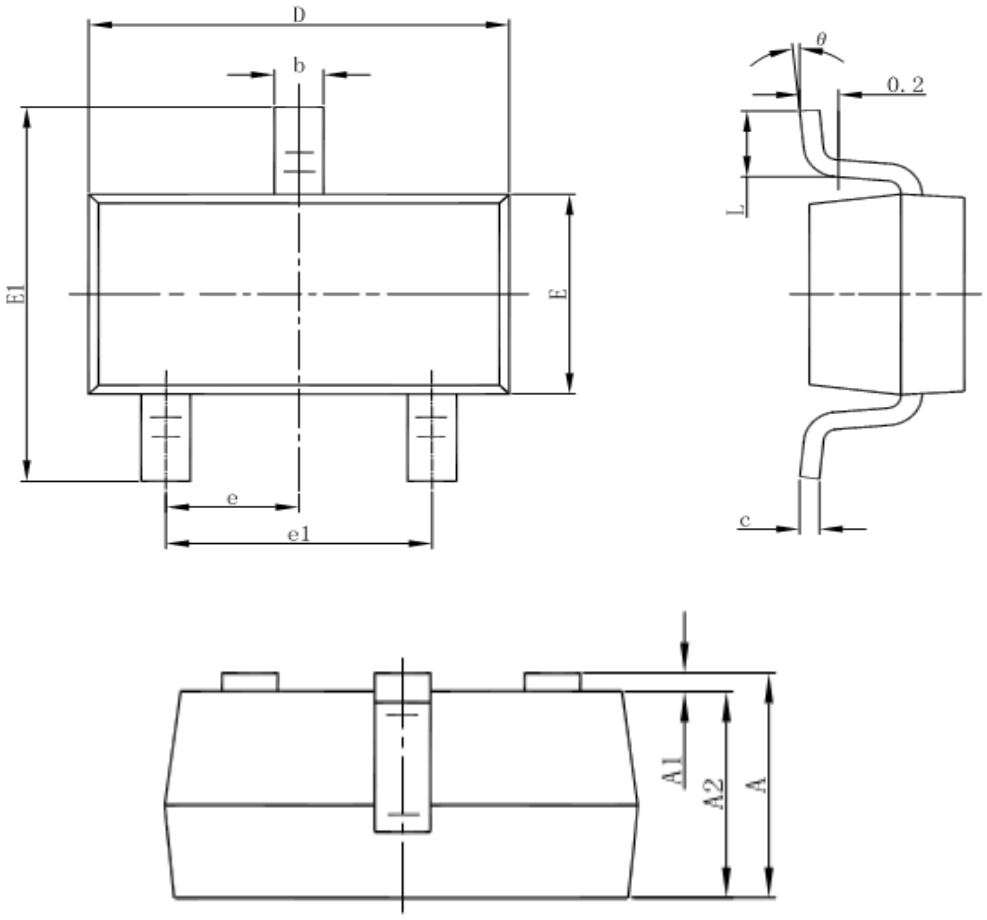
2. Propagation delay time (tDLY) represents the time it takes for VIN to appear at VOUT once the said voltage has exceeded the VDR level.

- **Timing Chart**



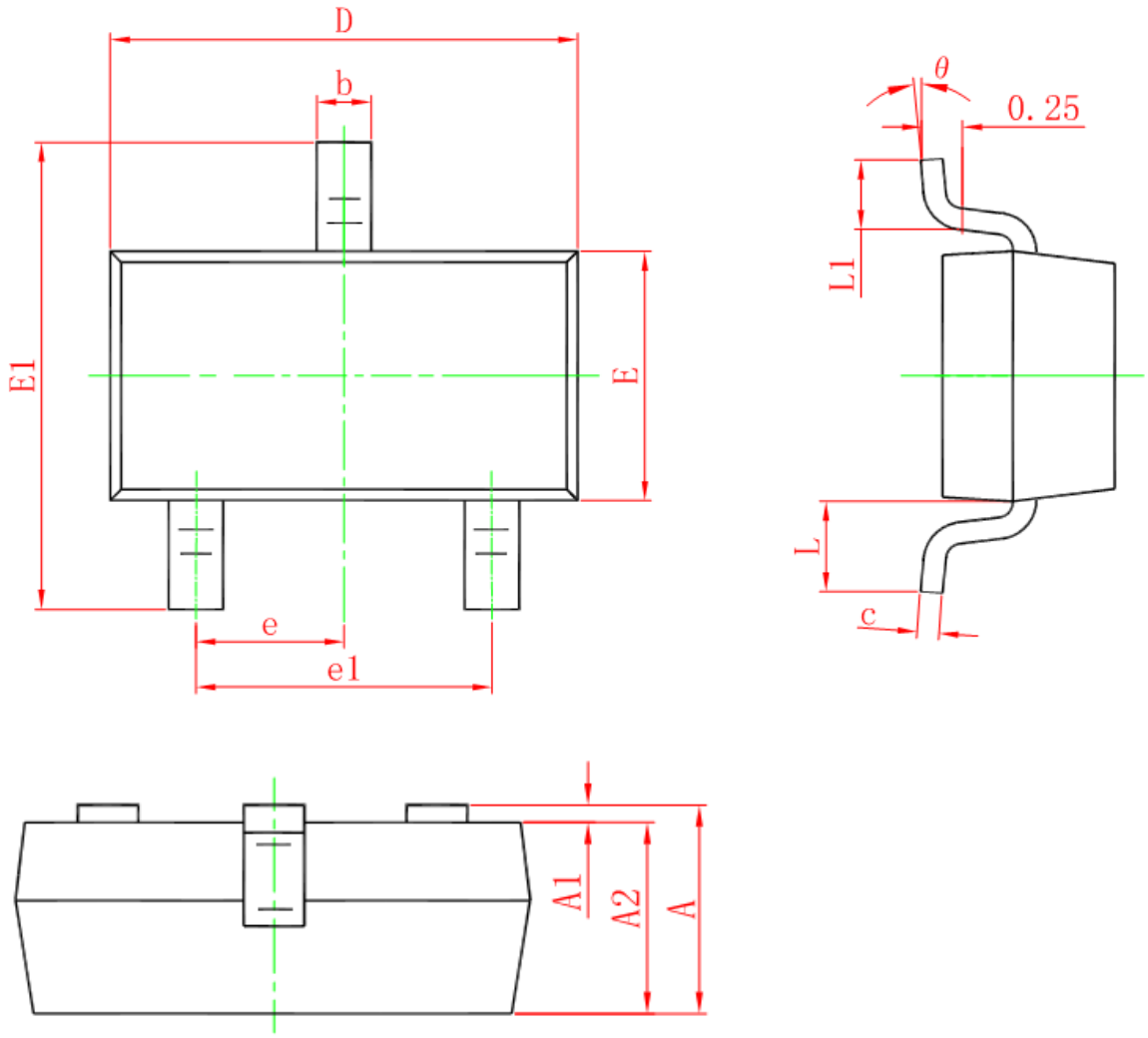
■ Package Information

- **SOT-23-3L**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

- **SOT-23-3B**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°