Built-in Delay Time High-Precision Low Power Voltage Detector

■ General Description

The LN819A series are the low power voltage detection chips for microprocessors and electronic systems. The characteristics of these chips are high precision and low temperature drift. The detection voltages of these series products basic cover most demands of the electronic products. Low static current is its important advantages. Two output forms, Nch open-drain and CMOS output, are available. The peripheral devices in the application circuit are less, for the built-in delay time mode.

■ Features

- Ultra-low current consumption: less than 2.5 μA typ.
- High-precision detection voltage: ±1.0 %, ±2.0 %
- Operating voltage range 0.7 V to 6.0 V
- CMOS output mode
- Detecting voltage temperature characteristics: ±100ppm/℃(TYP.)

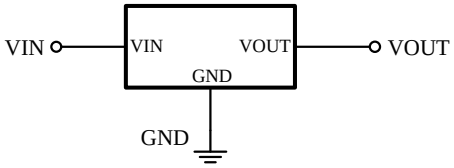
■ Applications

- The microprocessor reset circuit
- Battery backup memory circuits
- Power on reset circuit
- The source is invalid
- System battery life and charging voltage monitoring
- Time delay circuit

■ Package

- SOT-23-3L

■ Typical Application Circuit



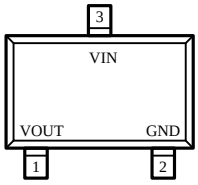
COMS Output

■ Ordering Information

LN819A ①②③④⑤

Item	Symbol	Description
①②	27	Detect Voltage：2.7V
③	2	Detect Accuracy: ±2%
④	M	Package Type: SOT-23-3L
⑤	R	Embossed Taped(Right)
	L	Embossed Taped(Left)

■ Pin Configurations



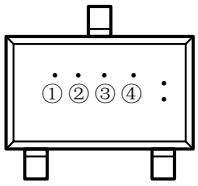
SOT-23-3L
(TOP VIEW)

■ Pin Assignment

Pin No. SOT-23-3L	Pin name	Pin description
3	VIN	Voltage input pin
2	GND	GND pin
1	VOUT	output pin

■ Marking Rule

- **SOT-23-3L**



SOT-23-3L
(TOP VIEW)

①②Represents the product name

Symbol	Product Description
19	LN819A◆◆◆◆◆◆◆

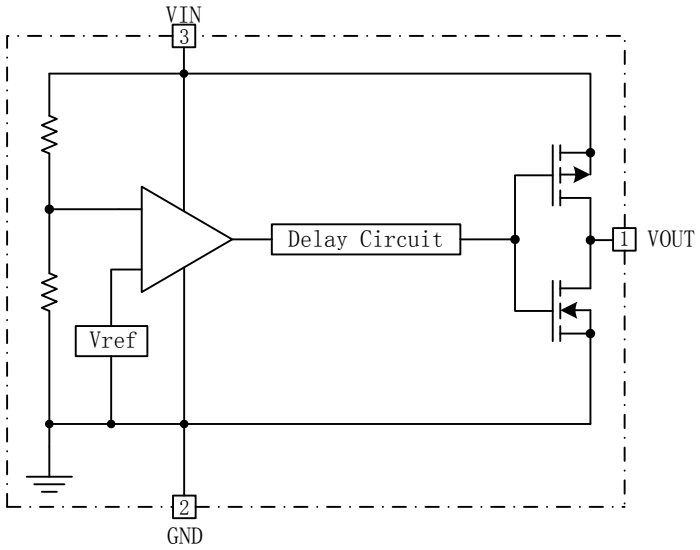
③Represents the detect voltage

Designatior	Detect Voltage（V）	Designatior	Detect Voltage（V）	Designatior	Detect Voltage（V）
1	1.8	C	2.9	N	4.0
2	1.9	D	3.0	P	4.1
3	2.0	E	3.1	Q	4.2
4	2.1	F	3.2	R	4.3
5	2.2	G	3.3	S	4.4
6	2.3	H	3.4	T	4.5
7	2.4	I	3.5	U	4.6
8	2.5	J	3.6	V	4.7
9	2.6	K	3.7	X	4.8
A	2.7	L	3.8	Y	4.9
B	2.8	M	3.9	Z	5.0

④Represents the batch number (based on the internal standard)

Notes: "• "represents the batch number. "• "says" 1 ", dot not said "0"; For example: dot on the top of the "③", and the top right of the "④", said "010010", used to track the product batch.

■ Function Block Diagram



■ Absolute Maximum Ratings

Item	Symbol	Absolute maximum ratings	unit
Power supply voltage	V_{IN}	6	V
Output current	IOUT	50	mA
Output voltage	VOUT	VSS -0.3 ~ VIN + 0.3	V
Power dissipation	Pd	150	mW
Operating ambient temperature range	Topr	-30～+85	℃
Storage temperature range	Tstg	-40～+125	℃

■ Electrical Characteristics

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Detection Voltage	VDF	-		VDF(T)* 0.98	VDF(T)	VDF(T)* 1.02	V
Hysteresis Voltage	VHYS	-		VDF* 0.002	VDF* 0.005	VDF* 0.01	V
Current Consumption	ISS	VIN = 1.5V		-	1.0	1.2	μA
		VIN = 2.0V		-	1.0	1.3	
		VIN = 3.0V		-	1.1	1.3	
		VIN = 4.0V		-	1.1	1.3	
		VIN = 5.0V		-	1.2	1.5	
Operating Voltage	VIN	-		0.7	-	6	V
Output Current	IOUT	N-ch VDF =0.5V	VIN = 1.5V	-	8	-	mA
			VIN = 2.0V	-	15	-	
			VIN = 3.0V	-	16	-	
			VIN = 4.0V	-	17	-	
			VIN = 5.0V	-	19	-	
		CMOS, P-ch VDF=2.63V VIN = 6.0V		-	-10	-	
Temperature Coefficient	ΔVDF ΔTopr ·VDF	-		-	±100	-	ppm/℃
Time Delay (VDR→VOUT)	TDLY	-		30	50	80	ms

VDF (T)：Detect Voltage

Release Voltage：VDR = VDF + VHYS

Note: Due to the delay current will have power, after the voltage recovery, the total power consumption will be bigger than the rating of the chip on the time delay circuit.

■ Operating annotation

- **CMOS output (Pay special attention to 4 points)**

① When the input voltage is higher than the release voltage (VDR), the voltage would gradually decrease. When the input voltage is higher than the detection voltage (VDF), the output voltage and the input voltage is equal.

Note: In the N-ch Open Drain Output circuit, using pull-up resistors, the output voltage should be equal to the pull-up voltage when the input voltage is high.

② When the input voltage fall below the detection voltage, the output voltage should equal to the ground voltage. The N-ch Open Drain Output circuit mode is the same function. When the input voltage is lower than the minimum operating voltage, the output voltage is unstable. The output voltage of the N-ch Open Drain Output circuit mode will be rising.

④ The input voltage is rosed from the ground potential (unlike the rises in higher than the minimum operating voltage potential), if the case of rising fast enough, the output voltage would be equal to the pull-up voltage, otherwise wiould be equal to the ground potential. After the delay time the output voltage is equal to the pull-up voltage.

⑤ When the input voltage is higher than the release voltage, the output voltage will keep potential until the end of the built-in time delay.

⑥ After the time delay, the input voltage will be equal to the output voltage. Pay attention, in the N-ch Open Drain Output

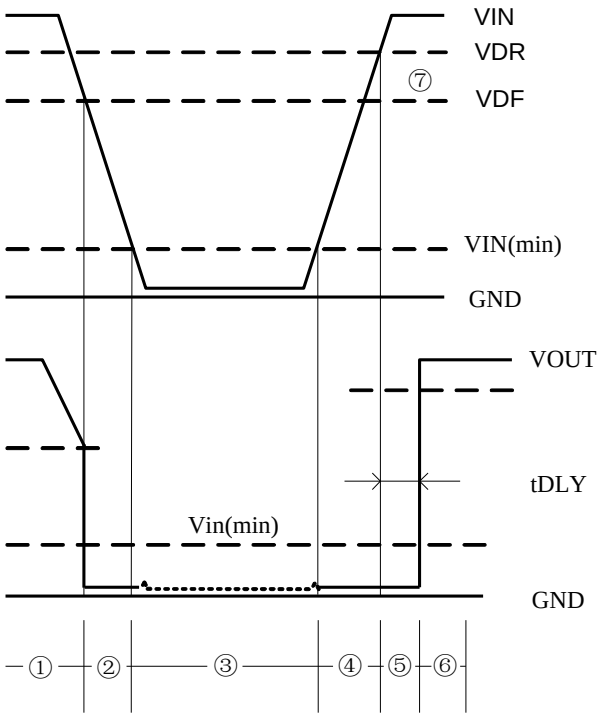
circuit, pull up resistors used to implement this functionality.

Note:

1. VDF= VDR+ VHYS (the Hysteresis Voltage)

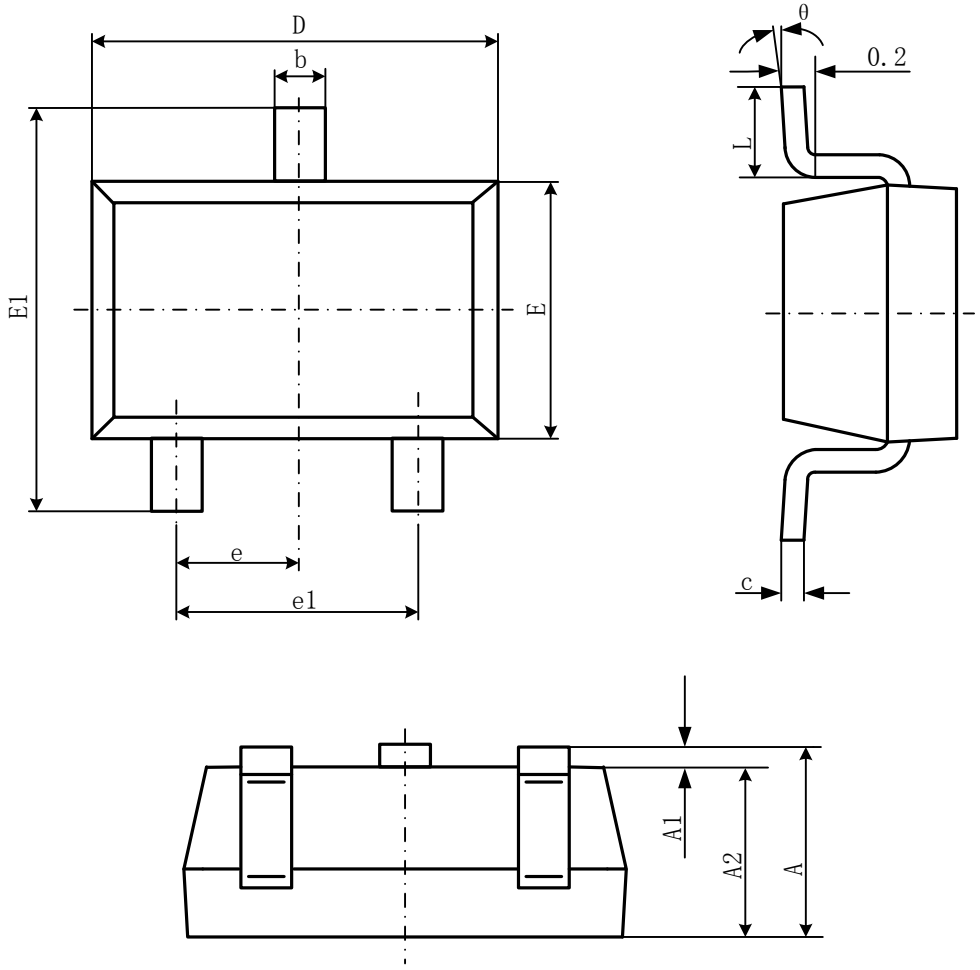
2. The built-in delay time (tDLY) is that of the output voltage turned into the input voltage, when the input voltage is restored to more than VDF.

- Timing Chart



■ Package

- SOT-23-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°