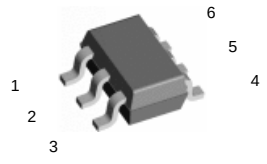
Dual N-Channel Enhancement-Mode MOSFET (20V, 6A)

LN9926LT1G



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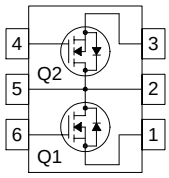
Description

This N-Channel 2.5V specified MOSFET is a rugged gate version of advanced trench process. It has been optimized for power management applications with a wide range of gate drive voltage (2.5V-10V)

Features

- $R_{DS(on)}$=40mΩ@V_{GS}=2.5V, I_D=5.2A; $R_{DS(on)}$=30mΩ@V_{GS}=4.5V, I_D=6A
- High Density Cell Design for Ultra Low On-Resistance
- High Power and Current Handing Capability
- Fully Characterized Avalanche Voltage and Current
- Ideal for Li ion Battery Pack Applications
- We declare that the material of product compliance with RoHS requirements.

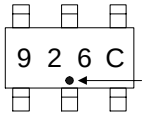


Pin 1: Source 1
Pin 2: Drania 1 & 2
Pin 3: Source 2
Pin 4: Gate 2
Pin 5: Drania 1 & 2
Pin 6: Gate 1

Applications

- Battery Protection
- Load Switch
- Power Management

Marking:



Pb Free Mark
Pb-Free: "●"(Note)
Normal: None

Pin Style: 1.Source1 2.Drain1&2 3.Source2
4.Gate2 5.Drain1&2 6.Gate1

Material:
- Lead solder plating: Sn60/Pb40 (Normal), Sn/3.0Ag/0.5Cu or Pure-Tin (Pb-free)
- Mold Compound: Epoxy resin family,

Absolute Maximum Ratings (T_A=25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	±12	V
I_D	Drain Current (Continuous)	6	A
I_{DM}	Drain Current (Pulsed) *1	30	A
P_D	Total Power Dissipation @T_A=25°C	2	W
	Total Power Dissipation @T_A=75°C	1.3	W
T_j, T_{stg}	Operating and Storage Temperature Range	-55 to +150	°C
$R_{\theta JA}$	Thermal Resistance Junction to Ambient*2	62.5	°C/W

*1: Maximum DC current limited by the package
*2: 1-in^2 2oz Cu PCB board

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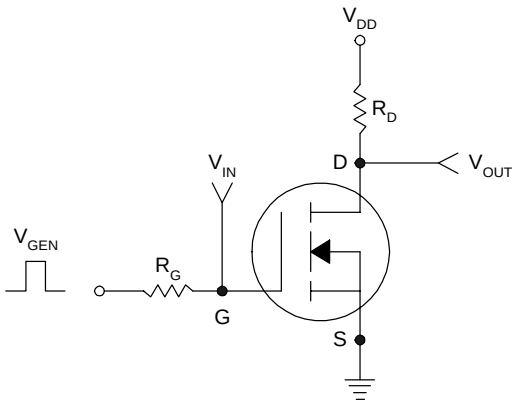
Electrical Characteristics (T_A=25°C, unless otherwise noted)

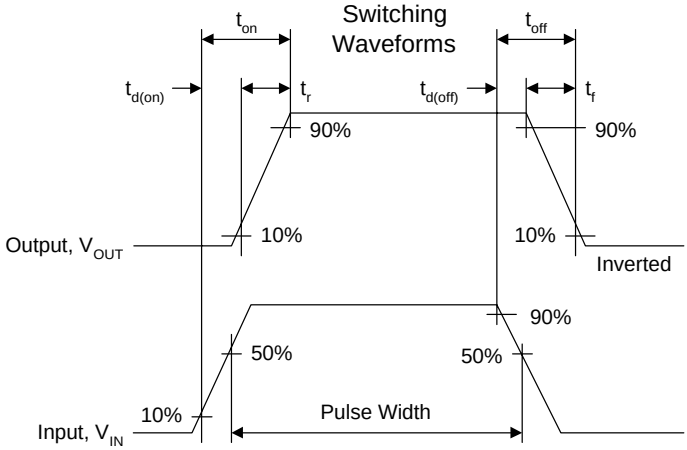
Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
• Static						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	20	-	-	V
$R_{DS(on)}$	Drain-Source On-State Resistance	V_{GS}=2.5V, I_D=5.2A	-	34	40	mΩ
		V_{GS}=4.5V, I_D=6A	-	25	30	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	0.6	-	1.5	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V	-	-	1	uA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±12V, V_{DS}=0V	-	-	±100	nA
g_{FS}	Forward Transconductance	V_{DS}=10V, I_D=6A	7	13	-	S
• Dynamic						
Q_g	Total Gate Charge	V_{DS}=10V, I_D=6A, V_{GS}=4.5V	-	4.86	-	nC
Q_{gs}	Gate-Source Charge		-	0.92	-	
Q_{gd}	Gate-Drain Charge		-	1.4	-	
C_{iss}	Input Capacitance	V_{DS}=8V, V_{GS}=0V, f=1MHz	-	562	-	pF
C_{oss}	Output Capacitance		-	106	-	
C_{rss}	Reverse Transfer Capacitance		-	75	-	
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=10V, I_D=1A, V_{GS}=4.5V R_{GEN}=6Ω	-	8.1	-	ns
t_r	Turn-on Rise Time		-	9.95	-	
$t_{d(off)}$	Turn-off Delay Time		-	21.85	-	
t_f	Turn-off Fall Time		-	5.35	-	
• Drain-Source Diode Characteristics						
I_S	Maximum Diode Forward Current		-	-	1.7	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS}=0V, I_S=1.7A	-	-	1.2	V

Note: Pulse Test: Pulse Width ≤300us, Duty Cycle≤2%

Switching Test Circuit



Switching Waveforms



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TYPICAL ELECTRICAL CHARACTERISTICS

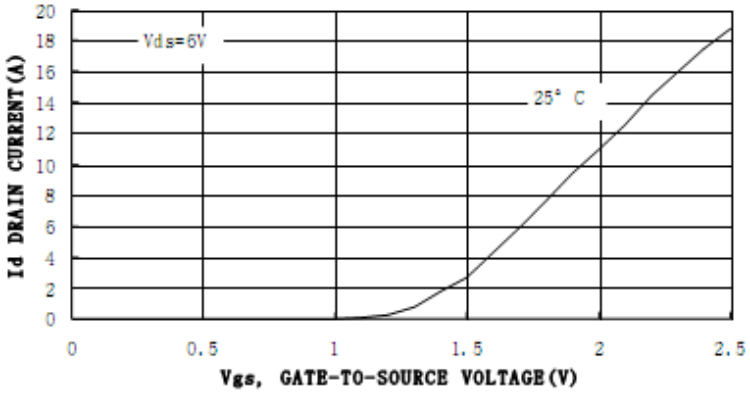

Figure 1. Transfer Characteristics

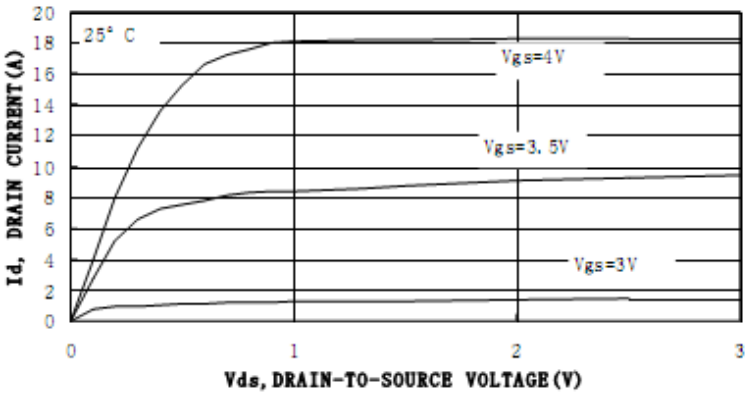

Figure 2. On–Region Characteristics

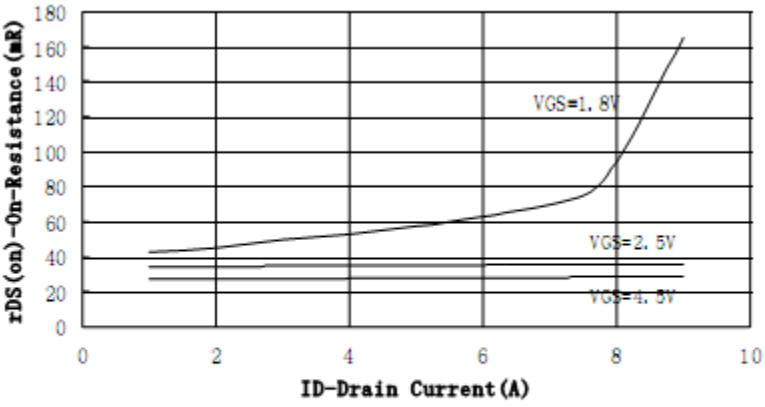

Figure 3. On–Resistance versus Drain Current

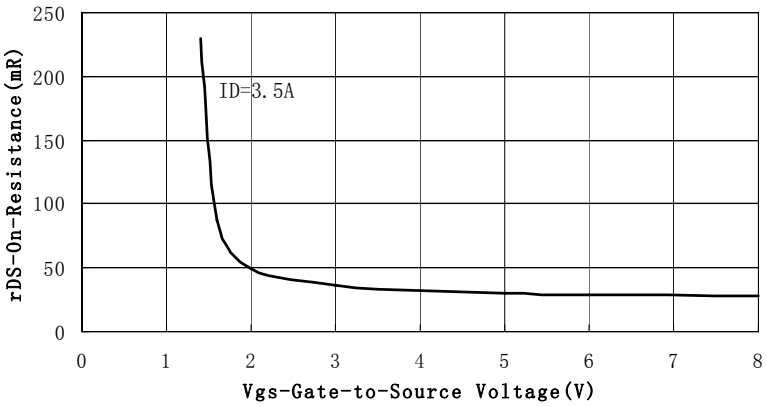

Figure 4. On-Resistance vs. Gate-to-Source Voltage

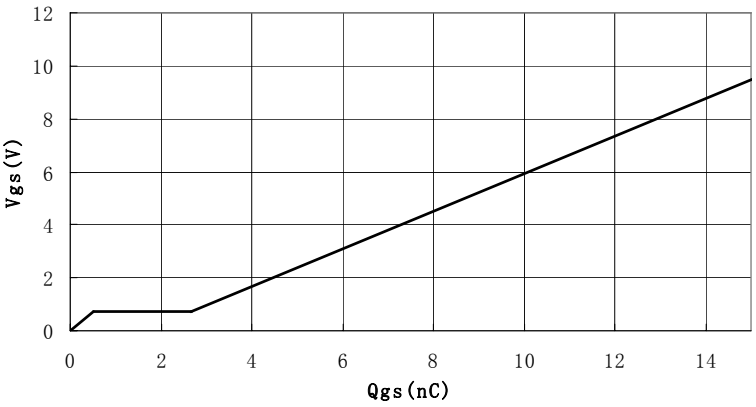

Figure 5. Gate Charge

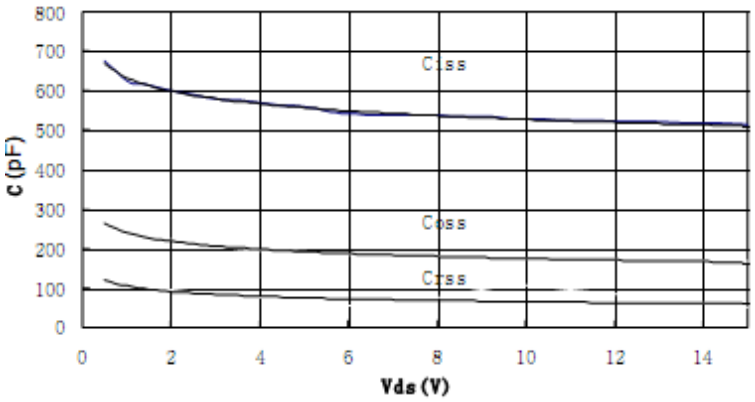

Figure 6. Capacitance

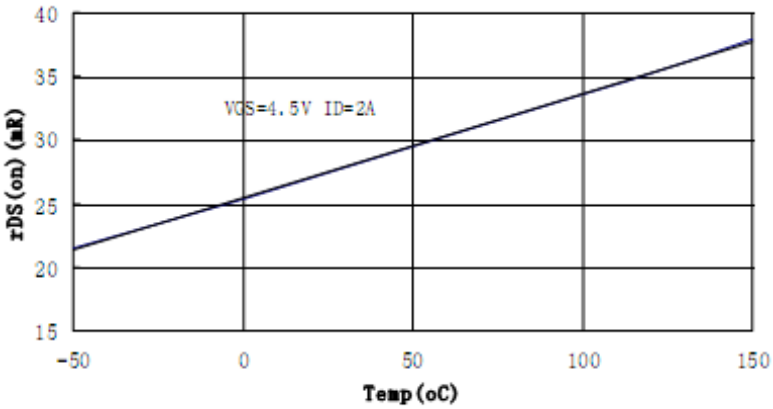

Figure 7. On-Resistance Vs.Junction Temperature

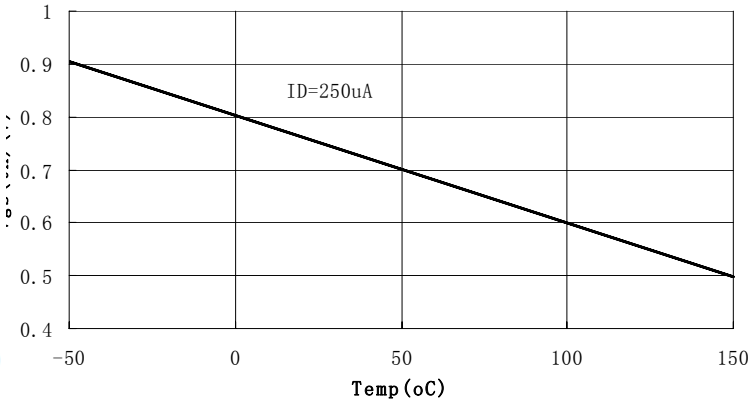

Figure 8. Vth Vs.Junction Temperature

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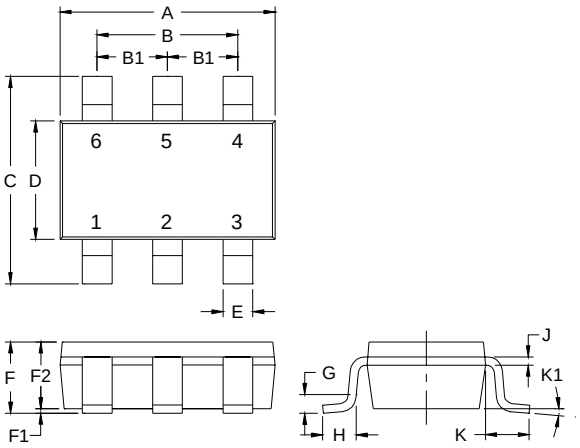

DIM	Min.	Max.
A	2.70	5.10
B	*1.90	-
B1	*0.95	-
C	2.60	3.00
D	1.40	1.80
E	0.30	0.50
F	-	1.10
F1	0	0.10
F2	0.70	1.00
G	*0.25	-
H	*0.45	-
J	*0.12	-
K	*0.60	-
K1	0^{o}	10^{o}

*: REF., Unit: mm