SPECIFICATION
FOR
APPROVAL

( ) **Preliminary Specification**
(◆) **Final Specification**

Title	17.1” WXGA+ TFT LCD

Customer	SONY
MODEL	

SUPPLIER	LG.Philips LCD Co., Ltd.
*MODEL	LP171WP4
Suffix	TLN1

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE
K. S. Kwon / S.Manager	
REVIEWED BY	
J. H. Park / Manager	
PREPARED BY	
S. W. Park / Engineer Y. J. Park / Engineer	

Products Engineering Dept.
LG. Philips LCD Co., Ltd

Contents

RECORD OF REVISIONS

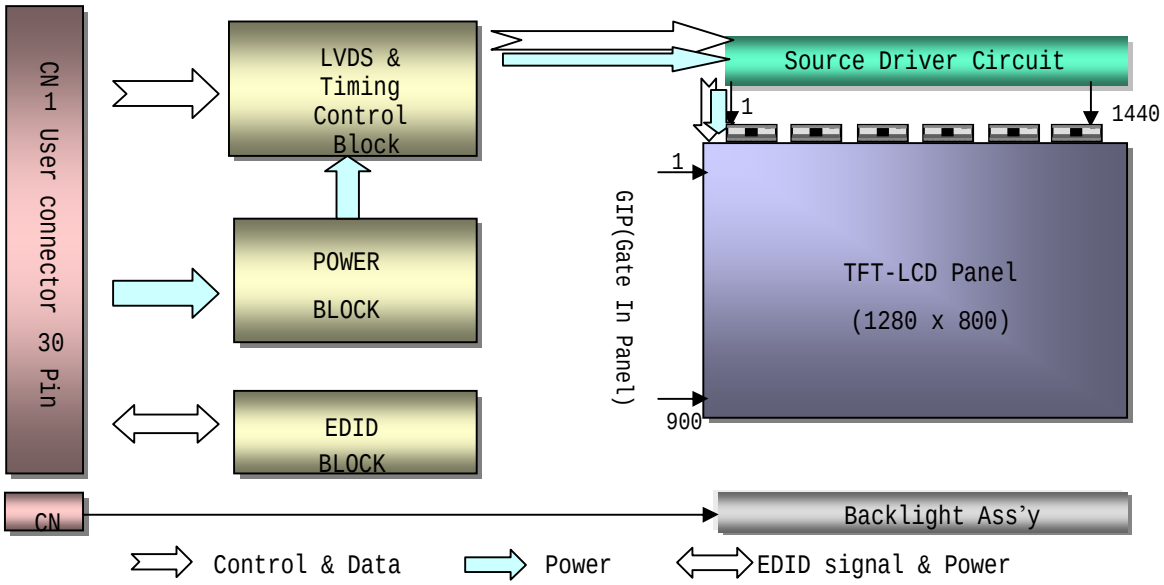
Revision No	Revision Date	Page	Description	EDID ver
0.0	Oct. 02. 2007	-	First Draft (Preliminary Specification)	0.0
0.1	Oct. 17. 2007	11	Add Dclk Spec. (Min. & Max.)	0.0
		13	Change Power Sequence Spec. (T1 (Min.), 0.5ms à 0ms)	
		14	Add Color Coordinate Spec.	
			Change Viewing Angle Min. Spec. (40/40/10/30 à 45/45/15/35)	
0.2	Nov. 16. 2007	6	Add In-Rush Current Spec.	0.0
1.0	Dec. 11. 2007	-	Final Draft	0.0

1. General Description

The LP171WP4 is a Color Active Matrix Liquid Crystal Display with an integral Cold Cathode Fluorescent Lamp (CCFL) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally white mode. This TFT-LCD has 17.1 inches diagonally measured active display area with WXGA+ resolution(900 vertical by 1440 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 6-bit gray scale signal for each dot, thus, presenting a palette of more than 262,144 colors.

The LP171WP4 has been designed to apply the interface method that enables low power, high speed, low EMI.

The LP171WP4 is intended to support applications where thin thickness, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LP171WP4 characteristics provide an excellent flat display for office automation products such as Notebook PC.



General Features

Active Screen Size	17.1 inches diagonal
Outline Dimension	382.2(H, typ) × 244.5(V, typ) × 6.5(D,max) [mm]
Pixel Pitch	0.255mm × 0.255 mm
Pixel Format	1440 horiz. By 900 vert. Pixels RGB strip arrangement
Color Depth	6-bit, 262,144 colors
Luminance, White	200 cd/m^2(Typ.5 point)
Power Consumption	Total 6.5 Watt(Typ.) @ LCM circuit 1.70Watt(Typ.), B/L input 4.80Watt(Typ.)
Weight	705g (Max.)
Display Operating Mode	Transmissive mode, normally white
Surface Treatment	Hard Coating(2H), Glare treatment of the front polarizer
RoHS Comply	Yes

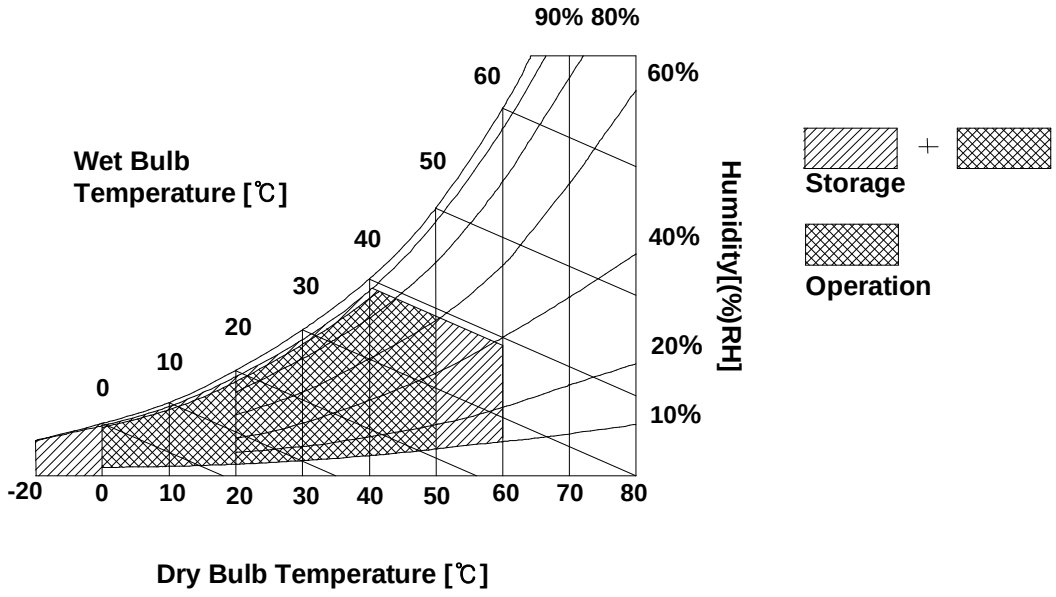
2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Values		Units	Notes
		Min	Max		
Power Input Voltage	VCC	-0.3	4.0	Vdc	at 25 ± 5°C
Operating Temperature	TOP	0	50	°C	1
Storage Temperature	HST	-20	60	°C	1
Operating Ambient Humidity	HOP	10	90	%RH	1
Storage Humidity	HST	10	90	%RH	1

Note : 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39°C Max, and no condensation of water.



3. Electrical Specifications

3-1. Electrical Characteristics

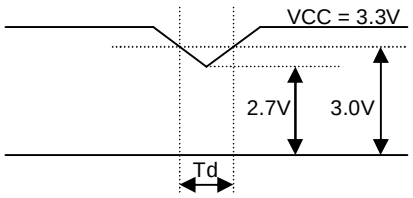
The LP171WP4 requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second input which powers the CCFL, is typically generated by an inverter. The inverter is an external unit to the LCD.

Table 2. ELECTRICAL CHARACTERISTICS

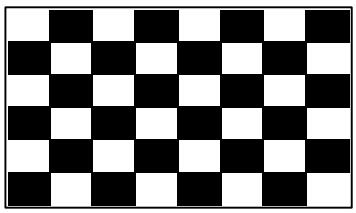
Parameter	Symbol	Values			Unit	Notes
		Min	Typ	Max		
MODULE :						
Power Supply Input Voltage	VCC	3.0	3.3	3.6	V_{DC}	1
Power Supply Input Current	I_{CC}	-	515	590	mA	2
Power Consumption	Pc	-	1.70	1.95	Watt	2
Differential Impedance	Zm	90	100	110	Ohm	3
In-Rush Current	I rush	-	-	1.5	A	
LAMP :						
Operating Voltage	V_{BL}	715(7.0mA)	738(6.5mA)	930(3.0mA)	V_{RMS}	
Operating Current	I_{BL}	3.0	6.5	7.0	mA_{RMS}	4
Power Consumption	P_{BL}	-	4.80	5.01		
Operating Frequency	f_{BL}	40	60	70	kHz	
Discharge Stabilization Time	Ts	-	-	3	Min	5
Life Time		10,000	-	-	Hrs	6
Established Starting Voltage at 25℃ at 0 ℃	Vs			 1300 1500	 V_{RMS} V_{RMS}	

Note)

1. VCC Dip condition
   1-1. When 2.7V ≦ VCC < 3.0V : Td ≦ 10 ms
   1-2. When VCC < 2.7V : VCC Dip must be kept in " 3-7. Power Sequence (page 13) "

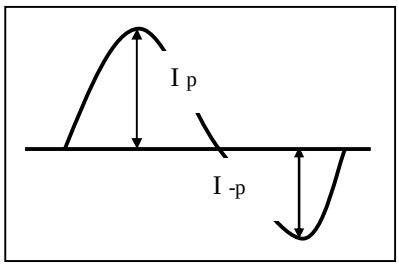


2. The specified current and power consumption are under the Vcc = 3.3V , 25℃, fv = 60Hz condition whereas Mosaic pattern is displayed and fv is the frame frequency.



Note)

3. This impedance value is needed to proper display and measured form LVDS Tx to the mating connector.
4. The typical operating current is for the typical surface luminance (L_{WH}) in optical characteristics.
5. Define the brightness of the lamp after being lighted for 5 minutes as 100%, Ts is the time required for the brightness of the center of the lamp to be not less than 95%.
6. The life time is determined as the time at which brightness of lamp is 50% compare to that of initial value at the typical lamp current.
7. The output of the inverter must have symmetrical(negative and positive) voltage waveform and symmetrical current waveform.(Asymmetrical ratio is less than 10%) Please do not use the inverter which has asymmetrical voltage and asymmetrical current and spike wave.
   Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.
8. It is defined the brightness of the lamp after being lighted for 5 minutes as 100%.
   T_S is the time required for the brightness of the center of the lamp to be not less than 95%.
9. The lamp power consumption shown above does not include loss of external inverter.
   The applied lamp current is a typical one.
10. Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following.
    It shall help increase the lamp lifetime and reduce leakage current.
    a. The asymmetry rate of the inverter waveform should be less than 10%.
    b. The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$.
    * Inverter output waveform had better be more similar to ideal sine wave.



* Asymmetry rate:

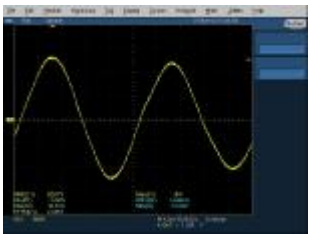
$| I_p - I_{-p} | / I_{rms} * 100\%$

* Distortion rate

I_p (or I_{-p}) / I_{rms}

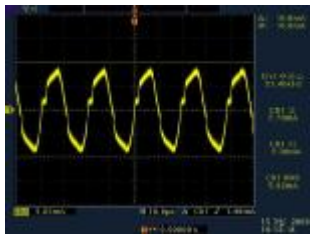
11. Inverter open voltage must be more than lamp voltage for more than 1 second for start-up.
    Otherwise, the lamps may not be turned on.
    ※ Do not attach a conducting tape to lamp connecting wire.
    If the lamp wire attach to a conducting tape, TFT-LCD Module has a low luminance and the inverter has abnormal action. Because leakage current is occurred between lamp wire and conducting tape.

Ex of current wave)



Normal current wave - Standard

Abnormal current wave - Bad



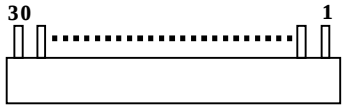
Abnormal current wave - Bad

Abnormal current wave - Bad

3-2. Interface Connections

This LCD employs two interface connections, a 30 pin connector is used for the module electronics interface and the other connector is used for the integral backlight system.
The electronics interface connector is a model GT101-30S-HR11 manufactured by LSC.

Table 3. MODULE CONNECTOR PIN CONFIGURATION (CN1)

Pin	Symbol	Description	Notes
1	GND	Ground	1, Interface chips 1.1 LCD : SW, SW0604 (LCD Controller) including LVDS Receiver 1.2 System : THC63LVDF823A or equivalent * Pin to Pin compatible with LVDS 2. Connector 2.1 LCD :IS100-C30R-C15 ,UJU Elec. GT101-30S-HR11,LS Cable its compatibles 2.2 Mating : FI-X30M or equivalent. 2.3 Connector pin arrangement  [LCD Module Rear View]
2	VCC	Power Supply, 3.3V Typ.	
3	VCC	Power Supply, 3.3V Typ.	
4	V EEDID	DDC 3.3V power	
5	NC	No Connection	
6	Clk EEDID	DDC Clock	
7	DATA EEDID	DDC Data	
8	Odd_R_{IN} 0-	Negative LVDS differential data input	
9	Odd_R_{IN} 0+	Positive LVDS differential data input	
10	GND	Ground	
11	Odd_R_{IN} 1-	Negative LVDS differential data input	
12	Odd_R_{IN} 1+	Positive LVDS differential data input	
13	GND	Ground	
14	Odd_R_{IN} 2-	Negative LVDS differential data input	
15	Odd_R_{IN} 2+	Positive LVDS differential data input	
16	GND	Ground	
17	Odd_CLKIN-	Negative LVDS differential clock input	
18	Odd_CLKIN+	Positive LVDS differential clock input	
19	GND	Ground	
20	Even_R_{IN} 0-	Negative LVDS differential data input	
21	Even_R_{IN} 0+	Positive LVDS differential data input	
22	GND	Ground	
23	Even_R_{IN} 1-	Negative LVDS differential data input	
24	Even_R_{IN} 1+	Positive LVDS differential data input	
25	GND	Ground	
26	Even_R_{IN} 2-	Negative LVDS differential data input	
27	Even_R_{IN} 2+	Positive LVDS differential data input	
28	GND	Ground	
29	Even_CLKIN-	Negative LVDS differential clock input	
30	Even_CLKIN+	Positive LVDS differential clock input	

The backlight interface connector is a model BHSR-02VS-1, manufactured by JST or Compatible.
The mating connector part number is AMP1674817-2 or equivalent.

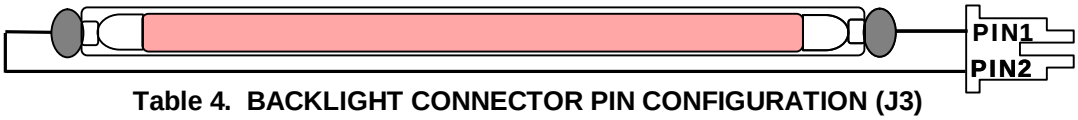


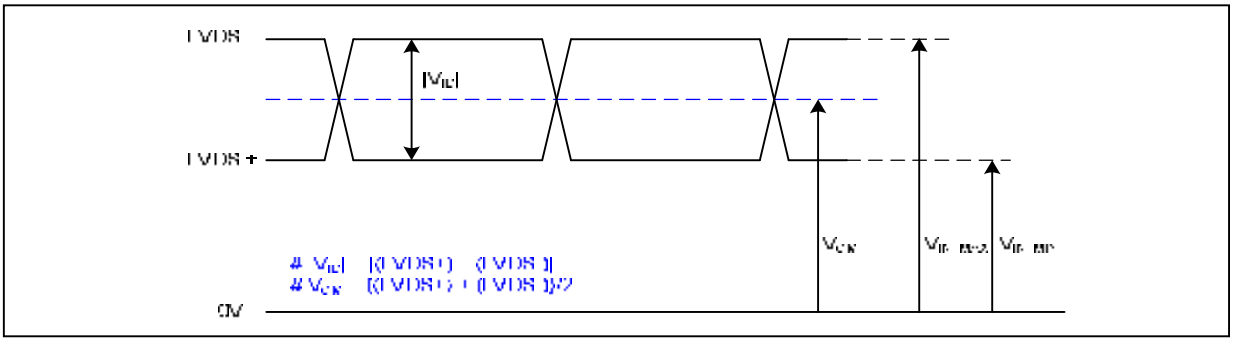
Table 4. BACKLIGHT CONNECTOR PIN CONFIGURATION (J3)

Pin	Symbol	Description	Notes
1	HV	Power supply for lamp (High voltage side)	1
2	LV	Power supply for lamp (Low voltage side)	1

Notes : 1. The high voltage side terminal is colored Sky Blue and the low voltage side terminal is Green.

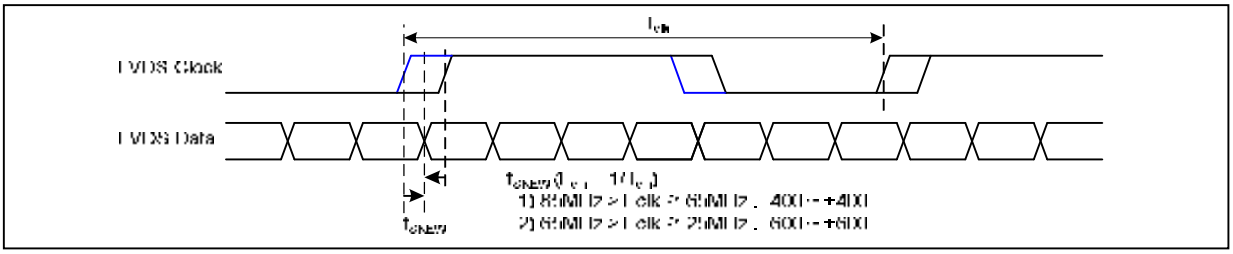
3-3. LVDS Signal Timing Specifications

3-3-1. DC Specification

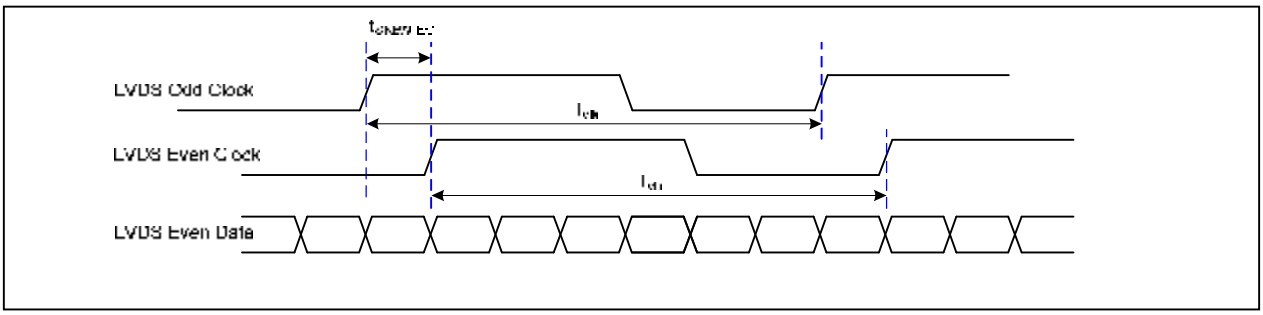


Description	Symbol	Min	Max	Unit	Notes
LVDS Differential Voltage	$\|V_{ID}\|$	100	600	mV	-
LVDS Common mode Voltage	V_{CM}	0.6	1.8	V	-
LVDS Input Voltage Range	V_{IN}	0.3	2.1	V	-

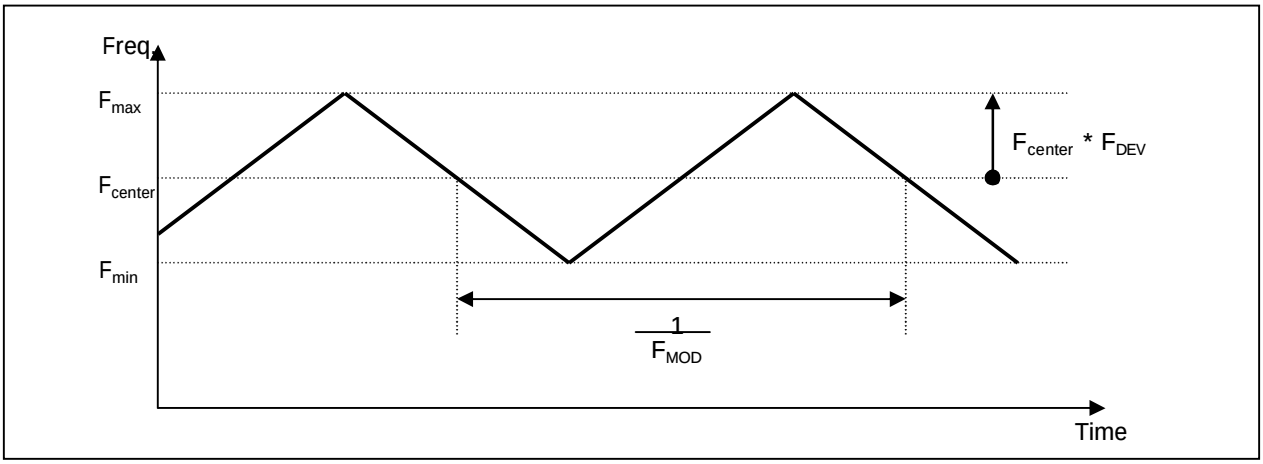
3-3-2. AC Specification



Description	Symbol	Min	Max	Unit	Notes
LVDS Clock to Data Skew Margin	t_{SKEW}	- 400	+ 400	ps	85MHz > Fclk ≥ 65MHz
	t_{SKEW}	- 600	+ 600	ps	65MHz > Fclk ≥ 25MHz
LVDS Clock to Clock Skew Margin (Even to Odd)	t_{SKEW_EO}	- 1/7	+ 1/7	T_{clk}	-
Maximum deviation of input clock frequency during SSC	F_{DEV}	-	± 3	%	-
Maximum modulation frequency of input clock during SSC	F_{MOD}	-	200	KHz	-



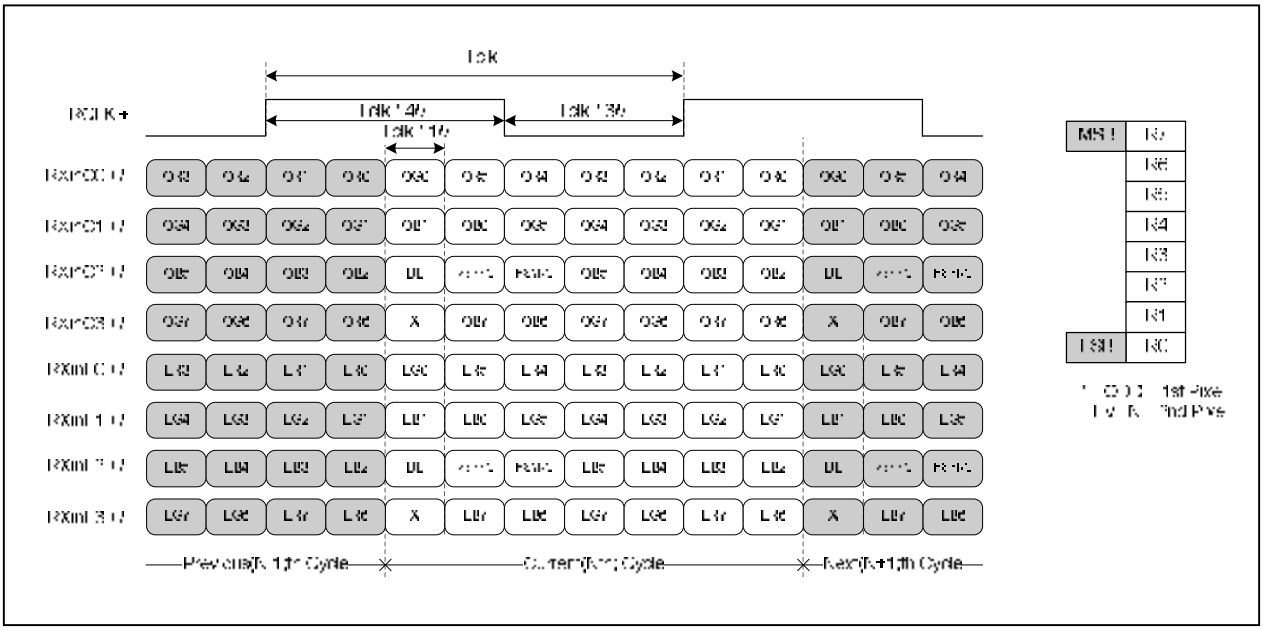
< Clock skew margin between channel >



< Spread Spectrum >

3-3-3. Data Format

1) LVDS 2 Port



< LVDS Data Format >

3-4. Signal Timing Specifications

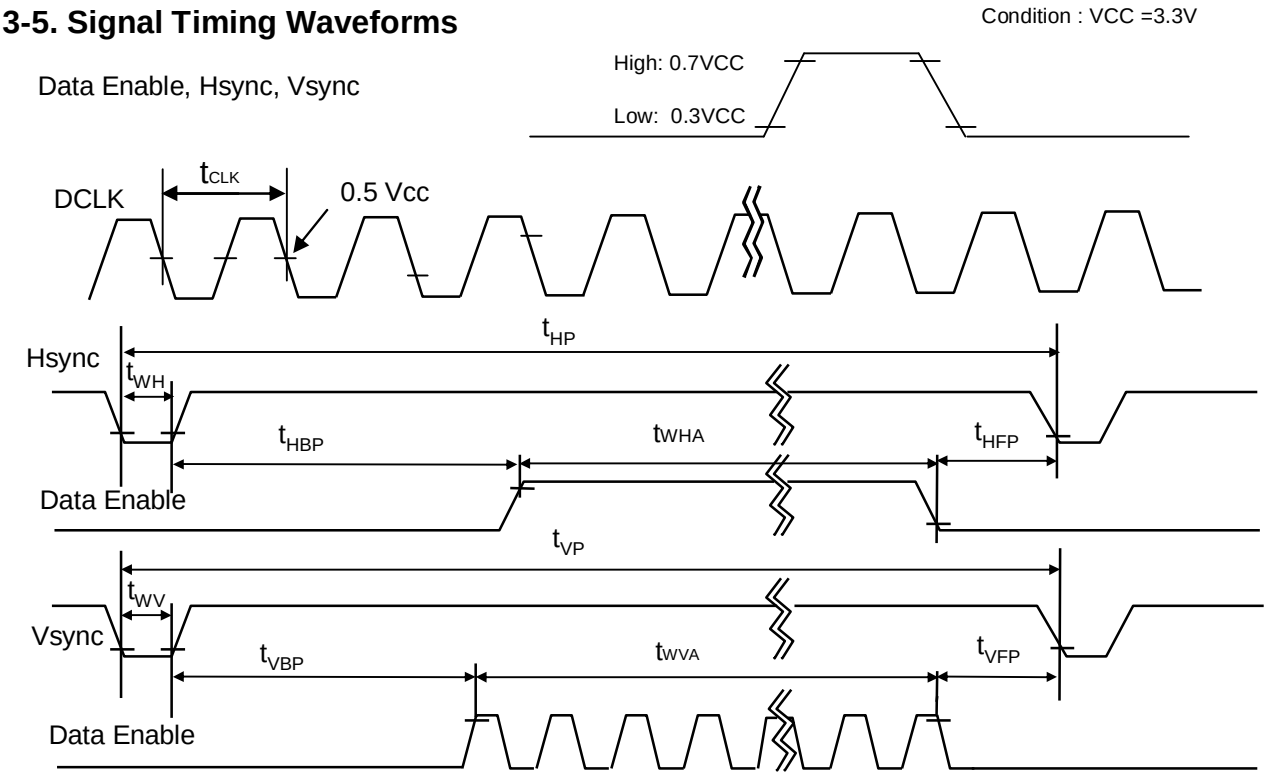
This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications and specifications of LVDS Tx/Rx for its proper operation.

Table 6. TIMING TABLE

ITEM	Symbol		Min	Typ	Max	Unit	Note
DCLK	Frequency	f_{CLK}	43.0	48.1	52.0	MHz	1port : fCLK * 2
Hsync	Period	Thp	832	880	920	tCLK	1port : fCLK * 2
	Width	t_{WH}	8	16	24		
	Width-Active	t_{WHA}	720	720	720		
Vsync	Period	t_{VP}	908	912	924	tHP	
	Width	t_{WV}	2	3	5		
	Width-Active	t_{WVA}	900	900	900		
Data Enable	Horizontal back porch	t_{HBP}	88	112	128	tCLK	1port : fCLK * 2
	Horizontal front porch	t_{HFP}	16	32	48		1port : fCLK * 2
	Vertical back porch	t_{VBP}	4	6	13	tHP	
	Vertical front porch	t_{VFP}	2	3	6		

3-5. Signal Timing Waveforms

Condition : VCC =3.3V



3-6. Color Input Data Reference

The brightness of each primary color (red,green and blue) is based on the 6-bit gray scale data input for the color ; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 7. COLOR DATA REFERENCE

Color		Input Color Data																	
		RED						GREEN						BLUE					
		MSB					LSB	MSB					LSB	MSB					LSB
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	…			…						…						…			
	RED (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	...			…						…						…			
	GREEN (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	GREEN (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
BLUE	BLUE (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	…			…						…						…			
	BLUE (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	BLUE (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

3-7. Power Sequence

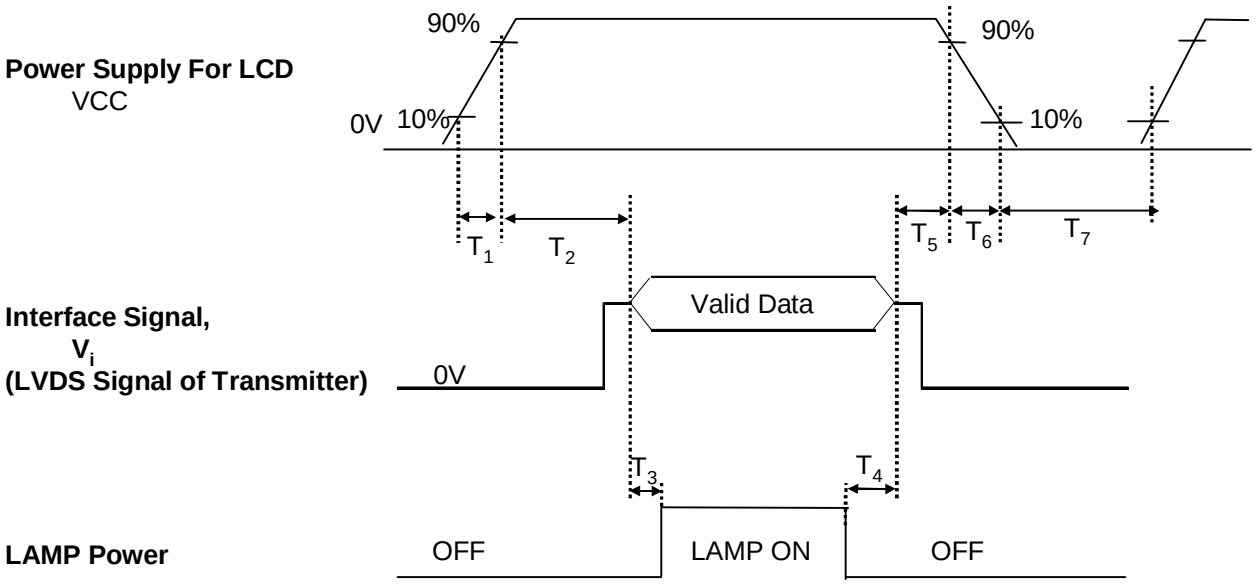


Table 8. POWER SEQUENCE TABLE

Parameter	Value			Units
	Min.	Typ.	Max.	
T_1	0	-	10	(ms)
T_2	0	-	50	(ms)
T_3	200	-	-	(ms)
T_4	200	-	-	(ms)
T_5	0	-	50	(ms)
T_6	3	-	10	(ms)
T_7	400	-	-	(ms)

Note)
1. Valid Data is Data to meet “3-3. LVDS Signal Timing Specifications”
2. Please avoid floating state of interface signal at invalid period.
3. When the interface signal is invalid, be sure to pull down the power supply for LCD VCC to 0V.
4. Lamp power must be turn on after power supply for LCD and interface signal are valid.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and Θ equal to 0°.
FIG. 1 presents additional information concerning the measurement equipment and method.

FIG. 1 Optical Characteristic Measurement Equipment and Method

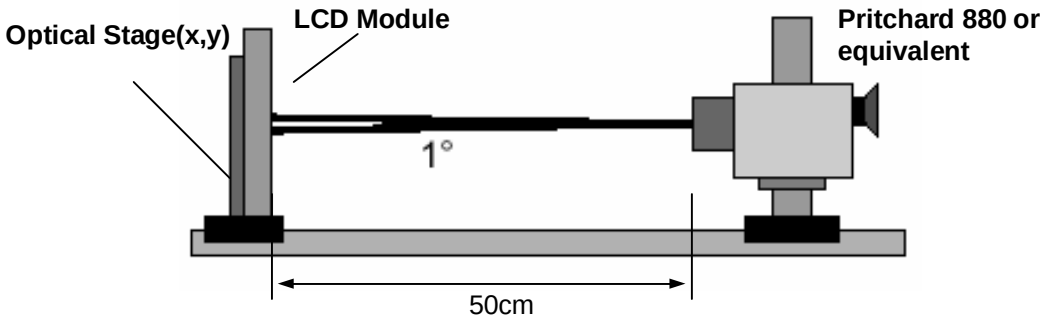


Table 9. OPTICAL CHARACTERISTICS

Ta=25°C, VCC=3.3V, fv=60Hz, f_{CLK}= 48.1MHz, F_{BL} = 60KHz , I_{BL}= 6.5mA

Parameter	Symbol	Values			Units	Notes
		Min	Typ	Max		
Contrast Ratio	CR	350	500	-		1
Surface Luminance, white	L_{WH}	170	200	-	cd/m^2	2
Luminance Variation	δ_{WHITE}	-	1.5	1.7		3
Response Time	Tr_R+ Tr_D		16		ms	4
Color Coordinates						
RED	RX	0.572	0.602	0.632		
	RY	0.319	0.349	0.379		
GREEN	GX	0.293	0.323	0.353		
	GY	0.521	0.551	0.581		
BLUE	BX	0.128	0.158	0.188		
	BY	0.111	0.141	0.171		
WHITE	WX	0.283	0.313	0.343		
	WY	0.299	0.329	0.359		
Viewing Angle						5
x axis, right(Φ=0°)	Θr	45	-	-	degree	
x axis, left (Φ=180°)	Θl	45	-	-	degree	
y axis, up (Φ=90°)	Θu	15	-	-	degree	
y axis, down (Φ=270°)	Θd	35	-	-	degree	
Gray Scale						6

Note)

1. Contrast Ratio(CR) is defined mathematically as

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

2. Surface luminance is the average of 5 point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see FIG 1.

$$L_{WH} = \text{Average}(L_1, L_2, \ldots L_5)$$

3. The variation in surface luminance , The panel total variation (δ_{WHITE}) is determined by measuring L_N at each test position 1 through 13 and then defined as followed numerical formula.
For more information see FIG 2.

$$\delta_{WHITE} = \frac{\text{Maximum}(L_1, L_2, \ldots L_{13})}{\text{Minimum}(L_1, L_2, \ldots L_{13})}$$

4. Response time is the time required for the display to transition from white to black (rise time, Tr_R) and from black to white(Decay Time, Tr_D). For additional information see FIG 3.

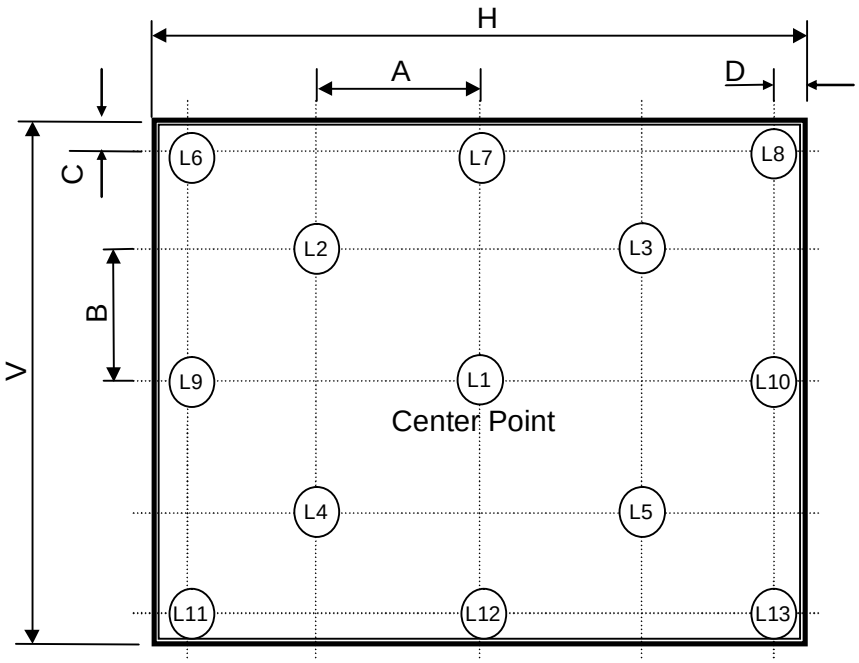
5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 4.

6. Gray scale specification * f_V = 60Hz

Gray Level	Luminance [%] (Typ)
L0	0
L7	1.00
L15	4.60
L23	11.4
L31	21.6
L39	35.4
L47	53.0
L55	77.0
L63	100

FIG. 2 Luminance

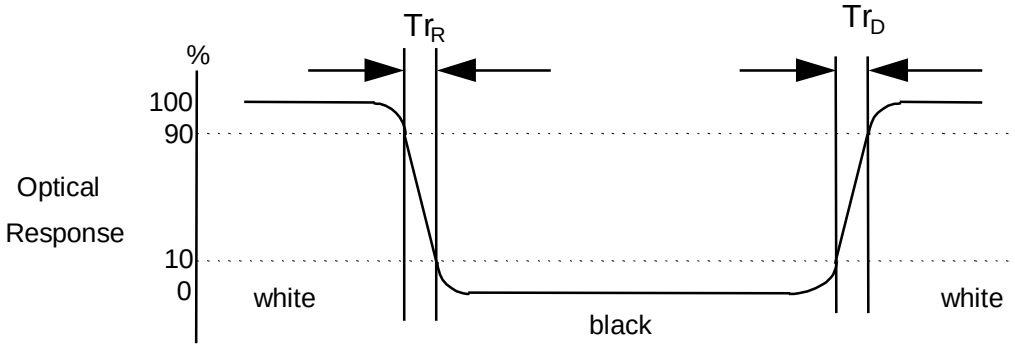
<measuring point for surface luminance & measuring point for luminance variation>



H,V : ACTIVE AREA
A : H/4 mm
B : V/4 mm
C : 10 mm
D : 10 mm
POINTS : 13 POINTS

FIG. 3 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.



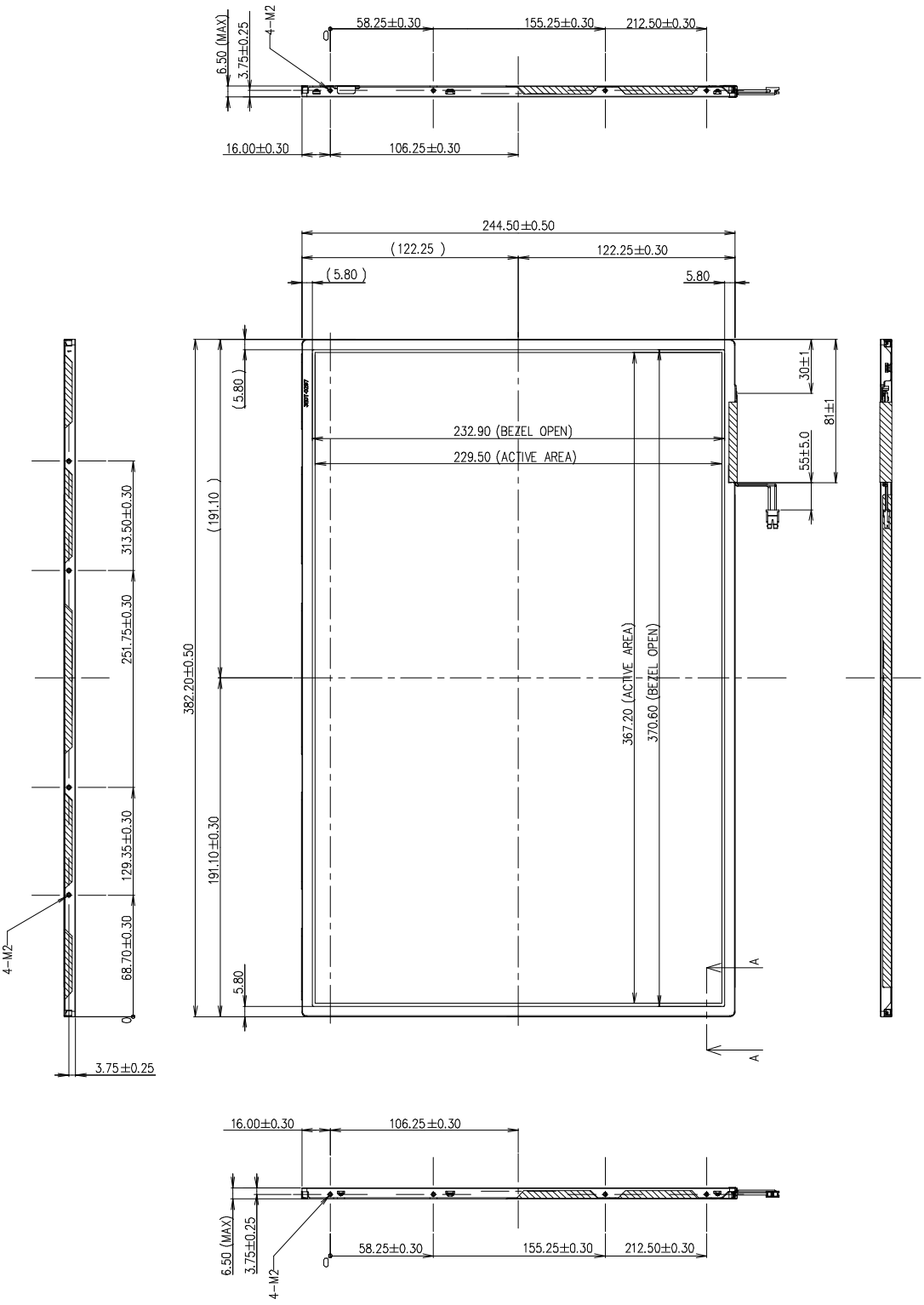
5. Mechanical Characteristics

The contents provide general mechanical characteristics for the model LP171WP4. In addition the figures in the next page are detailed mechanical drawing of the LCD.

Outline Dimension	Horizontal	382.2 ± 0.5mm
	Vertical	244.5 ± 0.5mm
	Thickness	6.5mm (max)
Bezel Area	Horizontal	370.6 ± 0.5mm
	Vertical	232.9 ± 0.5mm
Active Display Area	Horizontal	367.2 mm
	Vertical	229.5 mm
Weight	705g (Max.)	
Surface Treatment	Hard Coating(2H), Glare treatment of the front polarizer	

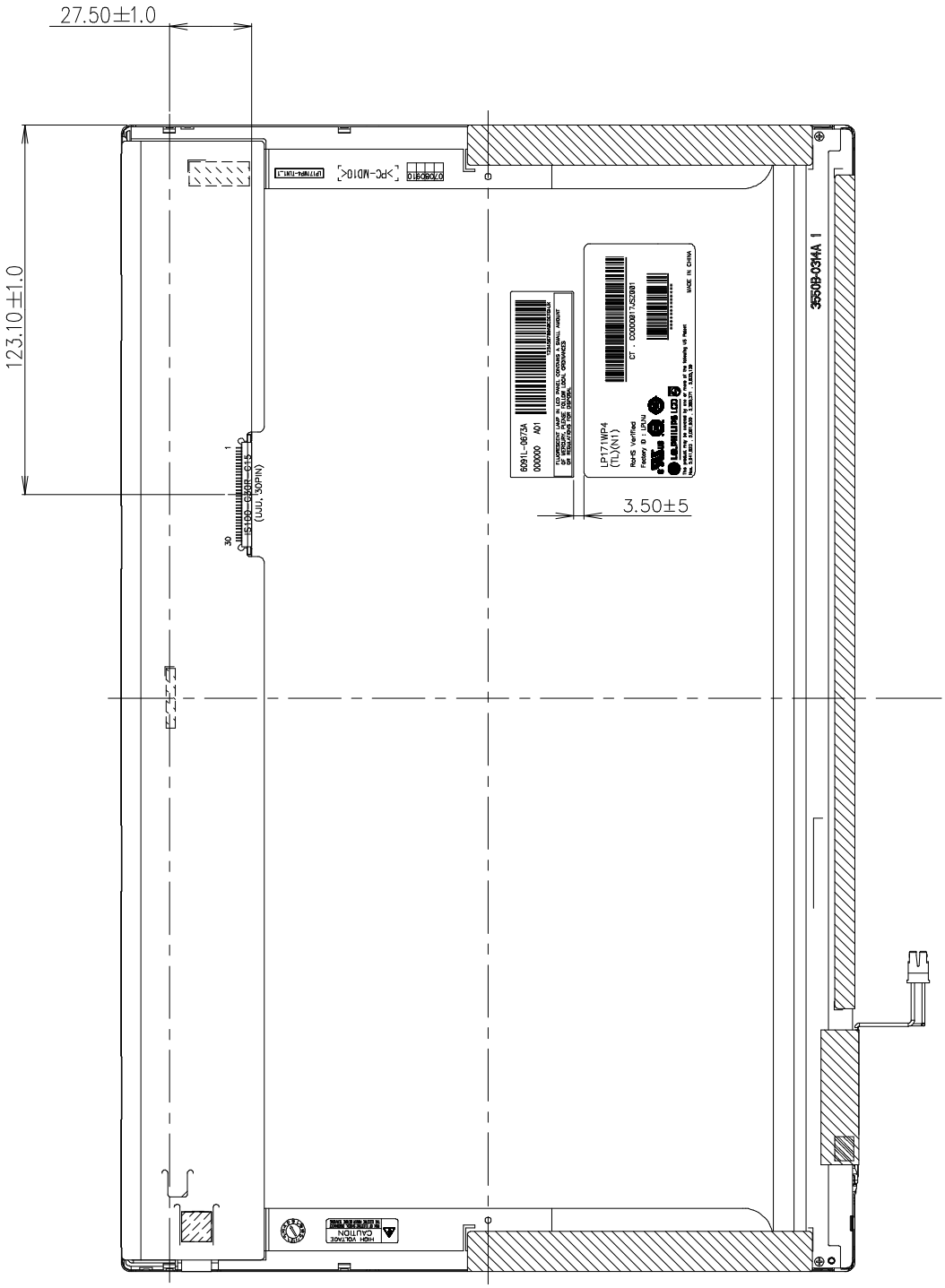
<FRONT VIEW>

Note) Unit:[mm], General tolerance: ± 0.5mm

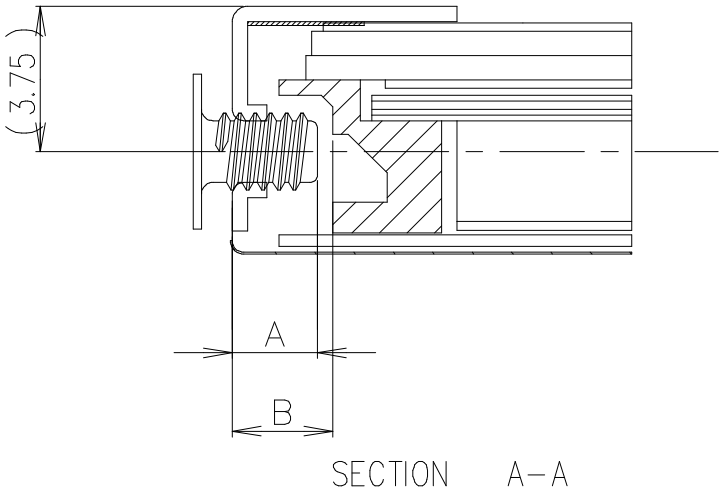


<REAR VIEW>

Note) Unit:[mm], General tolerance: ± 0.5mm



[DETAIL DESCRIPTION OF SIDE MOUNTING SCREW]

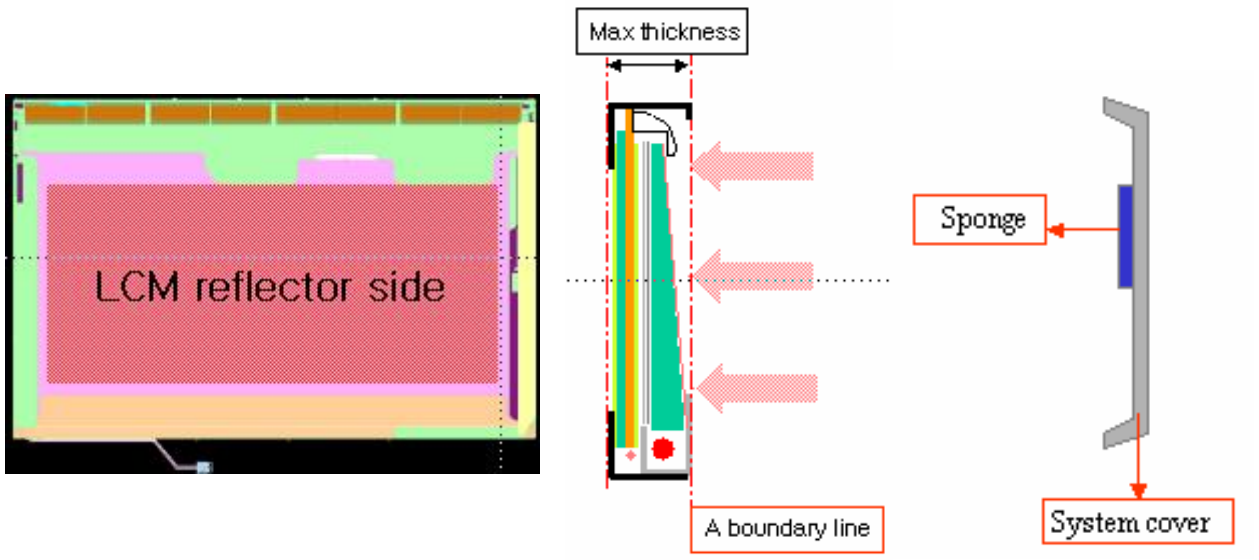


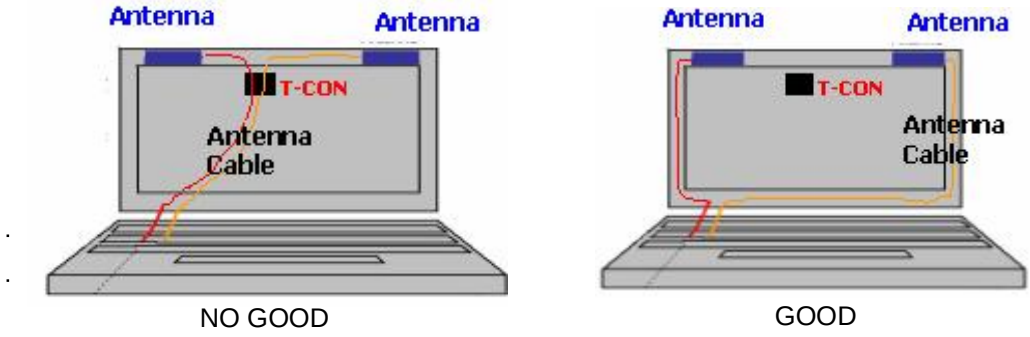
* Mounting Screw Length (A)
  = 2.0(Min) / 2.5(Max)
* Mounting Screw Hole Depth (B)
  = 2.5(Min)
* Mounting hole location : 3.75(typ.)
* Torque : 2.0 kgf.cm(Max)
  (Measurement gauge : torque meter)

Notes : 1. Screw plated through the method of non-electrolytic nickel plating is preferred to reduce possibility that results in vertical and/or horizontal line defect due to the conductive particles from screw surface.

LPL Proposal for system cover design.(Appendix)

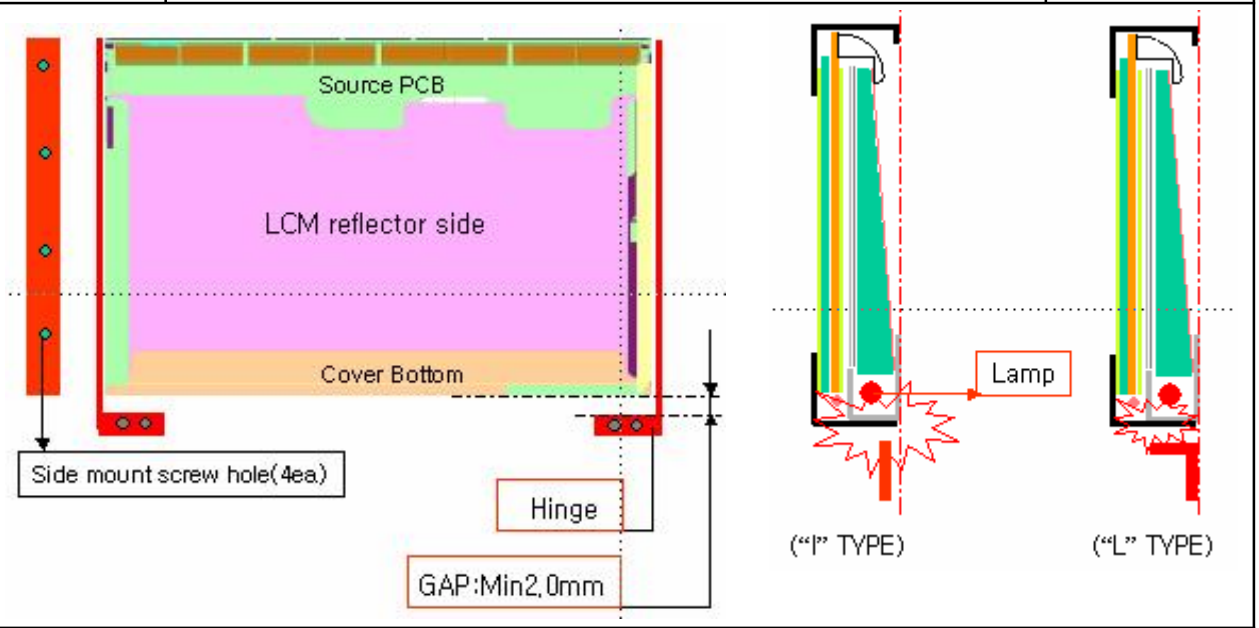
1	Gap check for securing the enough gap between LCM and System cover.	



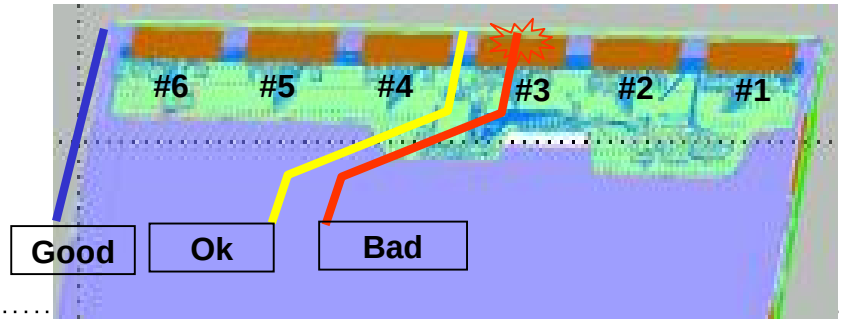
Define	1.Rear side of LCM is sensitive against external stress,and previous check about interference is highly needed. 2.In case there is something from system cover comes into the boundary above,mechanical interference may cause the FOS defects. (Eg:Ripple,White spot..)
2	Check if antenna cable is sufficiently apart from T-CON of LCD Module.
Define	
	1.If system antenna is overlapped with T-CON,it might be cause the noise.

LPL Proposal for system cover design.

3	Gap check for securing the enough gap between LCM and System hinge.	



Define	1.At least 2.0mm of gap needs to be secured to prevent the shock related defects. 2."L" type of hinge is recommended than "I" type under shock test.
4	Checking the path of the System wire.

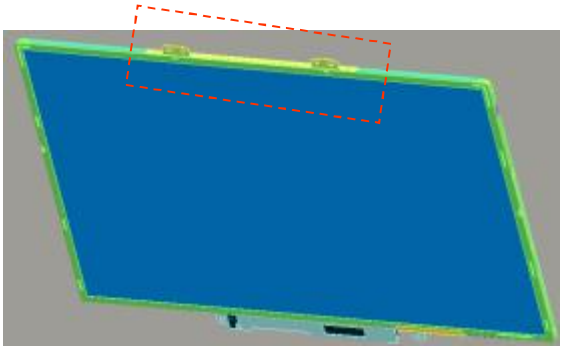


Define	1.COF area needs to be handled with care. 2.GOOD **è** Wire path design to system side. OK **è** Wire path is located between COFs. BAD **è** Wire path overlapped with COF area.

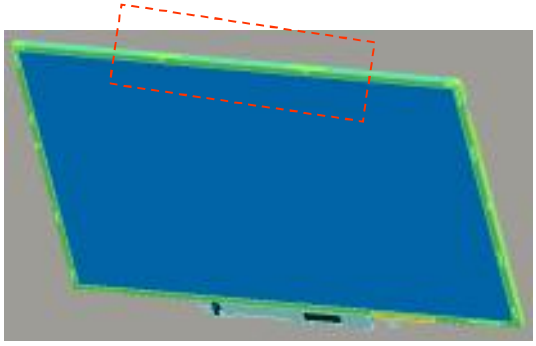
LPL Proposal for system cover design.

5	Using a bracket on the top of LCM is not recommended.	

bracket

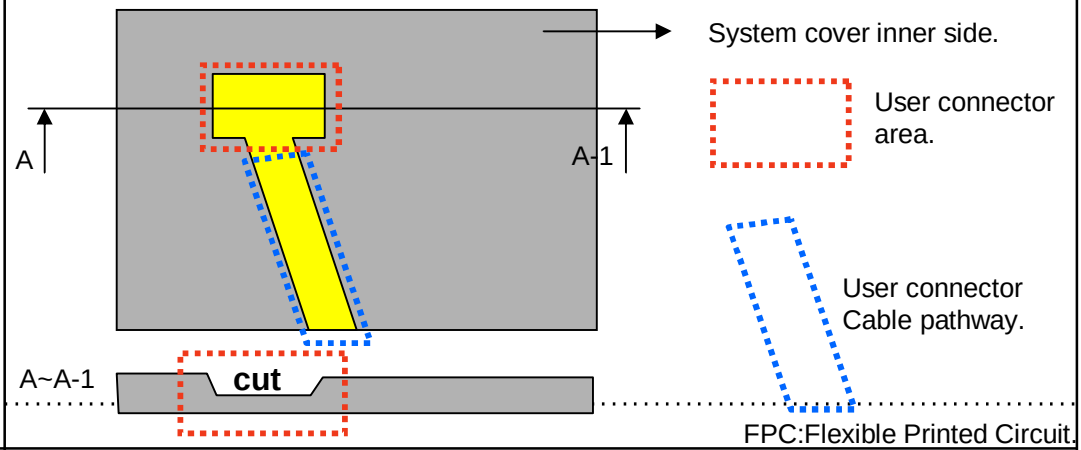


With bracket



Without bracket

Define	1.Condition without bracket is good for mechanical noise,and can minimize the light leakage from deformation of bracket. 2.The results shows that there is no difference between the condition with or without bracket.
6	Securing additional gap on CNT area..



Define	1.CNT area is specially sensitive against external stress,and additional gap by cutting on system cover will be helpful on removing the Ripple. 2.Using a thinner CNT will be better. (eg: FPC type)

6. Reliability

Environment test condition

No.	Test Item	Conditions
1	High temperature storage test	Ta= 60°C, 240h
2	Low temperature storage test	Ta= -20°C, 240h
3	High temperature operation test	Ta= 50°C, 50%RH, 240h
4	Low temperature operation test	Ta= 0°C, 240h
5	Vibration test (non-operating)	Sine wave, 10 ~ 500 ~ 10Hz, 1.5G, 0.37oct/min 3 axis, 1hour/axis
6	Shock test (non-operating)	Half sine wave, 180G, 2ms one shock of each six faces(I.e. run 180G 2ms for all six faces)
7	Altitude operating storage / shipment	0 ~ 10,000 feet (3,048m) 24Hr 0 ~ 40,000 feet (12,192m) 24Hr

{ Result Evaluation Criteria }
There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.

7. International Standards

7-1. Safety

a) UL 60950-1:2003, First Edition, Underwriters Laboratories, Inc.,
Standard for Safety of Information Technology Equipment.
b) CAN/CSA C22.2, No. 60950-1-03 1st Ed. April 1, 2003, Canadian Standards Association,
Standard for Safety of Information Technology Equipment.
c) EN 60950-1:2001, First Edition,
European Committee for Electrotechnical Standardization(CENELEC)
European Standard for Safety of Information Technology Equipment.

7-2. EMC

a) ANSI C63.4 “Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHZ to 40GHz. “American National Standards Institute(ANSI), 1992
b) C.I.S.P.R “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.“ International Special Committee on Radio Interference.
c) EN 55022 “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.“ European Committee for Electrotechnical Standardization.(CENELEC), 1998
(Including A1: 2000)

8. Packing

8-1. Designation of Lot Mark

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
E : MONTH
D : YEAR
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Mark	1	2	3	4	5	6	7	8	9	0

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial No. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one box : 20 pcs

b) Box Size : 482mm × 371mm × 325mm

9. PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD module.

9-1. MOUNTING PRECAUTIONS

(1) You must mount a module using holes arranged in four corners or four sides.
(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.

9-2. OPERATING PRECAUTIONS

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=± 200mV(Over and under shoot voltage)

(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.

9-3. ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

9-5. STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. HANDLING PRECAUTIONS FOR PROTECTION FILM

(1) When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to remain on the polarizer.
Please carefully peel off the protection film without rubbing it against the polarizer.
(3) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
(4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 1/3

Byte# (decimal)	Byte# (HEX)	Field Name and Comments	Value (HEX)		Value (binary)	
0	00	Header	0	0	0000 0000	
1	01		F	F	1111 1111	
2	02		F	F	1111 1111	
3	03		F	F	1111 1111	Header
4	04		F	F	1111 1111	
5	05		F	F	1111 1111	
6	06		F	F	1111 1111	
7	07		0	0	0000 0000	
8	08	EISA manufacturer code (3 Character ID) = LPL	3	2	0011 0010	
9	09	Compressed ASCII	0	C	0000 1100	
10	0A	Panel Supplier Reserved - Product code = A101	0	1	0000 0001	
11	0B	(Hex, LSB first)	A	1	1010 0001	
12	0C	LCD Module Serial No. = 0 (If not used)	0	0	0000 0000	Vender/
13	0D	LCD Module Serial No. = 0 (If not used)	0	0	0000 0000	Product ID
14	0E	LCD Module Serial No. = 0 (If not used)	0	0	0000 0000	
15	0F	LCD Module Serial No. = 0 (If not used)	0	0	0000 0000	
16	10	Week of Manufacture = 00	0	0	0000 0000	
17	11	Year of manufacture = 2007	1	1	0001 0001	
18	12	EDID Structure version # = 1	0	1	0000 0001	EDID Version/
19	13	EDID Revision # = 2	0	2	0000 0010	Revision
20	14	Video input definition = Digital I/p, non TMDS CRGB	8	0	1000 0000	
21	15	Max H image size (cm) = 36.72 cm (37)	2	5	0010 0101	Display
22	16	Max V image size (cm) = 22.95 cm (23)	1	7	0001 0111	Parameter
23	17	Display gamma = 2.20	7	8	0111 1000	
24	18	Feature support (DPMS) = Active off, RGB Color	0	A	0000 1010	
25	19	Red/Green low Bits	1	C	0001 1100	
26	1A	Blue/White Low Bits	8	5	1000 0101	
27	1B	Red X Rx = 0.602	9	A	1001 1010	
28	1C	Red Y Ry = 0.349	5	9	0101 1001	
29	1D	Green X Gx = 0.323	5	2	0101 0010	Color
30	1E	Green Y Gy = 0.551	8	D	1000 1101	Characteristic
31	1F	Blue X Bx = 0.158	2	8	0010 1000	
32	20	Blue Y By = 0.141	2	4	0010 0100	
33	21	White X Wx = 0.313	5	0	0101 0000	
34	22	White Y Wy = 0.329	5	4	0101 0100	
35	23	Established Timing I	0	0	0000 0000	Established
36	24	Established Timing II	0	0	0000 0000	Timings
37	25	Manufacturer's Timings	0	0	0000 0000	
38	26	Standard Timing Identification 1 was not used	0	1	0000 0001	
39	27	Standard Timing Identification 1 was not used	0	1	0000 0001	
40	28	Standard Timing Identification 2 was not used	0	1	0000 0001	
41	29	Standard Timing Identification 2 was not used	0	1	0000 0001	
42	2A	Standard Timing Identification 3 was not used	0	1	0000 0001	
43	2B	Standard Timing Identification 3 was not used	0	1	0000 0001	
44	2C	Standard Timing Identification 4 was not used	0	1	0000 0001	Standard
45	2D	Standard Timing Identification 4 was not used	0	1	0000 0001	Timing ID
46	2E	Standard Timing Identification 5 was not used	0	1	0000 0001	
47	2F	Standard Timing Identification 5 was not used	0	1	0000 0001	
48	30	Standard Timing Identification 6 was not used	0	1	0000 0001	
49	31	Standard Timing Identification 6 was not used	0	1	0000 0001	
50	32	Standard Timing Identification 7 was not used	0	1	0000 0001	
51	33	Standard Timing Identification 7 was not used	0	1	0000 0001	
52	34	Standard Timing Identification 8 was not used	0	1	0000 0001	
53	35	Standard Timing Identification 8 was not used	0	1	0000 0001	

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 2/3

Byte# (decimal)	Byte# (HEX)	Field Name and Comments	Value (HEX)		Value (binary)	
54	36	1440 X 900 @ 60Hz mode : pixelclock = 96.21MHz	9	5	1001 0101	
55	37	(Stored LSB first)	2	5	0010 0101	
56	38	HorizontalActive = 1440 pixels	A	0	1010 0000	
57	39	HorizontalBlanking = 320 pixels	4	0	0100 0000	
58	3A	HorizontalActive : HorizontalBlanking = 1440 : 320	5	1	0101 0001	
59	3B	VerticalAvtive = 900 lines	8	4	1000 0100	
60	3C	VerticalBlanking = 12 lines	0	C	0000 1100	Detailed
61	3D	VerticalActive : VerticalBlanking = 900 : 12	3	0	0011 0000	Timing
62	3E	HorizontalSync. Offset = 64 pixels	4	0	0100 0000	Description
63	3F	HorizontalSync Pulse Width = 32 pixels	2	0	0010 0000	#1
64	40	VerticalSync Offset = 1 lines, Sync Width = 3 lines	1	3	0001 0011	
65	41	HorizontalVertical Sync Offset/Width upper 2bits = 0	0	0	0000 0000	
66	42	HorizontalImage Size = 367.2mm(367)	6	F	0110 1111	
67	43	VerticalImage Size = 229.5mm(230)	E	6	1110 0110	
68	44	Horizontal& VerticalImage Size	1	0	0001 0000	
69	45	HorizontalBorder = 0	0	0	0000 0000	
70	46	VerticalBorder = 0	0	0	0000 0000	
71	47	Non-interlaced,Normaldisplay,no stereo,Digitalseparate sync,H/V polnegatives	1	9	0001 1001	
72	48	Detailed Timing Descriptor#2	0	0	0000 0000	
73	49		0	0	0000 0000	
74	4A		0	0	0000 0000	
75	4B		0	0	0000 0000	
76	4C		0	0	0000 0000	
77	4D		0	0	0000 0000	
78	4E		0	0	0000 0000	Detailed
79	4F		0	0	0000 0000	Timing
80	50		0	0	0000 0000	Description
81	51		0	0	0000 0000	#2
82	52		0	0	0000 0000	
83	53		0	0	0000 0000	
84	55		0	0	0000 0000	
85	55		0	0	0000 0000	
86	56		0	0	0000 0000	
87	57		0	0	0000 0000	
88	58		0	0	0000 0000	
89	59		0	0	0000 0000	
90	5A	Detailed Timing Descriptor#3	0	0	0000 0000	
91	5B		0	0	0000 0000	
92	5C		0	0	0000 0000	
93	5D		F	E	1111 1110	
94	5E		0	0	0000 0000	
95	5F	L	4	C	0100 1100	
96	60	G	4	7	0100 0111	Detailed
97	61	P	5	0	0101 0000	Timing
98	62	h	6	8	0110 1000	Description
99	63	i	6	9	0110 1001	#3
100	64	l	6	C	0110 1100	
101	65	i	6	9	0110 1001	
102	66	p	7	0	0111 0000	
103	67	s	7	3	0111 0011	
104	68	L	4	C	0100 1100	
105	69	C	4	3	0100 0011	
106	6A	D	4	4	0100 0100	
107	6B	LF	0	A	0000 1010	

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 3/3

Byte# (decimal)	Byte# (HEX)	Field Name and Comments	Value (HEX)		Value (binary)	
108	6C	Detailed Timing Descriptor #4	0	0	0000 0000	
109	6D		0	0	0000 0000	
110	6E		0	0	0000 0000	
111	6F		F	E	1111 1110	
112	70		0	0	0000 0000	
113	71	L	4	C	0100 1100	
114	72	P	5	0	0101 0000	Detailed Timing Description #4
115	73	1	3	1	0011 0001	
116	74	7	3	7	0011 0111	
117	75	1	3	1	0011 0001	
118	76	W	5	7	0101 0111	
119	77	P	5	0	0101 0000	
120	78	4	3	4	0011 0100	
121	79	-	2	D	0010 1101	
122	7A	T	5	4	0101 0100	
123	7B	L	4	C	0100 1100	
124	7C	N	4	E	0100 1110	
125	7D	1	3	1	0011 0001	
126	7E	Extension flag = 00	0	0	0000 0000	Extension Flag
127	7F	Checksum	2	4	0010 0100	Checksum