

LP171WU7
Liquid Crystal Display

Product Specification

SPECIFICATION
FOR
APPROVAL

() Preliminary Specification

(●) Final Specification

Title	17.1" WUXGA TFT LCD
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BUYER	Dell
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LP171WU7
Suffix	TLD1

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE
_____ /	_____
_____ /	_____
_____ /	_____

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE
K. J. KWON / S.Manager	_____
REVIEWED BY	
M. J. Lee / Manager	_____
PREPARED BY	
S. U. Kim / Engineer	_____

Product Engineering Dept.
LG Display Co., Ltd

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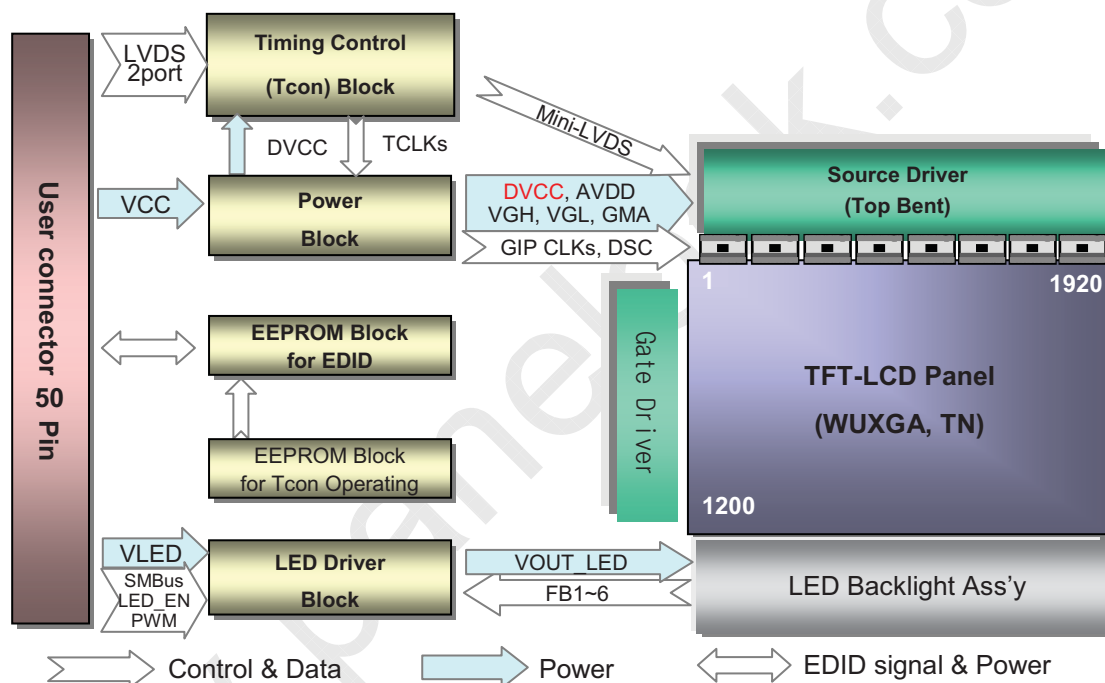
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1. General Description

The LP171WU7 is a Color Active Matrix Liquid Crystal Display with an integral LED backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally white mode. This TFT-LCD has 17.1 inches diagonally measured active display area with WUXGA resolution (1920 horizontal by 1200 vertical pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 6-bit gray scale signal for each dot, thus, presenting a palette of more than 262,144 colors. The LP171WU7 has been designed to apply the interface method that enables low power, high speed, low EMI. The LP171WU7 is intended to support applications where thin thickness, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LP171WU7 characteristics provide an excellent flat display for office automation products such as Notebook PC.



General Features

Active Screen Size	17.1 inches diagonal
Outline Dimension	382.2 (H) × 244.6 (V) × 6.5(D, max.) mm
Pixel Pitch	0.191 mm × 0.191 mm
Pixel Format	1920 horiz. by 1200 vert. Pixels RGB strip arrangement
Color Depth	6-bit, 262,144 colors
Luminance, White	300 cd/m ² (typ., @I _{LED} =TBD mA), 5 points Min
Power Consumption	Total 8.99 Watt @LCM circuit 2.87 W(Typ.), LED 6.12W (Typ.)
Weight	705g(Max.)
Display Operating Mode	Transmissive mode, normally white
Surface Treatment	Anti-glare treatment (3H) of the front Polarizer
RoHS Compliance	Yes
BFR / PVC / As Free	Yes for all

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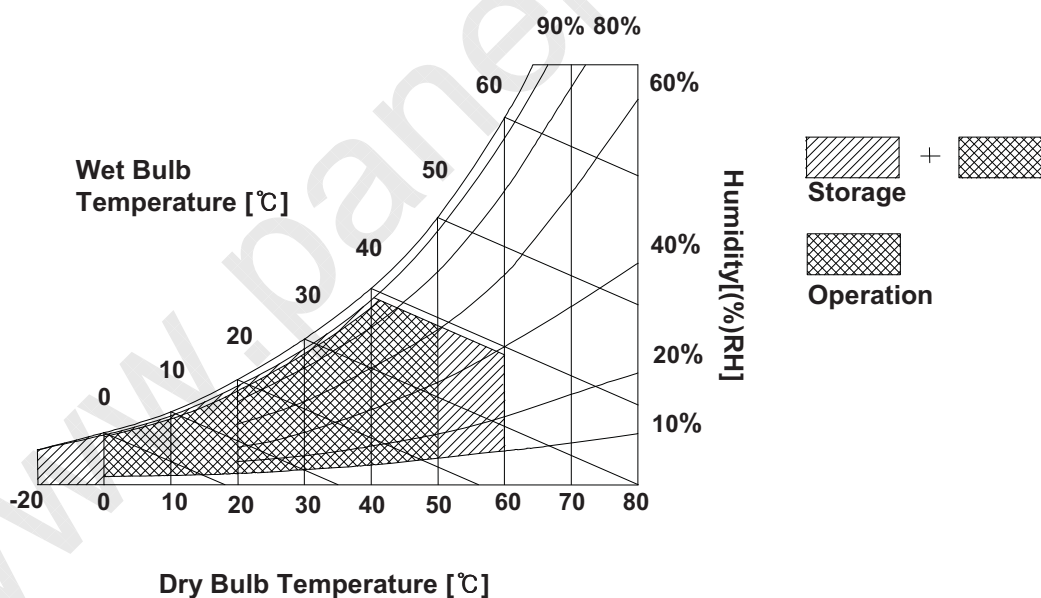
2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Values		Units	Notes
		Min	Max		
Power Input Voltage	VCC	-0.3	4.0	Vdc	at 25 ± 5°C
Operating Temperature	TOP	0	50	°C	1
Storage Temperature	HST	-20	60	°C	1
Operating Ambient Humidity	HOP	10	90	%RH	1
Storage Humidity	HST	10	90	%RH	1

Note : 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39°C Max, and no condensation of water.



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3. Electrical Specifications

3-1. Electrical Characteristics

The LP171WU7 requires two power inputs. The first logic is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second backlight is the input about LED BL with LED Driver.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Values			Unit	Notes
		Min	Typ	Max		
LOGIC :						
Power Supply Input Voltage	VCC	3.0	3.3	3.6	V	1
Power Supply Input Current	ICC	-	870	1000	mA	2
Power Consumption	PCC	-	2.87	3.60	W	2
Power Supply Inrush Current	ICC_P	-	-	1500	mA	4
LVDS Impedance	ZeDP	90	100	110	Ω	5
BACKLIGHT : (with LED Driver)						
LED Power Input Voltage	VLED	7.0	12.0	21.0	V	6
LED Power Input Current	ILED	-	510	586	mA	7
LED Power Consumption	PLED	-	6.12	7.03	W	7
LED Power Inrush Current	ILED_P	-	-	1500	mA	8
PWM Duty Ratio		5	-	100	%	9
PWM Jitter	-	0	-	0.3	%	10
PWM Impedance	ZPWM	20	40	60	k Ω	
PWM Frequency	FPWM	200	-	1000	Hz	11
PWM High Level Voltage	V _{PWM_H}	2.1	3.3	5	V	
PWM Low Level Voltage	V _{PWM_L}	0	-	0.3	V	
LED_EN Impedance	ZPWM	20	40	60	k Ω	
LED_EN High Voltage	VLED_EN_H	3.0	-	5.3	V	
LED_EN Low Voltage	VLED_EN_L	0	-	0.3	V	
SMBus CLK & Data High Level Voltage	V _{SMBusH}	3.0	-	5.3	V	
SMBus CLK & Data Low Level Voltage	V _{SMBus_L}	0	-	0.3	V	
SMBus CLK Frequency	F _{SMBus}	50	55	60	kHz	
SMBus CLK Set-up time	-	250	-	-	us	
SMBus CLK Hold time	-	300	-	-	us	
SMBus CLK Set-up time	-	-	-	1000	us	
SMBus CLK Hold time	-	-	-	300	us	
Life Time		12,000	-	-	Hrs	12

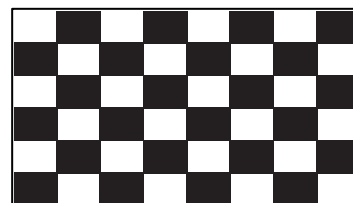


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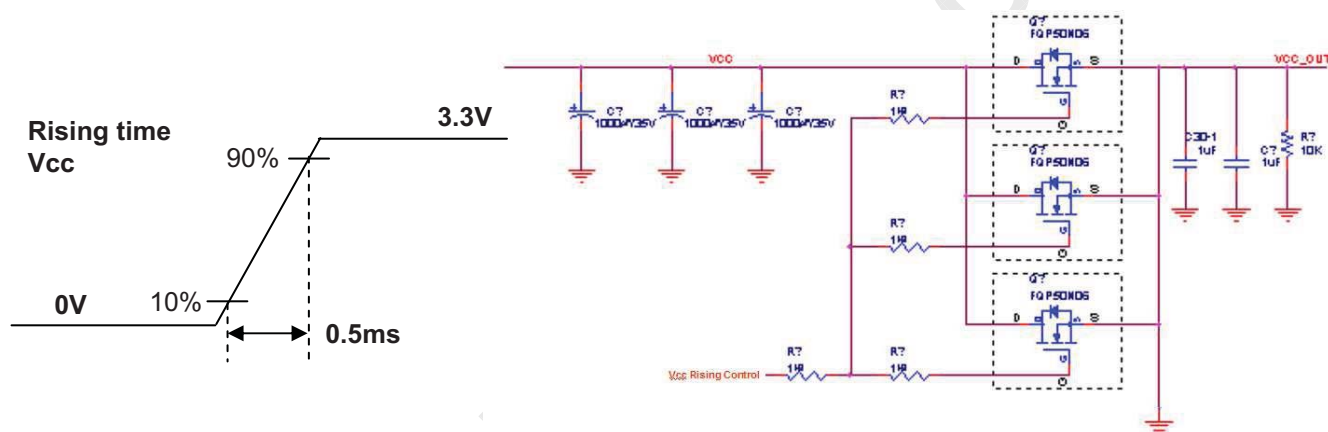
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Note)

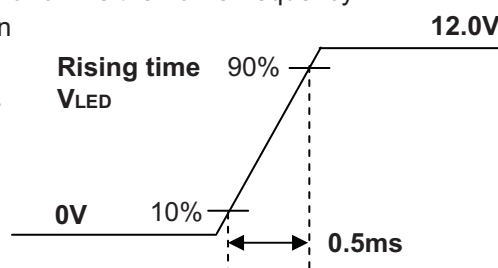
1. The measuring position is the connector of LCM and the test conditions are under 25°C, $f_v = 60\text{Hz}$, Black pattern.
2. The specified I_{cc} current and power consumption are under the $V_{cc} = 3.3\text{V}$, 25°C, $f_v = 60\text{Hz}$ condition whereas Mosaic pattern is displayed and f_v is the frame frequency.



3. This Spec. is the max load condition for the cable impedance designing.
4. The below figures are the measuring V_{cc} condition and the V_{cc} control block LGD used.
The V_{cc} condition is same the minimum of T1 at Power on sequence.



5. This impedance value is needed to proper display and measured form eDP Tx to the mating connector.
6. The measuring position is the connector of LCM and the test conditions are under 25°C.
7. The current and power consumption with LED Driver are under the $V_{led} = 12.0\text{V}$, 25°C, Dimming of Max luminance whereas White pattern is displayed and f_v is the frame frequency.
8. The below figures are the measuring V_{led} condition and the V_{led} control block LGD used.
 V_{LED} control block is same with V_{cc} control block.



9. The operation of LED Driver below minimum dimming ratio may cause flickering or reliability issue.
10. If Jitter of PWM is bigger than maximum. It may cause flickering.
11. This Spec. is not effective at 100% dimming ratio as an exception because it has DC level equivalent to 0Hz. In spite of acceptable range as defined, the PWM Frequency should be fixed and stable for more consistent brightness control at any specific level desired.
12. The life time is determined as the time at which the typical brightness of LCD is 50% compare to that of initial value at the typical LED current. These LED backlight has 6 strings on it and the typical current of LED's string is base on TBDmA.

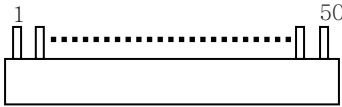
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3-2. Interface Connections

This LCD employs two interface connections, a 50 pin connector is used for the module electronics interface and the other connector is used for the internal backlight system.

The electronics interface connector is a model FI-VHP50S manufactured by JAE.

Table 3. MODULE CONNECTOR PIN CONFIGURATION (CN1)

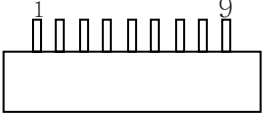
Pin	Symbol	Description	Notes
1	Test loop	Dell test loop to pin 30	1, Interface chips 1.1 LCD : SW, ST2_BS (LCD Controller) including LVDS Receiver 1.2 System : * Pin to Pin compatible with LVDS 2.Connector 2.1 LCD :JAE FI-VHP50 or equivalent (1.0 mm thickness, lock-in type, pin 1 starts from left on the front) 2.2 Mating:JAE FI-VHP50 series or equivalent (micro-coax type) 2.3 Connector pin arrangement LCD rear view  [LCD Module Rear View]
2	V_EEDID	EDID 3.3V power	
3	GND	Ground	
4	CLK EEDID	EDID clock	
5	DATA EEDID	EDID data	
6	GND	Ground	
7	Odd_Rin0-	Negative LVDS differential data input	
8	Odd_Rin0+	Positive LVDS differential data input	
9	GND	Ground	
10	Odd_Rin1-	Negative LVDS differential data input	
11	Odd_Rin1+	Positive LVDS differential data input	
12	GND	Ground	
13	Odd_Rin2-	Negative LVDS differential data input	
14	Odd_Rin2+	Positive LVDS differential data input	
15	GND	Ground	
16	Odd_ClkIN-	Negative LVDS differential clock input	
17	Odd_ClkIN+	Positive LVDS differential clock input	
18	GND	Ground	
19	Even_Rin0-	Negative LVDS differential data input	
20	Even_Rin0+	Positive LVDS differential data input	
21	GND	Ground	
22	Even_Rin1-	Negative LVDS differential data input	
23	Even_Rin1+	Positive LVDS differential data input	
24	GND	Ground	
25	Even_Rin2-	Negative LVDS differential data input	
26	Even_Rin2+	Positive LVDS differential data input	
27	GND	Ground	
28	Even_ClkIN-	Negative LVDS differential clock input	
29	Even_ClkIN+	Positive LVDS differential clock input	
30	Test loop	Dell test loop to pin 1	

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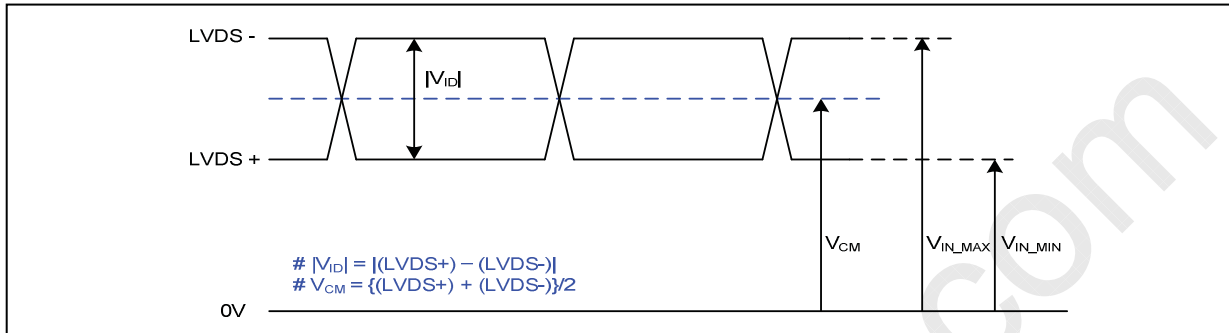
31	Test loop	Dell test loop to pin 50
32	VCC	Logic power 3.3V
33	VCC	Logic power 3.3V
34	BIST_EN	Panel Self Test
35	LED_EN	LED Controller Supply Voltage (+5V_ALW)
36	GND	Ground
37	GND	Ground
38	PWM	PWM brightness control
39	GND	Ground (VBL-)
40	GND	Ground (VBL-)
41	GND	Ground (VBL-)
42	GND	Ground (VBL-)
43	NC	No connect
44	VLED	7.5V ~ 21V LED power
45	VLED	7.5V ~ 21V LED power
46	VLED	7.5V ~ 21V LED power
47	VLED	7.5V ~ 21V LED power
48	SMB_DATA	SMBus Data
49	SMB_CLK	SMBus Clk
50	Test loop	Dell test loop to pin 31

The LED backlight connector is a model TF12-9S-0.5H, manufactured by Hirose.

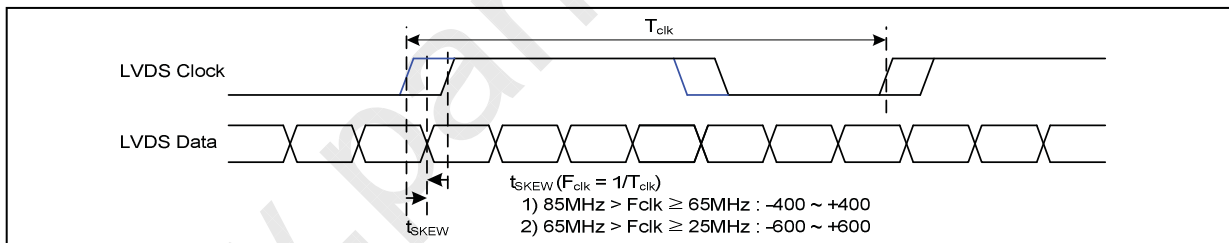
Table 4. BACKLIGHT CONNECTOR PIN CONFIGURATION (CN2)

Pin	Symbol	Description	Notes
1	Vdc(1,2,3,4,5,6)	LED Anode(Positive)	
2	Vdc(1,2,3,4,5,6)	LED Anode(Positive)	
3	NC	No Connection	
4	Vdc1	LED Cathode (Negative)	
5	Vdc2	LED Cathode (Negative)	
6	Vdc3	LED Cathode (Negative)	
7	Vdc4	LED Cathode (Negative)	
8	Vdc5	LED Cathode (Negative)	
9	Vdc6	LED Cathode (Negative)	

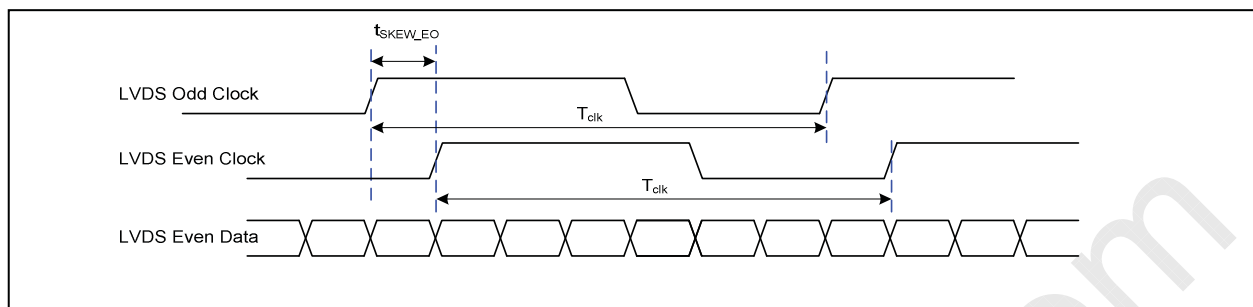
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3-3. LVDS Signal Timing Specifications**3-3-1. DC Specification**

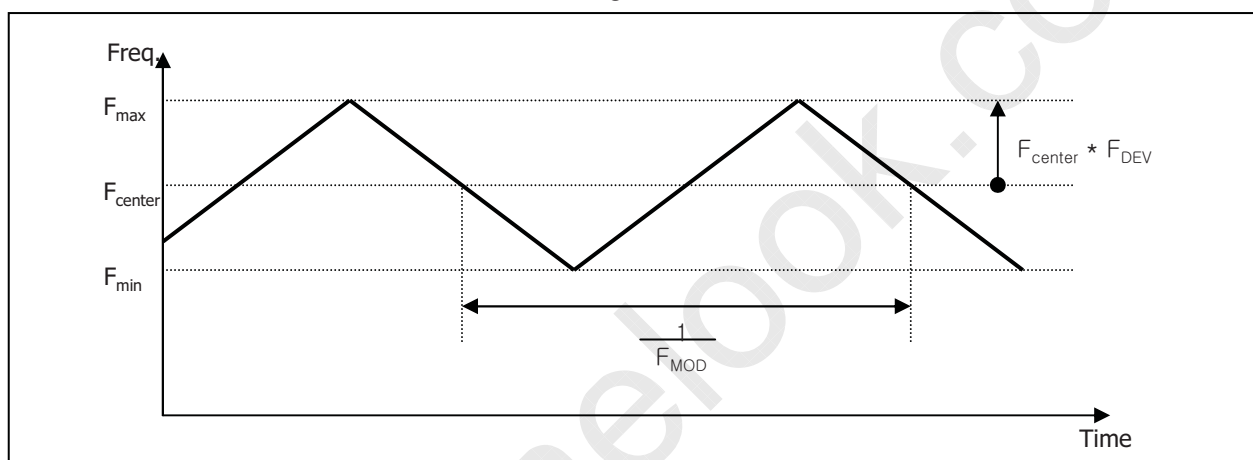
Description	Symbol	Min	Max	Unit	Notes
LVDS Differential Voltage	V_{ID}	100	600	mV	-
LVDS Common mode Voltage	V_{CM}	0.6	1.8	V	-
LVDS Input Voltage Range	V_{IN}	0.3	2.1	V	-

3-3-2. AC Specification

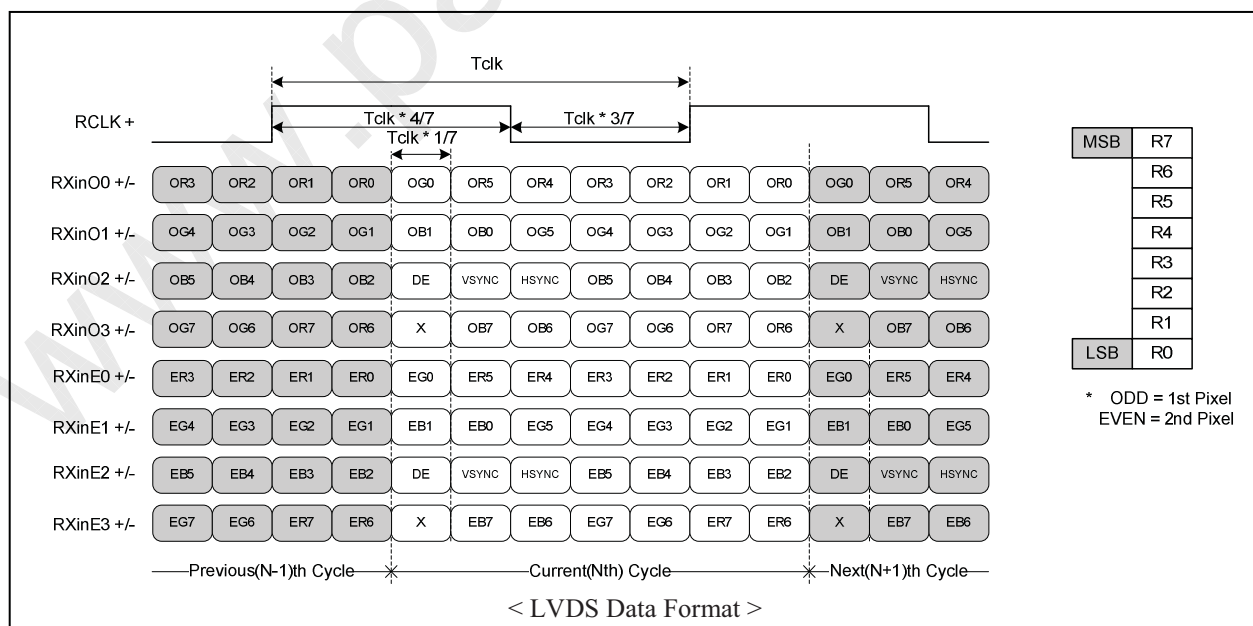
Description	Symbol	Min	Max	Unit	Notes
LVDS Clock to Data Skew Margin	t_{SKEW}	- 400	+ 400	ps	$85MHz > F_{clk} \geq 65MHz$
	t_{SKEW}	- 600	+ 600	ps	$65MHz > F_{clk} \geq 25MHz$
LVDS Clock to Clock Skew Margin (Even to Odd)	t_{SKEW_EO}	- 1/7	+ 1/7	T_{clk}	-
Maximum deviation of input clock frequency during SSC	F_{DEV}	-	± 3	%	-
Maximum modulation frequency of input clock during SSC	F_{MOD}	-	200	KHz	-

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< Clock skew margin between channel >



< Spread Spectrum >

3-3-3. Data Format
1) LVDS 2 Port


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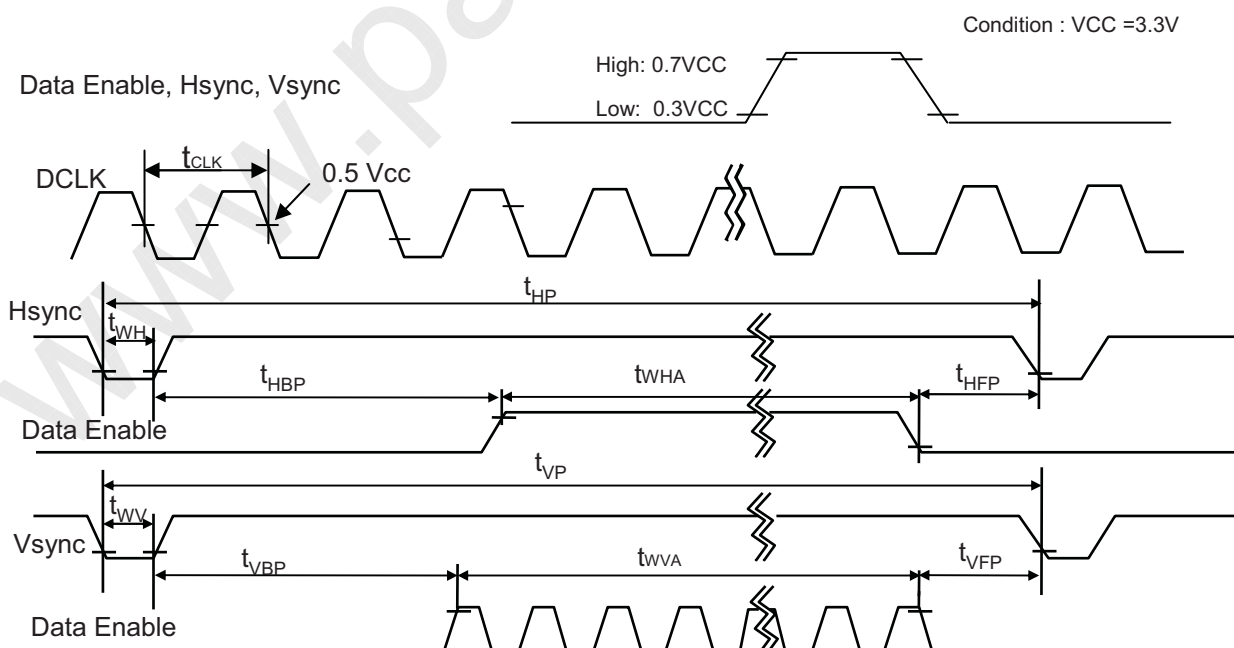
3-4. Signal Timing Specifications

This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications and specifications of LVDS Tx/Rx for its proper operation.

Table 5. TIMING TABLE

ITEM	Symbol		Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	f_{CLK}	-	142.8	-	MHz	
Hsync	Period	t_{HP}	1990	2000	2010	tCLK	
	Width	t_{WH}	32	32	32		
	Width-Active	tw_{HA}	1920	1920	1920		
Vsync	Period	t_{VP}	1210	1215	1220	tHP	
	Width	t_{WV}	6	6	6		
	Width-Active	tw_{VA}	1200	1200	1200		
Data Enable	Horizontal back porch	t_{HBP}	29	34	39	tCLK	
	Horizontal front porch	t_{HFP}	9	14	19		
	Vertical back porch	t_{VBP}	3	6	8	tHP	
	Vertical front porch	t_{VFP}	1	3	6		

3-5. Signal Timing Waveforms



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3-6. Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color ; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 6. COLOR DATA REFERENCE

Color		Input Color Data																	
		RED						GREEN						BLUE					
		MSB			LSB			MSB			LSB			MSB			LSB		
		R 5	R 4	R 3	R 2	R 1	R 0	G 5	G 4	G 3	G 2	G 1	G 0	B 5	B 4	B 3	B 2	B 1	B 0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	...	...						...						...					
	RED (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	...	...						...						...					
	GREEN (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	GREEN (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
BLUE	BLUE (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	...	...						...						...					
	BLUE (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	BLUE (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1



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3-7. Power Sequence

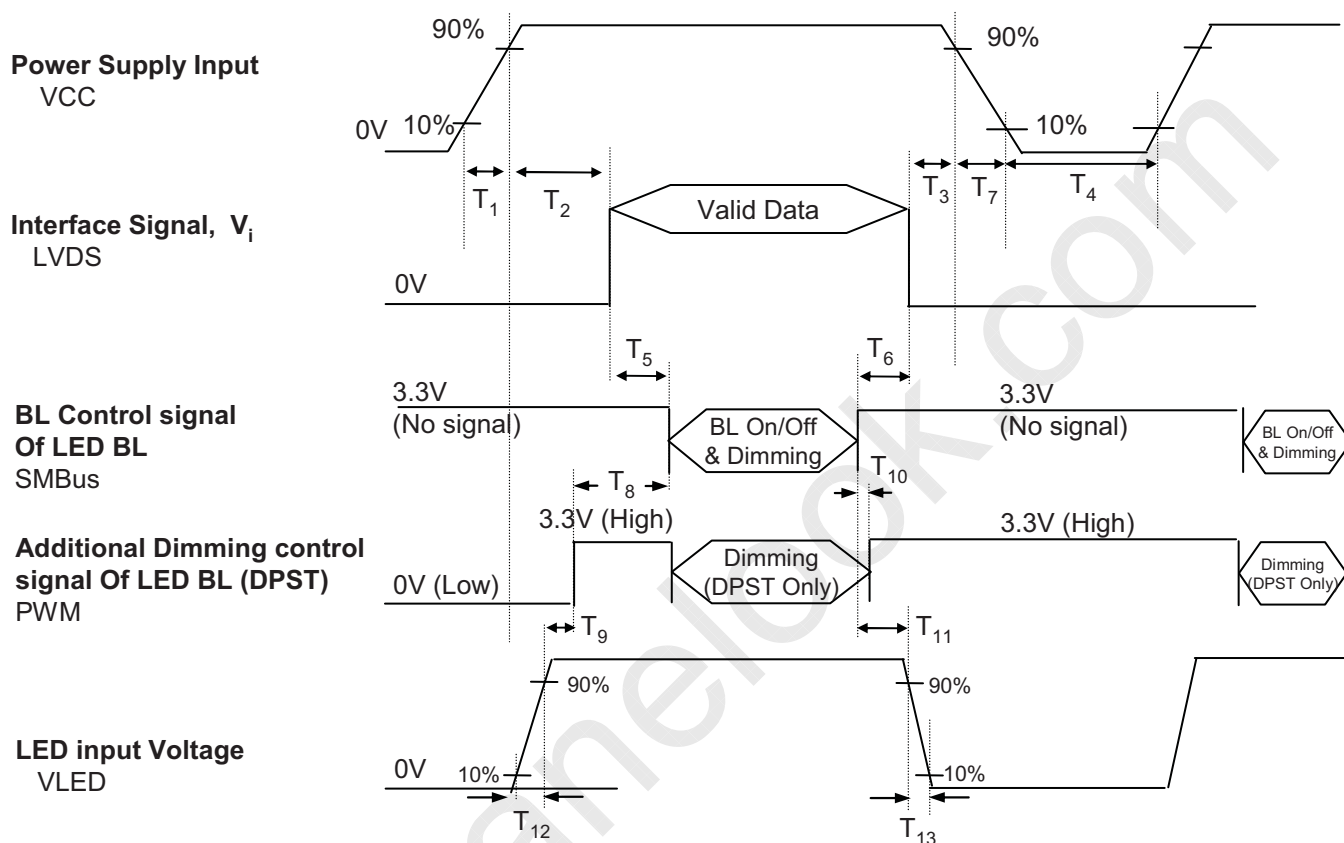


Table 6. POWER SEQUENCE TABLE

Logic Parameter	Value			Units	LED Parameter	Value			Units
	Min.	Typ.	Max.			Min.	Typ.	Max.	
T ₁	0.5	-	10	ms	T ₈	200	-	-	ms
T ₂	0	-	50	ms	T ₉	0	-	-	ms
T ₃	0	-	50	ms	T ₁₀	0	-	50	ms
T ₄	400	-	-	ms	T ₁₁	50	-	-	ms
T ₅	200	-	-	ms	T ₁₃	0	-	5000	ms
T ₆	200	-	-	ms	T ₁₂	0.5	-	-	ms
T ₇	3	-	10	ms					

Note)

1. Do not insert the mating cable when system turn on.
2. Valid Data have to meet "3-3. LVDS Signal Timing Specifications"
3. LVDS, SMBus and PWM need to be on pull-down condition on invalid status of system.
4. LGD recommend the rising sequence of VLED after the Vcc and valid status of LVDS turn on.

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4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 20 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and Θ equal to 0°.

FIG. 1 presents additional information concerning the measurement equipment and method.

FIG. 1 Optical Characteristic Measurement Equipment and Method

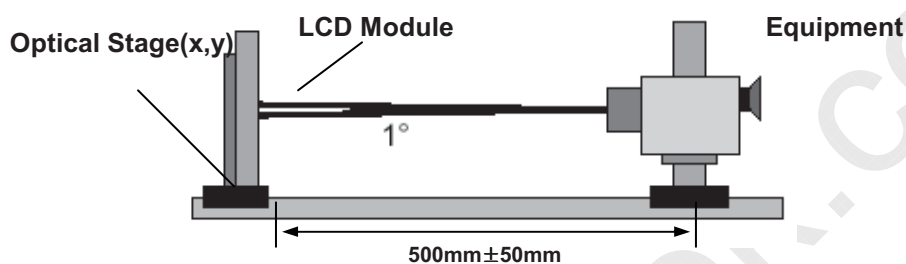


Table 7. OPTICAL CHARACTERISTICS

Ta=25°C, VCC=3.3V, fv=60Hz, fCLK= 142.8 MHz

Parameter	Symbol	Values			Units	Notes
		Min	Typ	Max		
Contrast Ratio	CR	500	600	-		1
Surface Luminance, white	L _{WH}	260	300	-	cd/m²	2
Luminance Variation	δ _{WHITE}		-	35	%	3
Response Time	Tr _R + Tr _D	-	16	25	ms	4
Color Coordinates						
RED	RX	0.580	0.610	0.640		
	RY	0.318	0.348	0.378		
GREEN	GX	0.298	0.329	0.358		
	GY	0.555	0.586	0.615		
BLUE	BX	0.123	0.153	0.183		
	BY	0.109	0.140	0.169		
WHITE	WX	0.283	0.313	0.343		
	WY	0.299	0.329	0.359		
Viewing Angle						5
x axis, right(Φ=0°)	Θ _r	60	65	-	degree	
x axis, left (Φ=180°)	Θ _l	60	65	-	degree	
y axis, up (Φ=90°)	Θ _u	40	45	-	degree	
y axis, down (Φ=270°)	Θ _d	50	55	-	degree	
Gray Scale						6
Color Gamut	C/G	-	50	-	%	
Gamma	γ	-	2.2	-		

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Note)

1. Contrast Ratio(CR) is defined mathematically as

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

2. Surface luminance is the average of 5 point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see FIG 1.

$$\text{LWH} = \text{Average}(\text{L1}, \text{L2}, \dots \text{L5})$$

3. The variation in surface luminance, The panel total variation (δ WHITE) is determined by measuring LN at each test position 1 through 13 and then defined as following numerical formula.
For more information see FIG 2.

$$\delta \text{ WHITE} (= \frac{\text{Maximum}(\text{L1}, \text{L2}, \dots \text{L13}) - \text{Minimum}(\text{L1}, \text{L2}, \dots \text{L13})}{\text{Maximum}(\text{L1}, \text{L2}, \dots \text{L13})} * 100(\%)$$

4. Response time is the time required for the display to transition from white to black (rise time, TrR) and from black to white(Decay Time, TrD). For additional information see FIG 3.

5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 4.

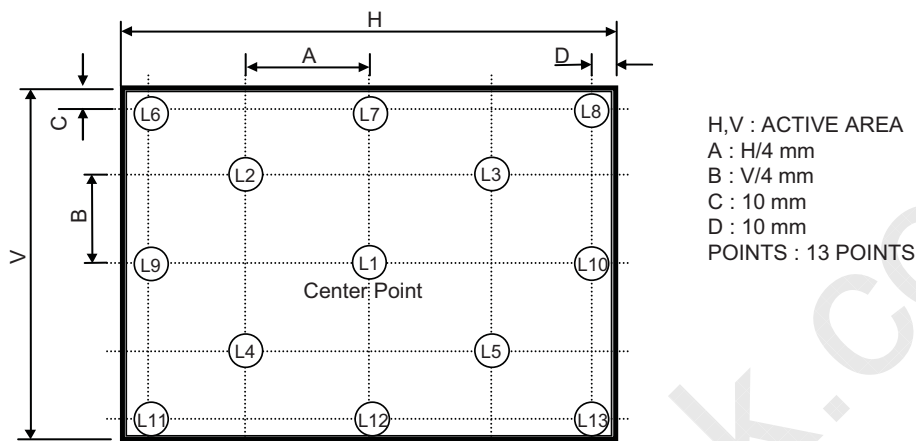
6. Gray scale specification

* fV = 60Hz

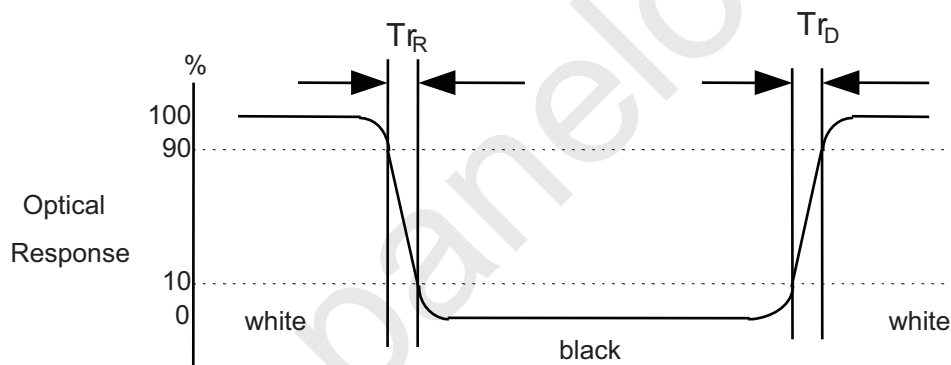
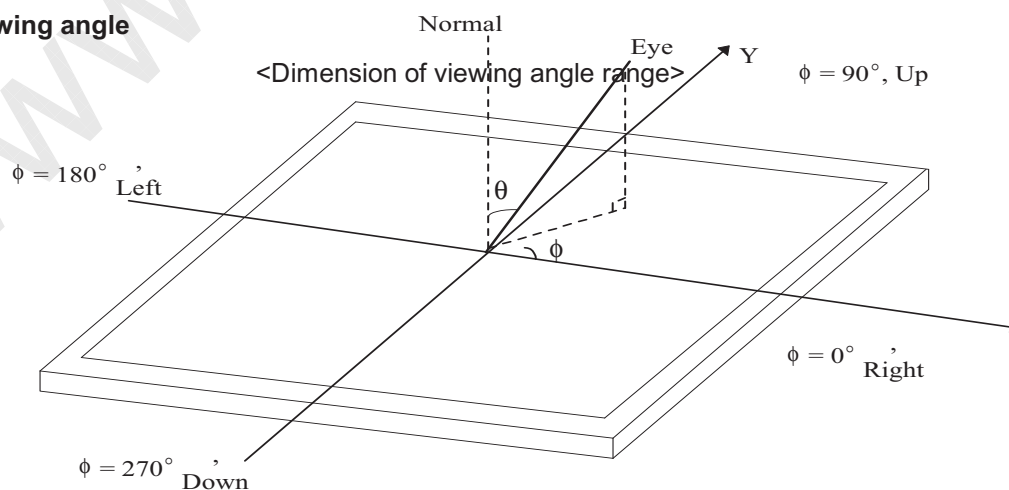
Gray Level	Luminance [%] (Typ)
L0	0.13
L7	1.85
L15	6.78
L23	43.87
L31	23.79
L39	39.39
L47	59.38
L55	80.83
L63	100

Product Specification
FIG. 2 Luminance

<Measuring point for Average Luminance & measuring point for Luminance variation>


FIG. 3 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white".


FIG. 4 Viewing angle


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5. Mechanical Characteristics

The contents provide general mechanical characteristics for the model LP171WU7.
In addition the figures in the next page are detailed mechanical drawing of the LCD.

Outline Dimension	Horizontal	382.2 ± 0.5mm
	Vertical	244.6 ± 0.5mm
	Thickness	6.5mm (max)
Bezel Area	Horizontal	370.6 ± 0.5mm
	Vertical	232.9 ± 0.5mm
Active Display Area	Horizontal	367.2 mm
	Vertical	229.5 mm
Weight	705g (Max.)	
Surface Treatment	Hard Coating (3H), Anti-Glare treatment of the front polarizer	

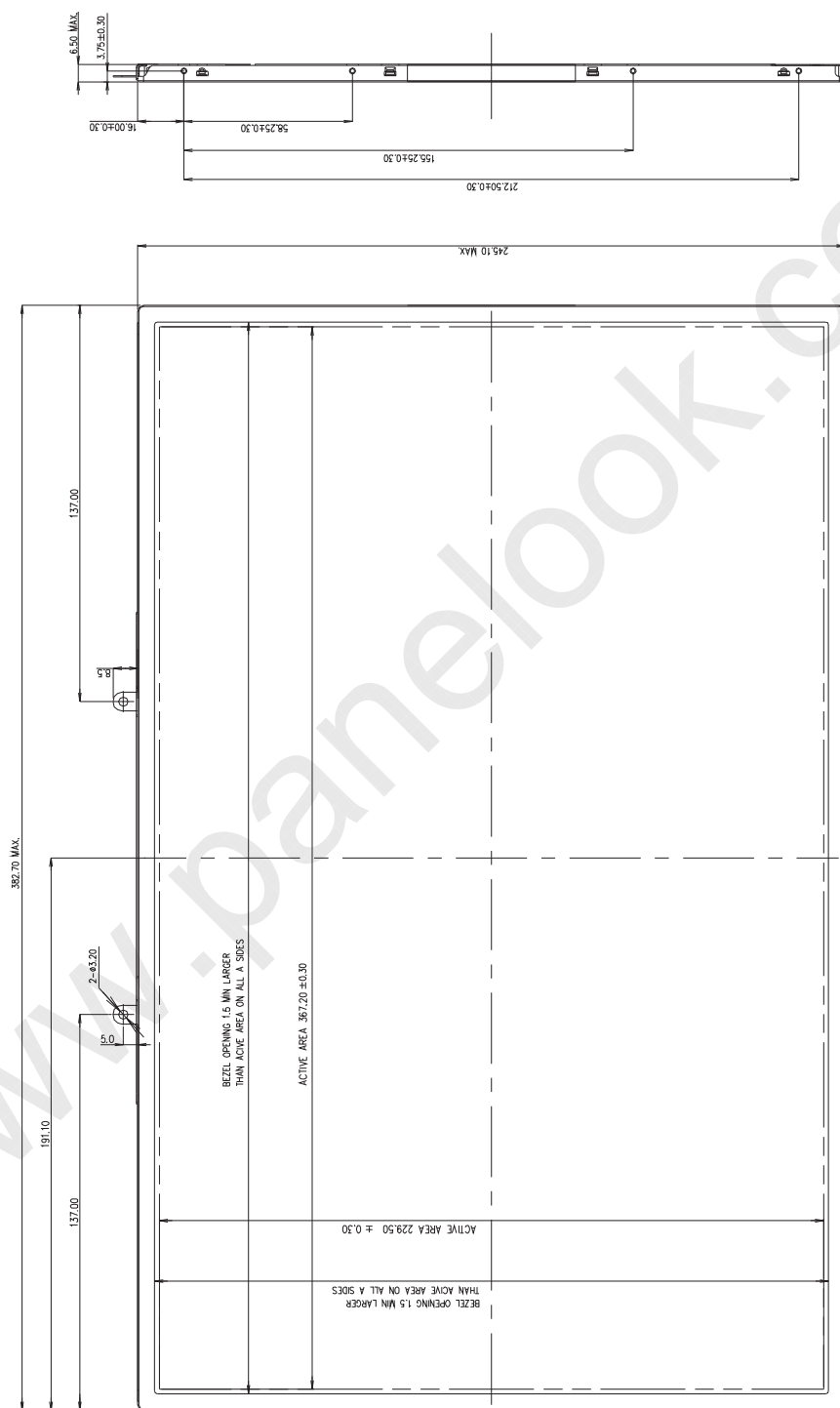


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<FRONT VIEW>

Note) Unit:[mm], General tolerance: $\pm 0.5\text{mm}$



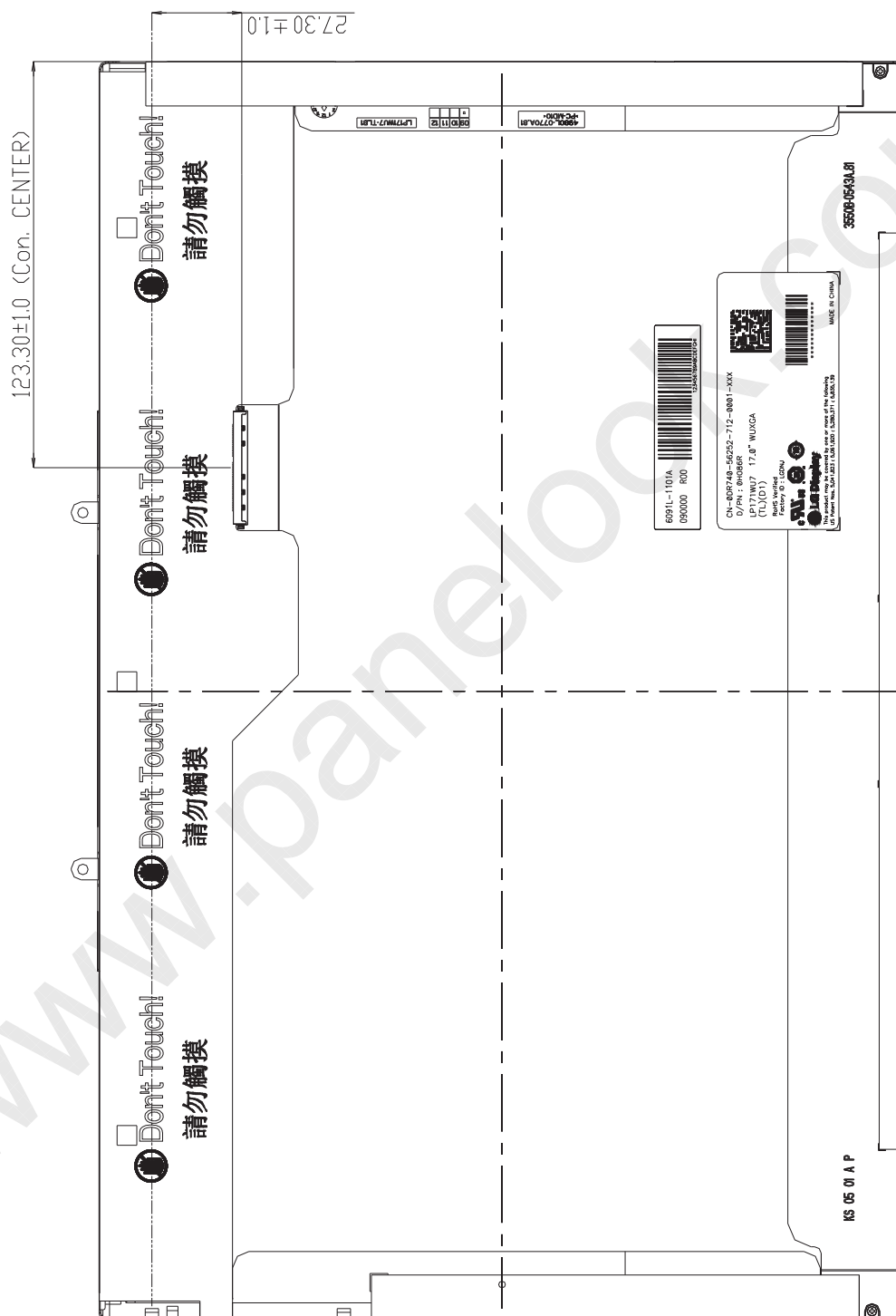


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<REAR VIEW>

Note) Unit:[mm], General tolerance: $\pm 0.5\text{mm}$

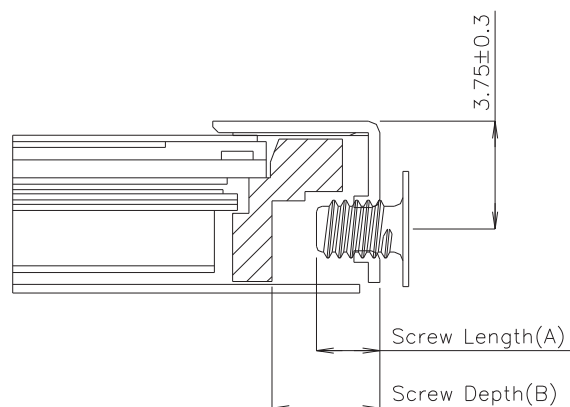




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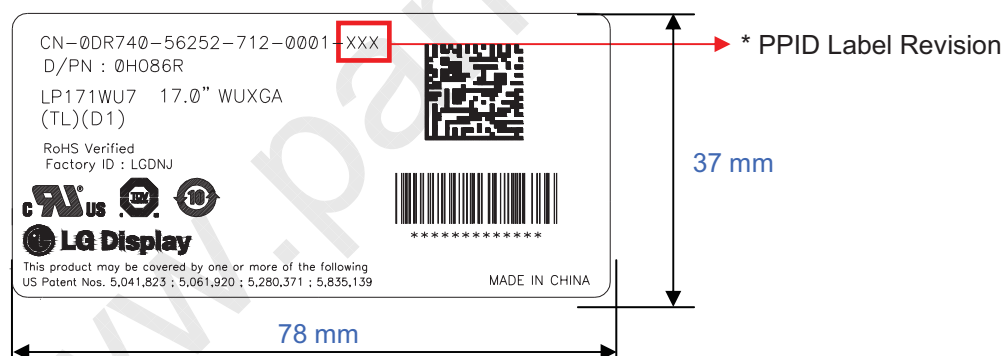
Product Specification

[DETAIL DESCRIPTION OF SIDE MOUNTING SCREW]



- * Screw Length(A) : Max : 2.5, Min : 2.0
- * Screw Depth(B) : Min 2.5
- * Screw Torque : Max 2.5kgf.cm (Measurement Gauge:Torque Meter)

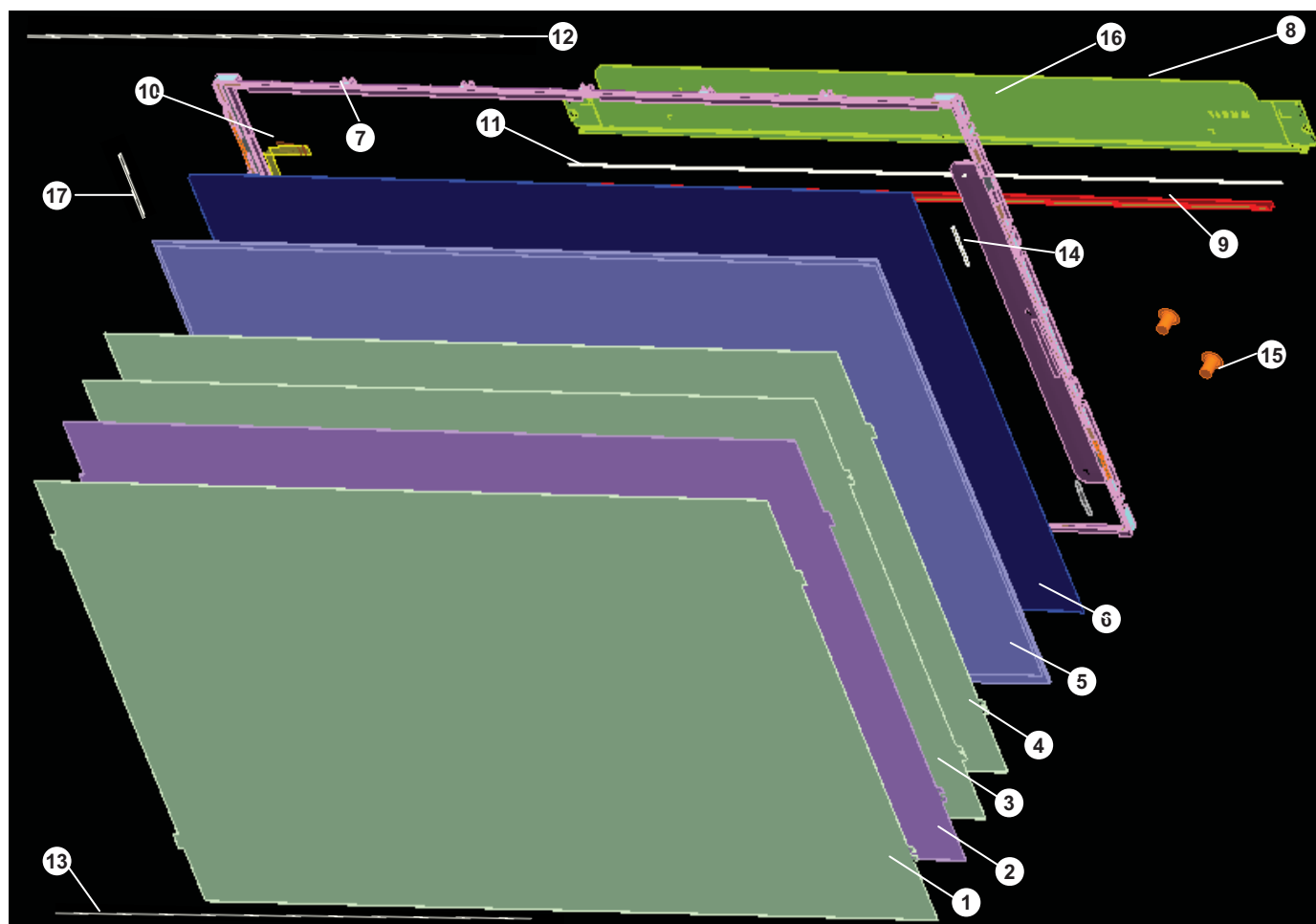
[DETAIL INFORMATION OF PPID LABEL AND REVISION CODE]



* PPID Label Revision :

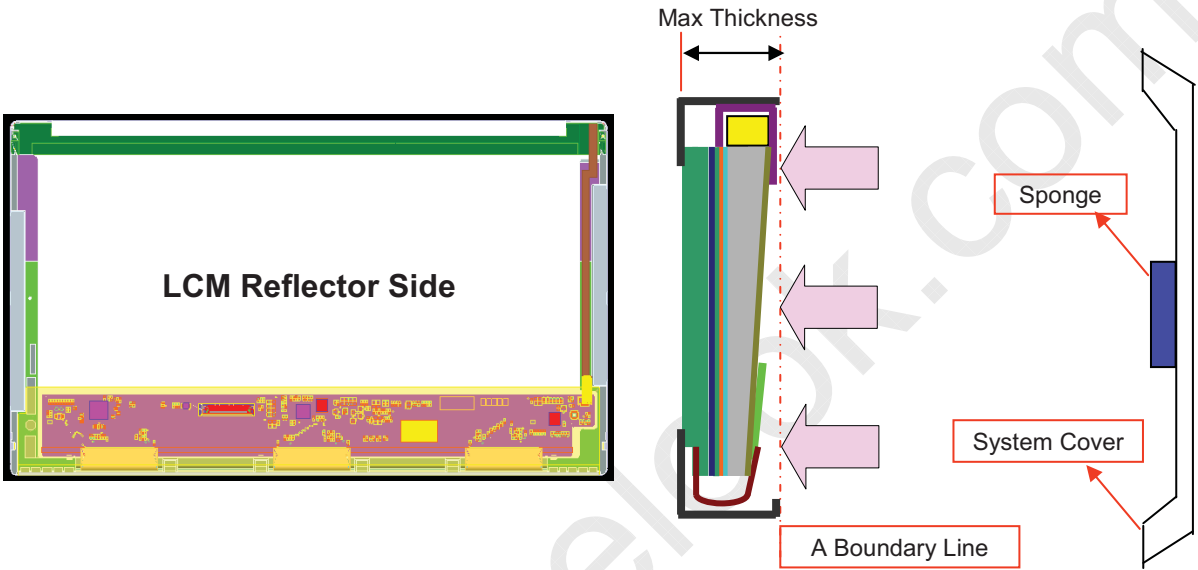
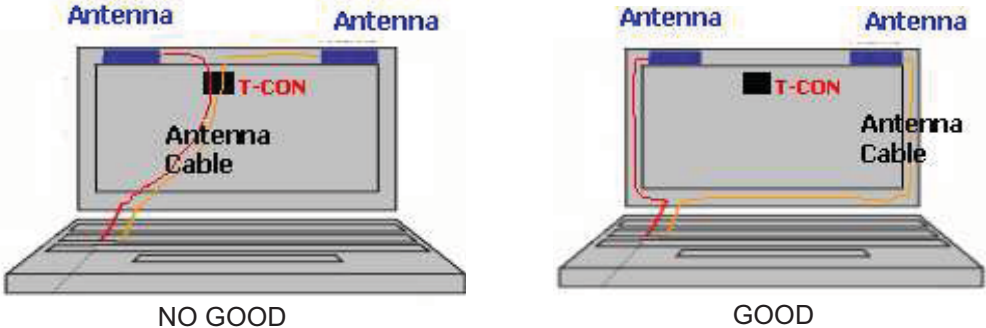
It is subject to change with Dell event. Please refer to the below table for detail.

Classification	No Change	1st Revision	2nd Revision	...	9th Revision	...
SST(WS)	X00	X01	X02	...	A09	...
PT(ES)	X10	X11	X12	...	A19	...
ST(CS)	X20	X21	X22	...	A29	...
XB(MP)	A00	A01	A02	...	A09	...

Backlight Exploded View. (Appendix)


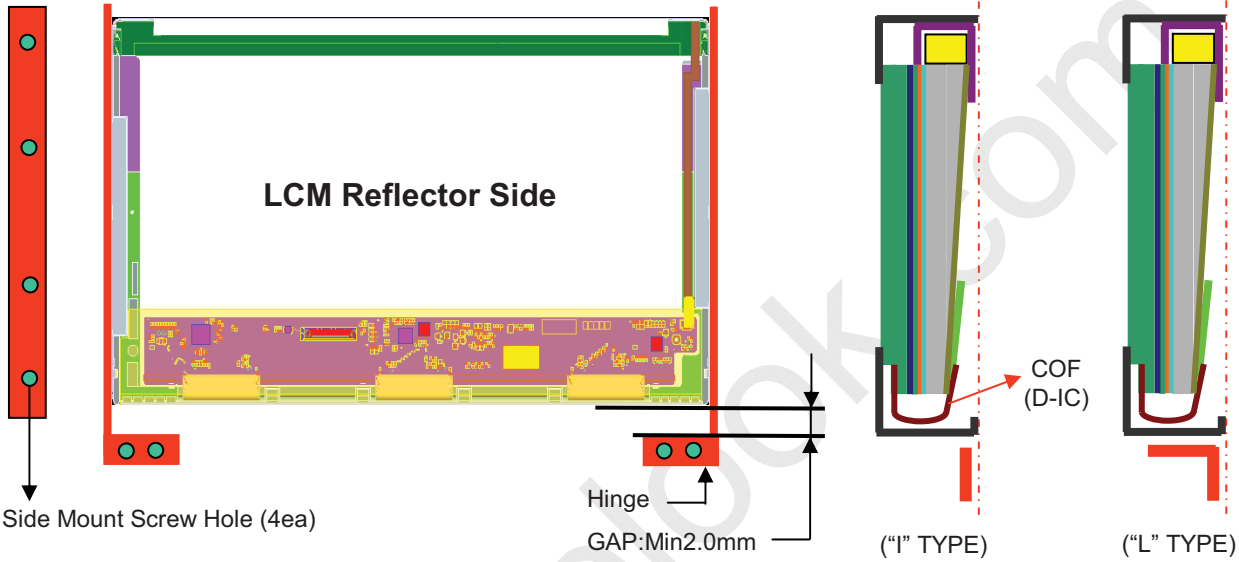
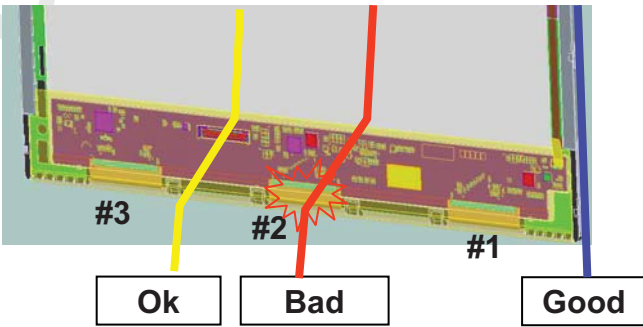
No	Part Name	No	Part Name
1	Diffuser Up Sheet	10	LED Array
2	Prism Up Sheet	11	Cover Bottom Fixing Double Tape
3	Prism Down Sheet	12	LGP Fixing Double Tape
4	Diffuser Down Sheet	13	Reflective Single Tape
5	Light Guide Panel	14	Sheet Fixing Pad (4pcs)
6	Reflector	15	Screw (2pcs)
7	Supporter Main	16	Reflector Fixing Tape
8	Cover Bottom	17	FPC Fixing Tape
9	LED Housing		

LGD Proposal for system cover design.(Appendix)

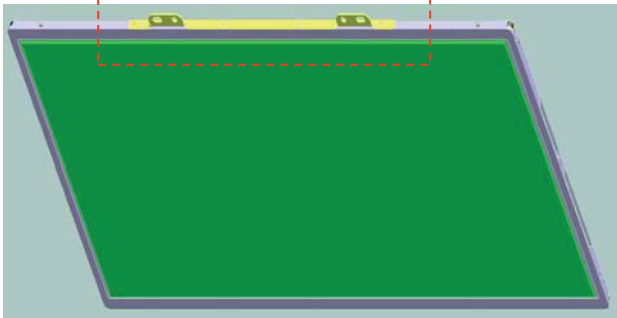
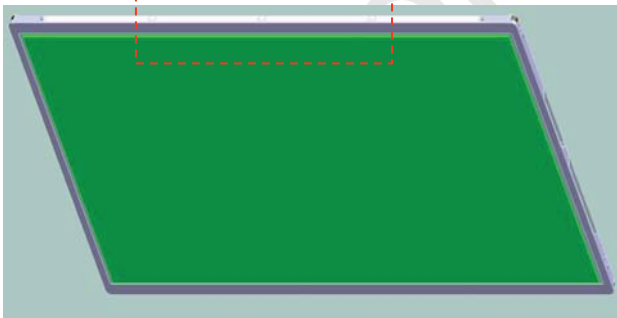
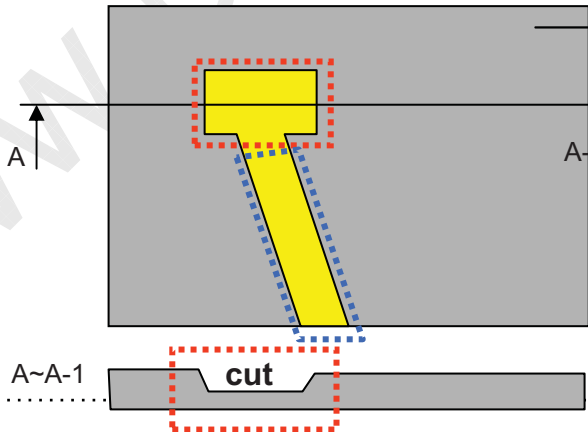
1	Gap check for securing the enough gap between LCM and System cover.	
 The diagram illustrates the gap check for securing the LCM and System cover. It shows the LCM Reflector Side, a cross-section of the LCM with a 'Max Thickness' dimension, a 'Boundary Line' indicated by a red dashed line, a 'Sponge' layer, and the 'System Cover'.		
Define	1.Rear side of LCM is sensitive against external stress,and previous check about interference is highly needed. 2.In case there is something from system cover comes into the boundary above,mechanical interference may cause the FOS defects. (Eg:Ripple,White spot..)	
2	Check if antenna cable is sufficiently apart from T-CON of LCD Module.	
Define	 The diagram shows two scenarios for antenna cable placement relative to the T-CON. The left scenario, labeled 'NO GOOD', shows the antenna cable overlapping the T-CON. The right scenario, labeled 'GOOD', shows the antenna cable positioned away from the T-CON.	
	1.If system antenna is overlapped with T-CON,it might be cause the noise.	

Product Specification

LGD Proposal for system cover design.

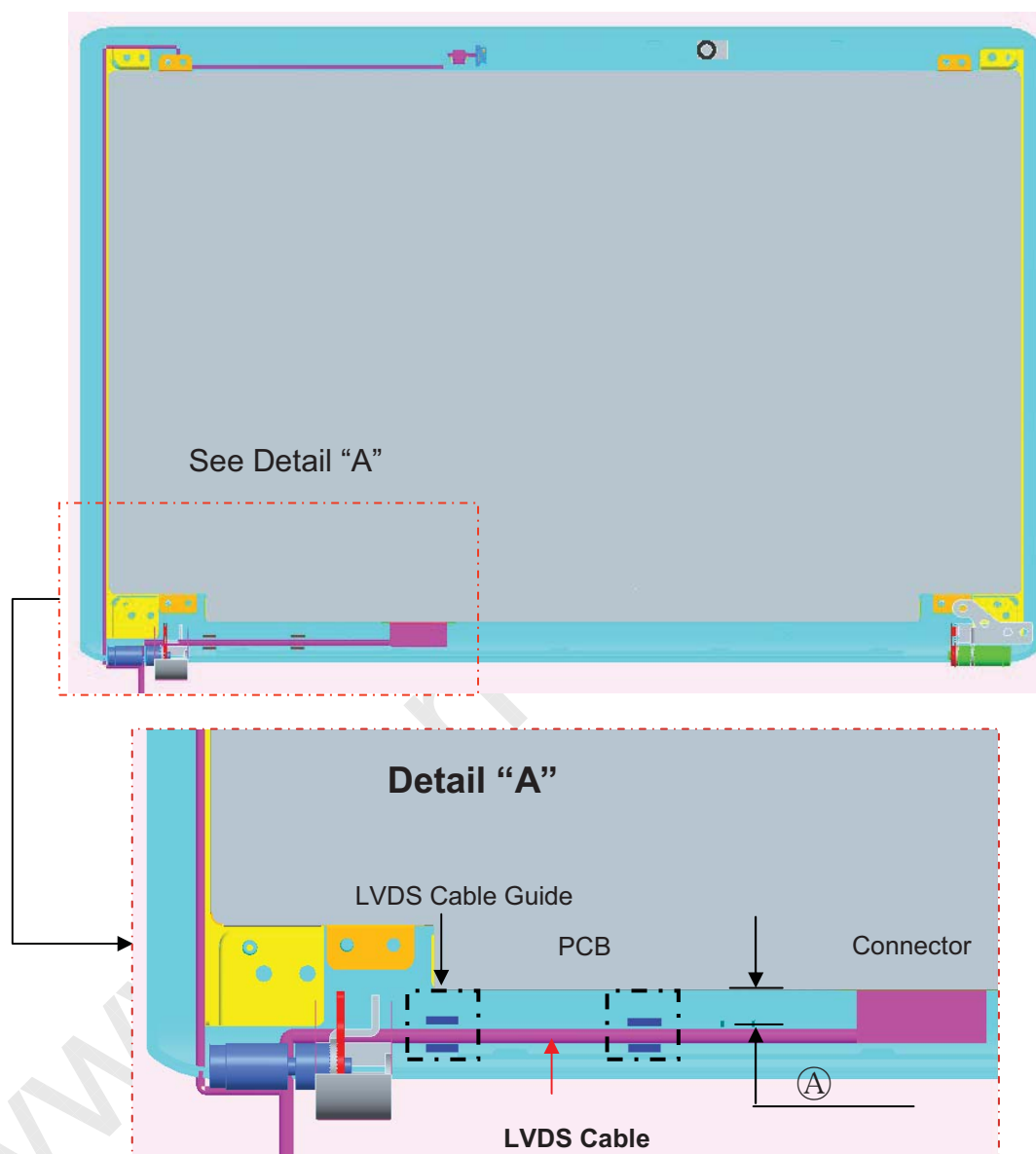
3	Gap check for securing the enough gap between LCM and System hinge.	
	 LCM Reflector Side Side Mount Screw Hole (4ea) Hinge GAP: Min 2.0mm COF (D-IC) ("I" TYPE) ("L" TYPE)	
Define	1. At least 2.0mm of gap needs to be secured to prevent the shock related defects. 2. "L" type of hinge is recommended than "I" type under shock test.	
4	Checking the path of the System wire.	
	 #3 #2 #1 Ok Bad Good	
Define	1. COF area needs to be handled with care. 2. GOOD → Wire path design to system side. OK → Wire path is located between COFs. BAD → Wire path overlapped with COF area.	

LGD Proposal for system cover design.

5	Using a bracket on the top of LCM is not recommended.	
 bracket  With bracket  Without bracket		
Define	1.Condition without bracket is good for mechanical noise,and can minimize the light leakage from deformation of bracket. 2.The results shows that there is no difference between the condition with or without bracket.	
6	Securing additional gap on CNT area..	
 System cover inner side. User connector area. User connector Cable pathway. FPC:Flexible Printed Circuit.		
Define	1.CNT area is specially sensitive against external stress,and additional gap by cutting on system cover will be helpful on removing the Ripple. 2.Using a thinner CNT will be better. (eg: FPC type)	
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Checking the path of the System LVDS Cable.

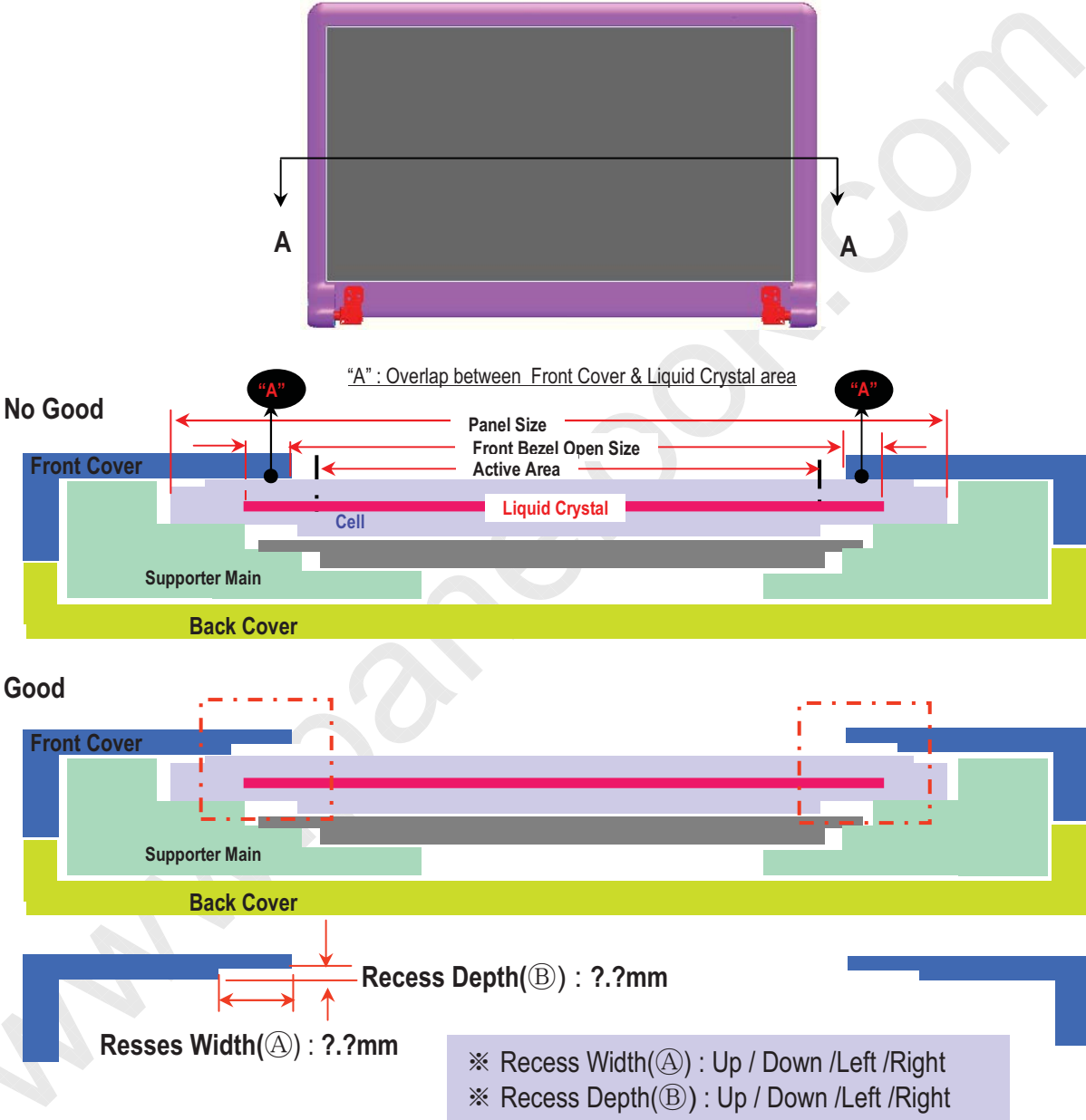


Define

1. At least 1.0mm of gap needs to be secured to prevent the overlap between LVDS cable and PCB. ($\textcircled{A} \geq 1.0\text{mm}$)
(This overlap may cause a Abnormal Display after hinge test)
2. "Flat" type of LVDS cable is recommended than "Cylindrical" type .
3. Making LVDS Cable Guide will be better. (Refer to detail "A")

Product Specification

LGD Proposal for system cover design.

8	Securing additional gap between front cover & LCD at edge of front cover.
	 No Good Good Recess Width(Ⓐ) : ?.?mm Recess Depth(Ⓑ) : ?.?mm ※ Recess Width(Ⓐ) : Up / Down /Left /Right ※ Recess Depth(Ⓑ) : Up / Down /Left /Right
Define	1.Liquid Crystal area is sensitive against external stress, so additional gap by making recess area at the edge of front cover will be helpful on removing a Ripple.(Dimension of Recess depends on each model)

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6. Reliability

Environment test condition

No.	Test Item	Conditions
1	High temperature storage test	Ta= 60°C, 240h
2	Low temperature storage test	Ta= -20°C, 240h
3	High temperature operation test	Ta= 50°C, 50%RH, 240h
4	Low temperature operation test	Ta= 0°C, 240h
5	Vibration test (non-operating)	Sine wave, 5 ~ 150Hz, 1.5G, 0.37oct/min 3 axis, 30min/axis
6	Shock test (non-operating)	Half sine wave, 180G, 2ms one shock of each six faces(I.e. run 180G 2ms for all six faces)
7	Altitude operating storage / shipment	0 ~ 10,000 feet (3,048m) 24Hr 0 ~ 40,000 feet (12,192m) 24Hr

{ Result Evaluation Criteria }

There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.

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7. International Standards

7-1. Safety

- a) UL 60950-1, Second Edition, Underwriters Laboratories Inc.
Information Technology Equipment - Safety - Part 1 : General Requirements.
- b) CAN/CSA C22.2 No.60950-1-07, Second Edition, Canadian Standards Association.
Information Technology Equipment - Safety - Part 1 : General Requirements.
- c) EN 60950-1:2006 + A11:2009, European Committee for Electrotechnical Standardization(CENELEC).
Information Technology Equipment - Safety - Part 1 : General Requirements.
- d) IEC 60950-1:2005, Second Edition, The International Electrotechnical Commission (IEC).
Information Technology Equipment - Safety - Part 1 : General Requirements.

7-2. EMC

- a) ANSI C63.4 – 2003 "American National Standard for Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electronic Equipment in the Range of 9 kHz to 40 GHz." American National Standards Institute (ANSI), 2003.
- b) C.I.S.P.R. Pub. 22. Limits and methods of measurement of radio interference characteristics of information technology equipment." International Special Committee on Radio Interference (C.I.S.P.R.), 2005.
- c) EN 55022 "Limits and methods of measurement of radio interference characteristics of information technology equipment." European Committee for Electrotechnical Standardization (CENELEC), 2006.

7-3. Environment

- a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003

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8. Packing

8-1. Designation of Lot Mark

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M
---	---	---	---	---	---	---	---	---	---	---	---	---

A,B,C : SIZE(INCH)

E : MONTH

D : YEAR

F ~ M : SERIAL NO.

Note

1. YEAR

Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Mark	1	2	3	4	5	6	7	8	9	0

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial No. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one box : 20 pcs

b) Box Size : 482mm × 371mm × 325mm



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9. PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD module.

9-1. MOUNTING PRECAUTIONS

- (1) You must mount a module using holes arranged in four corners or four sides.
- (2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to resist external force.
- (4) You should adopt radiation structure to satisfy the temperature specification.
- (5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- (6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)
- (7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- (8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (9) Do not open the case because inside circuits do not have sufficient strength.

9-2. OPERATING PRECAUTIONS

- (1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
 $V = \pm 200\text{mV}$ (Over and under shoot voltage)
- (2) Response time depends on the temperature. (In lower temperature, it becomes longer.)
- (3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.
- (4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
- (6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.



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9-3. ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

9-5. STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

- (1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- (2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. HANDLING PRECAUTIONS FOR PROTECTION FILM

- (1) When the protection film is peeled off, static electricity is generated between the film and polarizer.
This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- (2) The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to remain on the polarizer.
Please carefully peel off the protection film without rubbing it against the polarizer.
- (3) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
- (4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.



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APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 1/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Header	0	00	Header	00	00000000
	1	01	Header	FF	11111111
	2	02	Header	FF	11111111
	3	03	Header	FF	11111111
	4	04	Header	FF	11111111
	5	05	Header	FF	11111111
	6	06	Header	FF	11111111
	7	07	Header	00	00000000
Vendor / Product	8	08	ID Manufacture Name LGD	30	00110000
	9	09	ID Manufacture Name	E4	11100100
	10	0A	ID Product Code 025Ah	5A	01011010
	11	0B	(Hex, LSB first)	02	00000010
	12	0C	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	00	00000000
	13	0D	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	00	00000000
	14	0E	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	00	00000000
	15	0F	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	00	00000000
	16	10	Week of Manufacture - Optional 00 weeks	00	00000000
	17	11	Year of Manufacture 2009 years	13	00010011
Display	18	12	EDID structure version # = 1	01	00000001
	19	13	EDID revision # = 4	04	00000100
	20	14	Video input Definition = Input is a Digital Video signal Interface , Colo Bit Depth : 6 Bits per Primary Color , Digital Video Interface Standard Supported: DisplayPort is supported	95	10010101
	21	15	Horizontal Screen Size (Rounded cm) = 37 cm	25	00100101
	22	16	Vertical Screen Size (Rounded cm) = 23 cm	17	00010111
Vendor / Product	23	17	Display Transfer Characteristic (Gamma) = (gamma*100)-100 = Example:(2.2*100)-100=120 = 2.2 Gamma	78	01111000
	24	18	Feature Support [Display Power Management(DPM) : Standby Mode is not supported, Suspend Mode is not supported, Active Off = Very Low Power is not supported ,Supported Color Encoding Formats : RGB 4:4:4 ,Other Feature Support Flags : No_sRGB, Preferred Timing Mode, No Display is continuous frequency (Multi-mode Base EDID and Extension Block).]	02	00000010
	25	19	Red/Green Low Bits (RxRy/GxGy)	44	01000100
	26	1A	Blue/White Low Bits (BxBy/WxWy)	75	01110101
	27	1B	Red X Rx = 0.610	9C	10011100
	28	1C	Red Y Ry = 0.348	59	01011001
	29	1D	Green X Gx = 0.329	54	01010100
	30	1E	Green Y Gy = 0.586	96	10010110
	31	1F	Blue X Bx = 0.153	27	00100111
	32	20	Blue Y By = 0.140	23	00100011
Established	33	21	White X Wx = 0.313	50	01010000
	34	22	White Y Wy = 0.329	54	01010100
	35	23	Established timing 1 (Optional_00h if not used)	00	00000000
	36	24	Established timing 2 (Optional_00h if not used)	00	00000000
	37	25	Manufacturer's timings (Optional_00h if not used)	00	00000000
Standard Timing ID	38	26	Standard timing ID1 (Optional_01h if not used)	01	00000001
	39	27	Standard timing ID1 (Optional_01h if not used)	01	00000001
	40	28	Standard timing ID2 (Optional_01h if not used)	01	00000001
	41	29	Standard timing ID2 (Optional_01h if not used)	01	00000001
	42	2A	Standard timing ID3 (Optional_01h if not used)	01	00000001
	43	2B	Standard timing ID3 (Optional_01h if not used)	01	00000001
	44	2C	Standard timing ID4 (Optional_01h if not used)	01	00000001
	45	2D	Standard timing ID4 (Optional_01h if not used)	01	00000001
	46	2E	Standard timing ID5 (Optional_01h if not used)	01	00000001
	47	2F	Standard timing ID5 (Optional_01h if not used)	01	00000001
	48	30	Standard timing ID6 (Optional_01h if not used)	01	00000001
	49	31	Standard timing ID6 (Optional_01h if not used)	01	00000001
	50	32	Standard timing ID7 (Optional_01h if not used)	01	00000001
	51	33	Standard timing ID7 (Optional_01h if not used)	01	00000001
	52	34	Standard timing ID8 (Optional_01h if not used)	01	00000001
	53	35	Standard timing ID8 (Optional_01h if not used)	01	00000001

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APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 2/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Timing Descriptor #1	54	36	Pixel Clock/10,000 (LSB) 142.8 MHz @ 58.8Hz	C8	11001000
	55	37	Pixel Clock/10,000 (MSB)	37	00110111
	56	38	Horizontal Active (HA) (lower 8 bits) 1920 Pixels	80	10000000
	57	39	Horizontal Blanking (HB) (lower 8 bits) 80 Pixels	50	01010000
	58	3A	Horizontal Active / Horizontal Blanking(HA HB) (upper 4:4bits)	70	01110000
	59	3B	Vertical Active (VA) 1200 Lines	B0	10110000
	60	3C	Vertical Blanking (VB) (DE Blanking typ.for DE only panels) 15 Lines	0F	00001111
	61	3D	Vertical Active / Vertical Blanking (VA VB) (upper 4:4bits)	40	01000000
	62	3E	Horizontal Front Porch in pixels (HF) (lower 8 bits) 14 Pixels	0E	00001110
	63	3F	Horizontal Sync Pulse Width in pixels (HS) (lower 8 bits) 32 Pixels	20	00100000
	64	40	Vertical Front Porch in lines (VF) (lower 4 bits) : Vertical Sync Pluse Width in lines (VS) (lower 4 bits) 3 Lines : 6 Lines	36	00110110
	65	41	Horizontal Front Porch/ Sync Pulse width/ Vertical Front Porch/ Sync Pulse width (upper 2bits)	00	00000000
	66	42	Horizontal Vedio Image Size (mm) (lower 8 bits) 370 mm	72	01110010
	67	43	Vertical Vedio Image Size (mm) (lower 8 bits) 230 mm	E6	11100110
	68	44	Horizontal Image Size / Vertical Image Size (upper 4 bits)	10	00010000
	69	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000
	70	46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
	71	47	Non-Interlace, Normal display, no stereo, Digital Separate [vsync_NEG, Hsync_POS (outside of v-sync)]	1A	00011010
	72	48	Pixel Clock/10,000 (LSB) 105 MHz @ 40.1Hz	3C	00111100
	73	49	Pixel Clock/10,000 (MSB)	28	00101000
Timing Descriptor #2	74	4A	Horizontal Active (HA) (lower 8 bits) 1920 Pixels	80	10000000
	75	4B	Horizontal Blanking (HB) (lower 8 bits) 160 Pixels	A0	10100000
	76	4C	Horizontal Active / Horizontal Blanking(HA HB) (upper 4:4bits)	70	01110000
	77	4D	Vertical Active (VA) 1200 Lines	B0	10110000
	78	4E	Vertical Blanking (VB) (DE Blanking typ.for DE only panels) 35 Lines	23	00100011
	79	4F	Vertical Active / Vertical Blanking (VA VB) (upper 4:4bits)	40	01000000
	80	50	Horizontal Front Porch in pixels (HF) (lower 8 bits) 48 Pixels	30	00110000
	81	51	Horizontal Sync Pulse Width in pixels (HS) (lower 8 bits) 32 Pixels	20	00100000
	82	52	Vertical Front Porch in lines (VF) (lower 4 bits) : Vertical Sync Pluse Width in lines (VS) (lower 4 bits) 3 Lines : 6 Lines	36	00110110
	83	53	Horizontal Front Porch/ Sync Pulse width/ Vertical Front Porch/ Sync Pulse width (upper 2bits)	00	00000000
	84	54	Horizontal Vedio Image Size (mm) (lower 8 bits) 370 mm	72	01110010
	85	55	Vertical Vedio Image Size (mm) (lower 8 bits) 230 mm	E6	11100110
	86	56	Horizontal Image Size / Vertical Image Size (upper 4 bits)	10	00010000
	87	57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000
	88	58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
	89	59	Non-Interlace, Normal display, no stereo, Digital Separate [vsync_NEG, Hsync_POS (outside of v-sync)]	1A	00011010
	90	5A	Flag	00	00000000
Timing Descriptor #3	91	5B	Flag	00	00000000
	92	5C	Flag	00	00000000
	93	5D	Data Type Tag : Alphanumeric Data String (ASCII String)	FE	11111110
	94	5E	Flag	00	00000000
	95	5F	Dell P/N 1st Character = H	48	01001000
	96	60	Dell P/N 2nd Character = 0	30	00110000
	97	61	Dell P/N 3rd Character = 8	38	00111000
	98	62	Dell P/N 4th Character = 6	36	00110110
	99	63	Dell P/N 5th Character = R	52	01010010
	100	64	EDID Revision Build Name = MP(X-Build) , Revision # = A00	80	10000000
	101	65	Manufacturer P/N = 1	31	00110001
	102	66	Manufacturer P/N = 7	37	00110111
	103	67	Manufacturer P/N = 1	31	00110001
	104	68	Manufacturer P/N = W	57	01010111
	105	69	Manufacturer P/N = U	55	01010101
	106	6A	Manufacturer P/N = 7	37	00110111
	107	6B	Manufacturer P/N (If < 13 char, then terminate with ASC II code 0Ah,set remaining char = 20h)	0A	00001010

LP171WU7
Liquid Crystal Display

Product Specification

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 3/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Timing Descriptor #4	108	6C	Flag	00	00000000
	109	6D	Flag	00	00000000
	110	6E	Flag	00	00000000
	111	6F	Data Type Tag : Descriptor Defined by manufacturer	00	00000000
	112	70	Flag	00	00000000
	113	71	Color Management [No +2 FRC Support, True Color Depth : 6 bit]	00	00000000
	114	72	Panel Type [WLED] , Configuration [Single light bar] , Number Lamp or LED Light Bar [one]	41	01000001
	115	73	Frame Rate Details [Minimum Frame Rate : 40Hz, Maximum Frame Rate : 65Hz , Tcon provides native Intel DRRS / sDRRS support]	31	00110001
	116	74	Controller Interface and Maximum Luminance [SMBUS type, 300 nit]	1E	00011110
	117	75	Front Surface / Polarizer [Anti-Glare, No Transflective] , Pixel Structure [RGB v-stripe]	00	00000000
	118	76	Multi-Media Features [Color Management : NTSC, Dynamic Backlight Control : No]	00	00000000
	119	77	Multi-Media Features [Motion Blur : No support , Active Gamma Control : No support]	00	00000000
	120	78	Special Features [Wireless Enhancement Hardware : No support , In-Cell Scanner : No support]	00	00000000
	121	79	Special Features [Number of LVDS channels or eDP lanes : two , Overdrive : yes ,Interface : LVDS , In-Cell Touch Support : No]	06	00000110
	122	7A	Special Features [BIST Support : yes , Electronic Privacy : No electronic privacy hardware support , 3-D Support : No]	01	00000001
	123	7B	(If<13 char--> 0Ah, then terminate with ASC II code 0Ah,set remaining char = 20h)	0A	00001010
	124	7C	(If<13 char--> 0Ah, then terminate with ASC II code 0Ah,set remaining char = 20h)	20	00100000
	125	7D	(If<13 char--> 0Ah, then terminate with ASC II code 0Ah,set remaining char = 20h)	20	00100000
Checksum	126	7E	Extension flag (# of optional 128 panel ID extension block to follow, Typ = 0)	00	00000000
	127	7F	Check Sum (The 1-byte sum of all 128 bytes in this panel ID block shall = 0)	4D	01001101