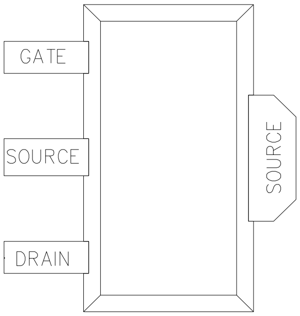
Filtronic

LP3000SOT89

LOW NOISE, HIGH LINEARITY PACKAGED PHEMT

- FEATURES
  - ♦ 29 dBm Output Power at 1-dB Compression at 1.8 GHz
  - ♦ 15 dB Power Gain at 1.8 GHz
  - ♦ 1.3 dB Noise Figure
  - ♦ 46 dBm Output IP3 at 1.8 GHz
  - ♦ 55% Power-Added Efficiency



- DESCRIPTION AND APPLICATIONS

The LP3000SOT89 is a packaged Aluminum Gallium Arsenide / Indium Gallium Arsenide (AlGaAs/InGaAs) pseudomorphic High Electron Mobility Transistor (pHEMT). It utilizes a 0.25 µm x 3000 µm Schottky barrier gate, defined by electron-beam photolithography. The recessed “mushroom” gate structure minimizes parasitic gate-source and gate resistance. The epitaxial structure and processing have been optimized for reliable high-power applications. The LP3000 also features Si3N4 passivation and is available in die form or in other packages.

Typical applications include PCS/Cellular low-voltage, high-efficiency amplifiers.

- ELECTRICAL SPECIFICATIONS @ $T_{Ambient}$ = 25°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Saturated Drain-Source Current LP3000SOT89-1	I_{DSS}	V_{DS} = 2 V; V_{GS} = 0 V	800	860	924	mA
LP3000SOT89-2			925	975	1024	mA
LP3000SOT89-3			1025	1060	1100	mA
Power at 1-dB Compression	P-1dB	V_{DS} = 5 V; I_{DS} = 50% I_{DSS}	28	29		dBm
Power Gain at 1-dB Compression	G-1dB	V_{DS} = 5 V; I_{DS} = 50% I_{DSS}	14	15		dB
Power-Added Efficiency	PAE	V_{DS} = 5 V; I_{DS} = 50% I_{DSS}; P_{IN} = 15 dBm		55		%
Noise Figure	NF	V_{DS} = 5 V; I_{DS} = 50% I_{DSS}		1.3		dB
Output Third-Order Intercept Point	IP3	V_{DS} = 5V; I_{DS} = 50% I_{DSS}; P_{IN} = 3 dBm		46		dBm
Maximum Drain-Source Current	I_{MAX}	V_{DS} = 2 V; V_{GS} = 1 V		1700		mA
Transconductance	G_M	V_{DS} = 2 V; V_{GS} = 0 V	700	900		mS
Gate-Source Leakage Current	I_{GSO}	V_{GS} = -5 V		15	200	µA
Pinch-Off Voltage	V_P	V_{DS} = 2 V; I_{DS} = 15 mA	-0.25	-1.2	-2.0	V
Gate-Source Breakdown Voltage Magnitude	$\lvert V_{BDGS} \rvert$	I_{GS} = 15 mA	-10	-12		V
Gate-Drain Breakdown Voltage Magnitude	$\lvert V_{BDGD} \rvert$	I_{GD} = 15 mA	-10	-13		V

frequency=1.8 GHz

• ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	V_{DS}	$T_{Ambient} = 22 \pm 3$ °C		7	V
Gate-Source Voltage	V_{GS}	$T_{Ambient} = 22 \pm 3$ °C		-4	V
Drain-Source Current	I_{DS}	$T_{Ambient} = 22 \pm 3$ °C		I_{DSS}	mA
Gate Current	I_G	$T_{Ambient} = 22 \pm 3$ °C		30	mA
RF Input Power	P_{IN}	$T_{Ambient} = 22 \pm 3$ °C		1	W
Channel Operating Temperature	T_{CH}	$T_{Ambient} = 22 \pm 3$ °C		175	ºC
Storage Temperature	T_{STG}	—	-65	175	ºC
Total Power Dissipation	P_{TOT}	$T_{Ambient} = 22 \pm 3$ °C		3.75	W

Notes:

- Operating conditions that exceed the Absolute Maximum Ratings could result in permanent damage to the device.
- Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$, where
  P_{DC}: DC Bias Power
  P_{IN}: RF Input Power
  P_{OUT}: RF Output Power
- Absolute Maximum Power Dissipation to be de-rated as follows above 25°C:
  P_{TOT}= 3.75W – (0.025W/°C) x T_{HS}
  where T_{PACK} = *source tab lead temperature..*
- This PHEMT is susceptible to damage from Electrostatic Discharge. Proper precautions should be used when handling these devices.

• OPTIMUM POWER OUTPUT MATCHING

	Load State	
Frequency (GHz)	Magnitude	Phase
1.8	0.77	-154°
2.2	0.68	-150°
2.5	0.59	-143°

• HANDLING PRECAUTIONS

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A (0-500 V). Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

• APPLICATIONS NOTES & DESIGN DATA

Applications Notes are available from your local Filtronic Sales Representative or directly from the factory. Complete design data, including S-parameters, noise data, and large-signal models are available on the Filtronic web site.

- PACKAGE OUTLINE

(dimensions in inches)