National Semiconductor

December 2006

LP38853
3A Fast-Response High-Accuracy Adjustable LDO Linear Regulator with Enable and Soft-Start

General Description

The LP38853-ADJ is a high current, fast response regulator which can maintain output voltage regulation with extremely low input to output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: V_{BIAS} provides voltage to drive the gate of the N-MOS power transistor, while V_{IN} is the input voltage which supplies power to the load. The use of an external bias rail allows the part to operate from ultra low V_{IN} voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of this device makes it suitable for use in powering DSP, Microcontroller Core voltages and Switch Mode Power Supply post regulators. The part is available in PSOP 8–pin, TO-220 7–pin, and TO-263 7-pin packages.

Dropout Voltage: 240 mV (typical) at 3A load current.

Low Ground Pin Current: 10 mA (typical) at 3A load current.

Soft-Start: Programmable Soft-Start time.

Precision ADJ Voltage: ±1.5% for T_J = 25°C, and ±2.0% for 0°C ≤ T_J ≤ +125°C, across all line and load conditions

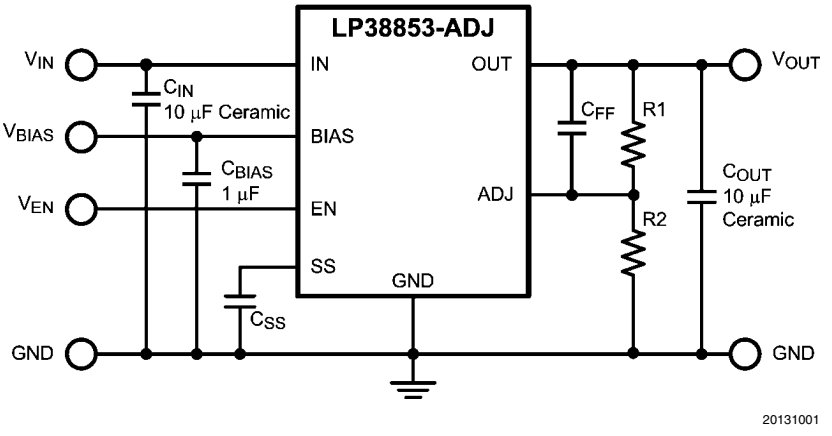
Features

- Adjustable V_{OUT} range of 0.80V to 1.8V
- Wide V_{BIAS} Supply operating range of 3.0V to 5.5V
- Stable with 10µF Ceramic capacitors
- Dropout voltage of 240 mV (typical) at 3A load current
- Precision V_{ADJ} across all line and load conditions:
  - — ±1.5% V_{ADJ} for T_J = 25°C
  - — ±2.0% V_{ADJ} for 0°C ≤ T_J ≤ +125°C
  - — ±3.0% V_{ADJ} for -40°C ≤ T_J ≤ +125°C
- Over-Temperature and Over-Current protection
- Available in 8 lead PSOP, 7 lead TO-220 and 7 lead TO-263 packages
- –40°C to +125°C Operating Junction Temperature Range

Applications

- ASIC Power Supplies in:
  - Desktops, Notebooks, and Graphics Cards, Servers
  - Gaming Set Top Boxes, Printers and Copiers
- Server Core and I/O Supplies
- DSP and FPGA Power Supplies
- SMPS Post-Regulator

Typical Application Circuit



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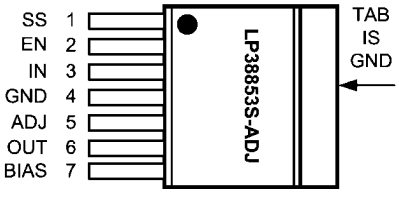
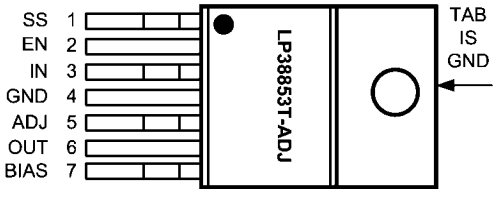
Ordering Information

V_{OUT}	Order Number	Package Type	Package Drawing	Supplied As
ADJ	LP38853S-ADJ	TO263-7	TS7B	Rail of 45
	LP38853SX-ADJ	TO263-7	TS7B	Tape and Reel of 500
	LP38853T-ADJ	TO220-7	TA07B	Rail of 45
	LP38853MR-ADJ	PSOP-8	MR08B	Rail of 95
	LP38853MRX-ADJ	PSOP-8	MR08B	Tape and Reel of 2500

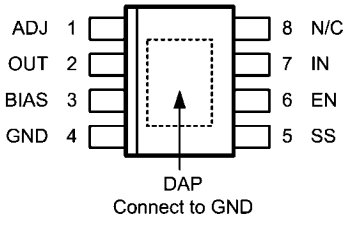
Connection Diagrams



TO263-7, Top View



TO220-7, Top View



PSOP-8, Top View

Pin Descriptions

TO220-7 Pin #	TO263-7 Pin #	PSOP-8 Pin #	Pin Symbol	Pin Description
1	1	5	SS	Soft-Start capacitor connection. Used to control the rise time of V_{OUT} at turn-on.
2	2	6	EN	Device Enable, High = On, Low = Off.
3	3	7	IN	The unregulated voltage input
4	4	4	GND	Ground
5	5	1	ADJ	The feedback connection to set the output voltage
6	6	2	OUT	The regulated output voltage
7	7	3	BIAS	The supply for the internal control and reference circuitry.
-	-	8	N/C	No internal connection
TAB	TAB	-	TAB	The TO220 and TO263 TAB is a thermal and electrical connection that is physically attached to the backside of the die, and used as a thermal heat-sink connection. See the Application Information section for details.
-	-	DAP	DAP	The PSOP DAP is a thermal connection only that is physically attached to the backside of the die, and used as a thermal heat-sink connection. See the Application Information section for details.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Soldering, 5 seconds	260°C
ESD Rating	
Human Body Model (Note 2)	±2 kV
Power Dissipation (Note 3)	Internally Limited
V_{IN} Supply Voltage (Survival)	−0.3V to +6.0V
V_{BIAS} Supply Voltage (Survival)	−0.3V to +6.0V
V_{SS} SoftStart Voltage (Survival)	−0.3V to +6.0V
V_{OUT} Voltage (Survival)	−0.3V to +6.0V
I_{OUT} Current (Survival)	Internally Limited
Junction Temperature	−40°C to +150°C

Operating Ratings (Note 1)

V_{IN} Supply Voltage	$(V_{OUT} + V_{DO})$ to V_{BIAS}
V_{BIAS} Supply Voltage	
$0.8V \le V_{OUT} \le 1.2V$	3.0V to 5.5V
$1.2V < V_{OUT} \le 1.8V$	4.5V to 5.5V
V_{EN} Voltage	0.0V to V_{BIAS}
I_{OUT}	0 mA to 3.0A
Junction Temperature Range (Note 3)	−40°C to +125°C

Electrical Characteristics

Unless otherwise specified: V_{OUT} = 0.80V, $V_{IN} = V_{OUT(NOM)}$ + 1V, V_{BIAS} = 3.0V, $V_{EN} = V_{BIAS}$, I_{OUT} = 10 mA, $C_{IN} = C_{OUT}$ = 10 µF, C_{BIAS} = 1 µF, C_{SS} = open. Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
V_{ADJ}	V_{ADJ} Accuracy	$V_{OUT(NOM)}$+1V ≤ V_{IN} ≤ V_{BIAS} ≤ 4.5V, See (Note 7) 3.0V ≤ V_{BIAS} ≤ 5.5V, 10 mA ≤ I_{OUT} ≤ 3A	492.5 **485.0**	500.	507.5 **515.0**	mV
		$V_{OUT(NOM)}$+1V ≤ V_{IN} ≤ V_{BIAS} ≤ 4.5V, See (Note 7) 3.0V ≤ V_{BIAS} ≤ 5.5V, 10 mA ≤ I_{OUT} ≤ 3.0A, 0°C ≤ T_J ≤ +125°C	490.0	500.	510.0	
V_{OUT}	V_{OUT} Range	3.0V ≤ V_{BIAS} ≤ 5.5V	0.80		1.20	V
		4.5V ≤ V_{BIAS} ≤ 5.5V	0.80		1.80	
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation, V_{IN} (Note 4)	$V_{OUT(NOM)}$+1V ≤ V_{IN} ≤ V_{BIAS}	-	0.04	-	%/V
$\Delta V_{OUT}/\Delta V_{BIAS}$	Line Regulation, V_{BIAS} (Note 4)	3.0V ≤ V_{BIAS} ≤ 5.5V	-	0.10	-	%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Output Voltage Load Regulation (Note 5)	10 mA ≤ I_{OUT} ≤ 3.0A	-	0.2	-	%/A
V_{DO}	Dropout Voltage (Note 6)	I_{OUT} = 3.0A	-	240	300 **450**	mV
$I_{GND(IN)}$	Quiescent Current Drawn from V_{IN} Supply	V_{OUT} = 0.80V V_{BIAS} = 3.0V 10 mA ≤ I_{OUT} ≤ 3.0A	-	7.0	8.5 **9.0**	mA
		V_{EN} ≤ 0.5V		1	10 **300**	µA
$I_{GND(BIAS)}$	Quiescent Current Drawn from V_{BIAS} Supply	10 mA ≤ I_{OUT} ≤ 3.0A	-	3.0	3.8 **4.5**	mA
		V_{EN} ≤ 0.5V		100	170 **200**	µA
UVLO	Under-Voltage Lock-Out Threshold	V_{BIAS} rising until device is functional	2.20 **2.00**	2.45	2.70 **2.90**	V
$UVLO_{(HYS)}$	Under-Voltage Lock-Out Hysteresis	V_{BIAS} falling from UVLO threshold until device is non-functional	60 **50**	150	300 **350**	mV
I_{SC}	Output Short-Circuit Current	$V_{IN} = V_{OUT(NOM)}$ + 1V, V_{BIAS} = 3.0V, V_{OUT} = 0.0V	-	5.8	-	A

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
Soft-Start						
r_{SS}	Soft-Start internal resistance		11.0	13.5	16.0	kΩ
t_{SS}	Soft-Start time $t_{SS} = C_{SS} \times r_{SS} \times 5$	C_{SS} = 10 nF	-	675	-	µs
Enable						
I_{EN}	ENABLE pin Current	$V_{EN} = V_{BIAS}$	-	0.01	-	µA
		V_{EN} = 0.0V, V_{BIAS} = 5.5V	-19 **-13**	-30	-40 **-51**	
$V_{EN(ON)}$	Enable Voltage Threshold	V_{EN} rising until Output = ON	1.00 **0.90**	1.25	1.50 **1.55**	V
$V_{EN(HYS)}$	Enable Voltage Hysteresis	V_{EN} falling from $V_{EN(ON)}$ until Output = OFF	50 **30**	100	150 **200**	mV
t_{OFF}	Turn-OFF Delay Time	R_{LOAD} x C_{OUT} << t_{OFF}	-	20	-	µs
t_{ON}	Turn-ON Delay Time	R_{LOAD} x C_{OUT} << t_{ON}	-	15	-	
AC Parameters						
PSRR (V_{IN})	Ripple Rejection for V_{IN} Input Voltage	$V_{IN} = V_{OUT(NOM)}$ + 1V, f = 120 Hz	-	80	-	dB
		$V_{IN} = V_{OUT(NOM)}$ + 1V, f = 1 kHz	-	70	-	
PSRR (V_{BIAS})	Ripple Rejection for V_{BIAS} Voltage	$V_{BIAS} = V_{OUT(NOM)}$ + 3V, f = 120 Hz	-	58	-	
		$V_{BIAS} = V_{OUT(NOM)}$ + 3V, f = 1 kHz	-	58	-	
e_n	Output Noise Density	f = 120 Hz	-	1	-	µV/√Hz
	Output Noise Voltage	BW = 10 Hz – 100 kHz	-	150	-	μV_{RMS}
		BW = 300 Hz – 300 kHz	-	90	-	
Thermal Parameters						
T_{SD}	Thermal Shutdown Junction Temperature		-	160	-	°C
$T_{SD(HYS)}$	Thermal Shutdown Hysteresis		-	10	-	
θ_{J-A}	Thermal Resistance, Junction to Ambient(Note 3)	TO220-7	-	60	-	°C/W
		TO263-7	-	60	-	
		PSOP-8	-	168	-	
θ_{J-C}	Thermal Resistance, Junction to Case(Note 3)	TO220-7	-	3	-	
		TO263-7	-	3	-	
		PSOP-8	-	11	-	

Note 1: Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and conditions, see the Electrical Characteristics.

Note 2: The human body model is a 100 pF capacitor discharged through a 1.5k resistor into each pin. Test method is per JESD22-A114.

Note 3: Device power dissipation must be de-rated based on device power dissipation (P_D), ambient temperature (T_A), and package junction to ambient thermal resistance (θ_{JA}). Additional heat-sinking may be required to ensure that the device junction temperature (T_J) does not exceed the maximum operating rating. See the Application Information section for details.

Note 4: Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.

Note 5: Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.

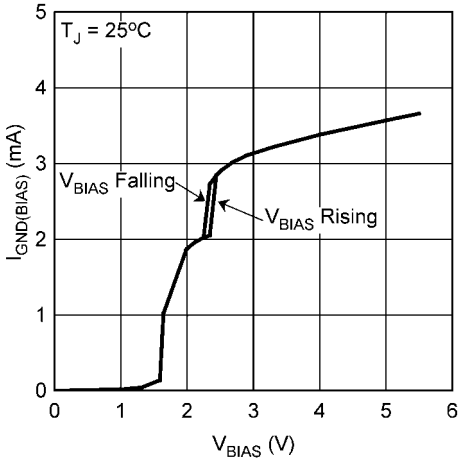
Note 6: Dropout voltage is defined as the input to output voltage differential (V_{IN} - V_{OUT}) where the input voltage is low enough to cause the output voltage to drop 2% from the nominal value.

Note 7: V_{IN} cannot exceed either V_{BIAS} or 4.5V, whichever value is lower.

Typical Performance Characteristics

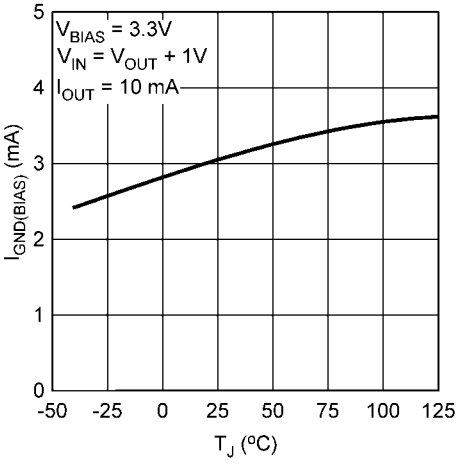
Refer to the *Typical Application Circuit*. Unless otherwise specified: T_J = 25°C, R1 = 1.40 kΩ, R2 = 1.00 kΩ, C_{FF}= 0.01 µF, $V_{IN} = V_{OUT(NOM)}$ + 1V, V_{BIAS} = 3.0V, I_{OUT} = 10 mA, C_{IN} = 10 µF Ceramic, C_{OUT} = 10 µF Ceramic, C_{BIAS} = 1 µF Ceramic, , C_{SS} = Open.

V_{BIAS} Ground Pin Current ($I_{GND(BIAS)}$) vs V_{BIAS}



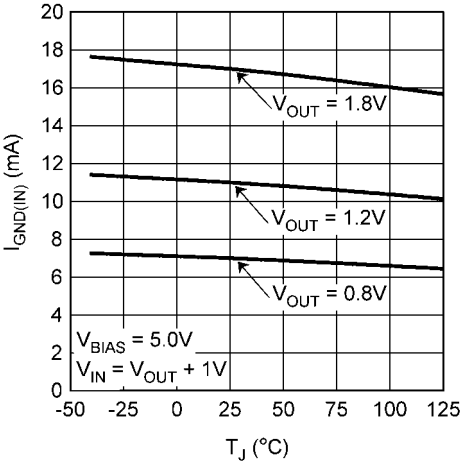
20131087

V_{BIAS} Ground Pin Current ($I_{GND(BIAS)}$) vs Temperature



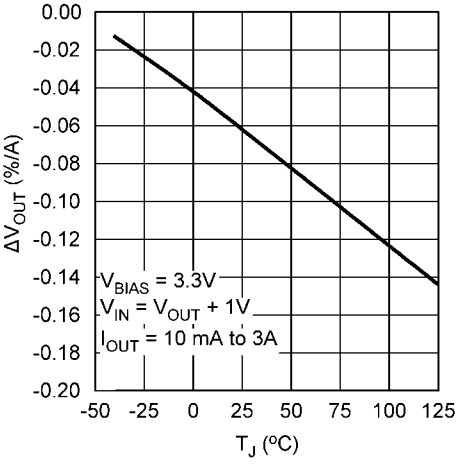
20131061

V_{IN} Ground Pin Current vs Temperature



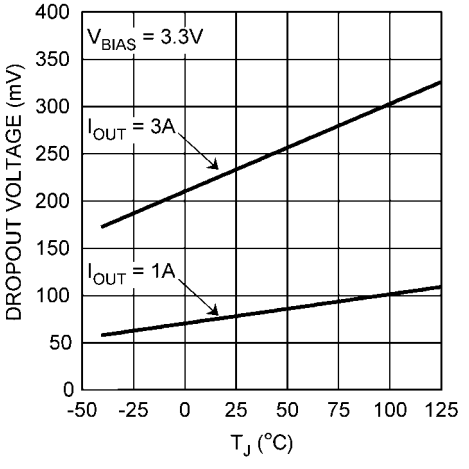
20131062

Load Regulation vs Temperature



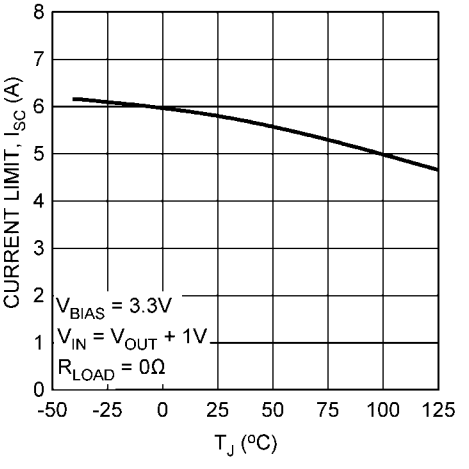
20131063

Dropout Voltage (V_{DO}) vs Temperature



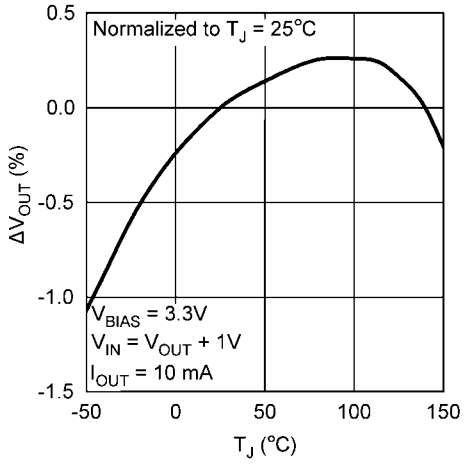
20131065

Output Current Limit (I_{SC}) vs Temperature



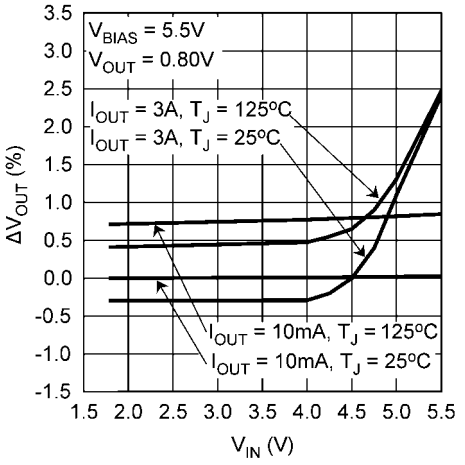
20131066

V_{OUT} vs Temperature



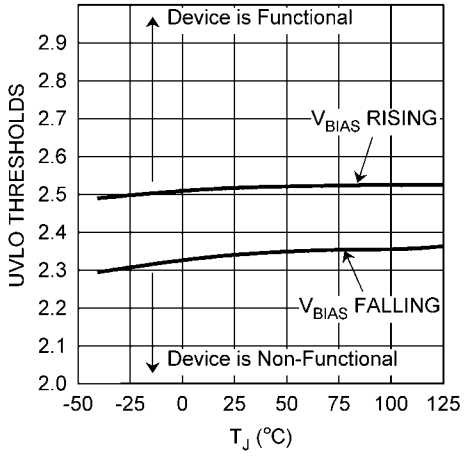
20131067

V_{OUT} vs V_{IN}



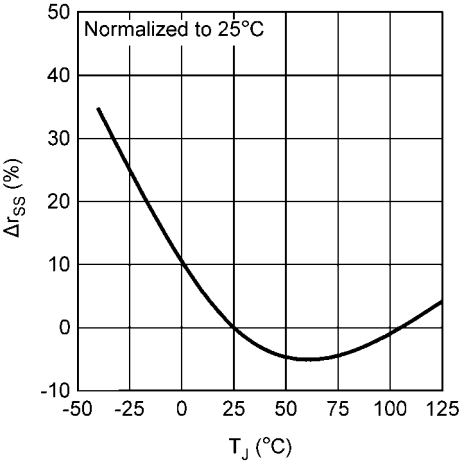
20131072

UVLO Thresholds vs Temperature



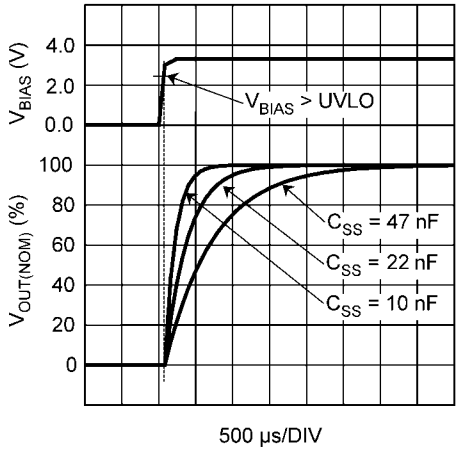
20131068

Soft-Start r_{SS} Variation vs Temperature



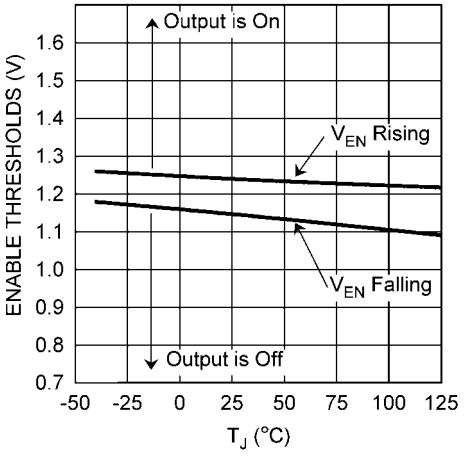
20131075

V_{OUT} vs C_{SS}, 10 nF to 47 nF



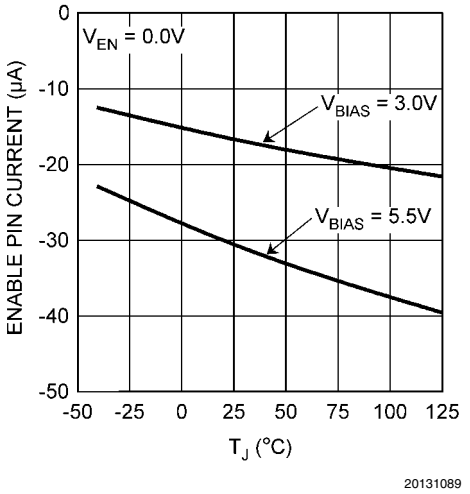
20131076

Enable Thresholds (V_{EN}) vs Temperature



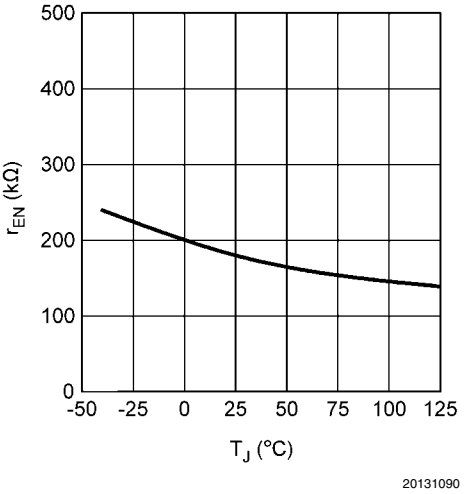
20131088

Enable Pull-Down Current (I_{EN}) vs Temperature



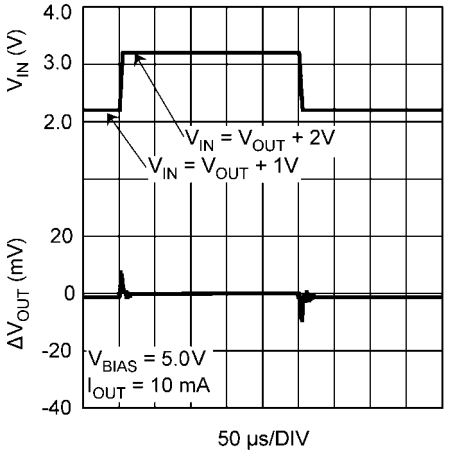
20131089

Enable Pull-Up Resistor (r_{EN}) vs Temperature



20131090

V_{IN} Line Transient Response



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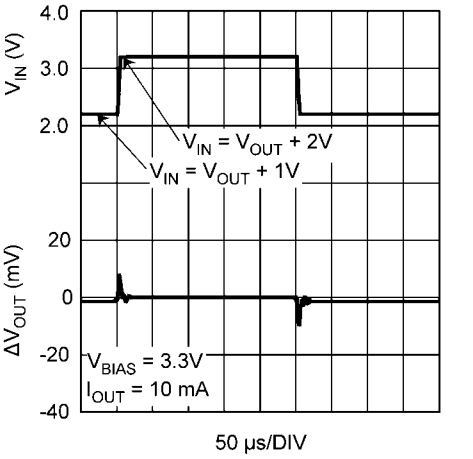
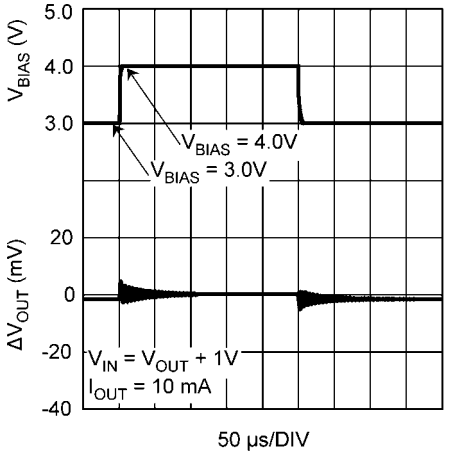
V_{IN} Line Transient Response



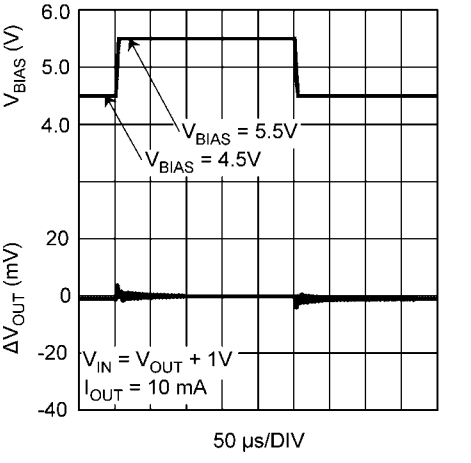
20131078

V_{BIAS} Line Transient Response



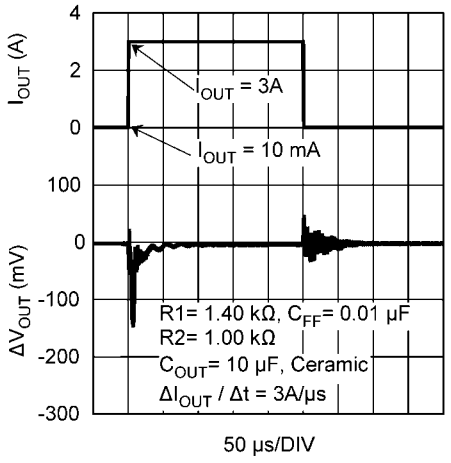
20131079

V_{BIAS} Line Transient Response



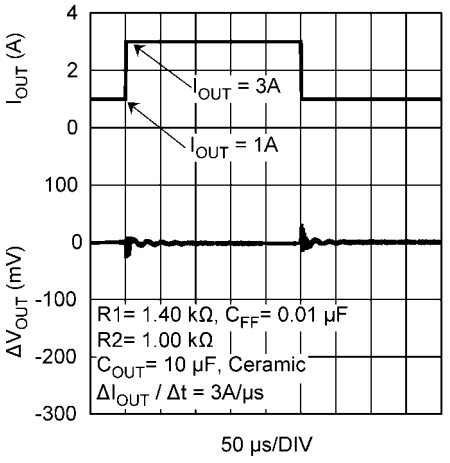
20131080

Load Transient Response, C_{OUT} = 10 µF Ceramic



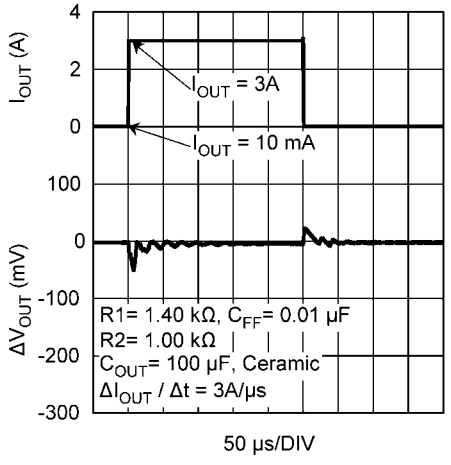
20131081

Load Transient Response, C_{OUT} = 10 µF Ceramic



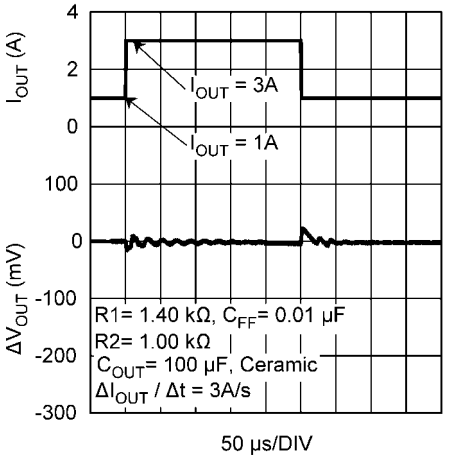
20131082

Load Transient Response, C_{OUT} = 100 µF Ceramic



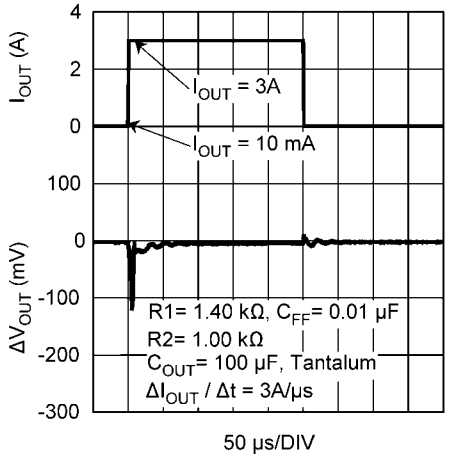
20131083

Load Transient Response, C_{OUT} = 100 µF Ceramic



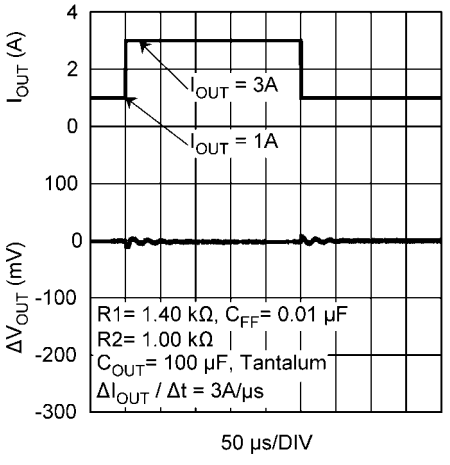
20131084

Load Transient Response, C_{OUT} = 100 µF Tantalum



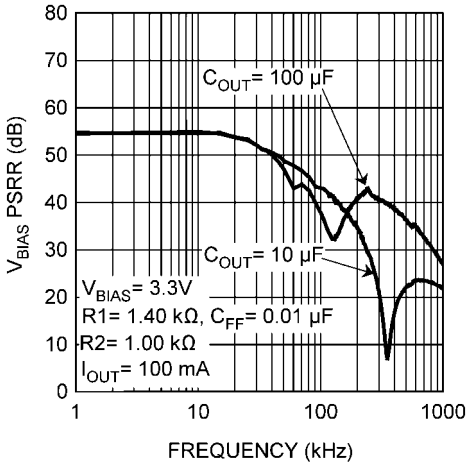
20131085

Load Transient Response, C_{OUT} = 100 µF Tantalum



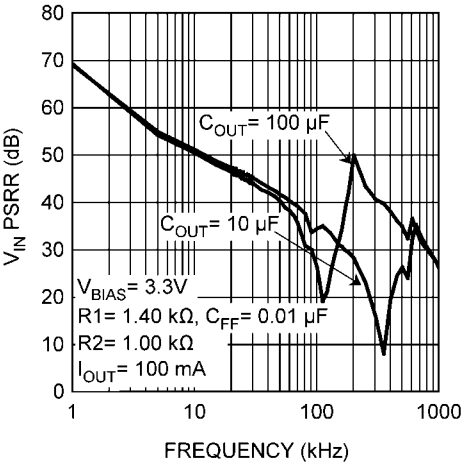
20131086

V_{BIAS} PSRR



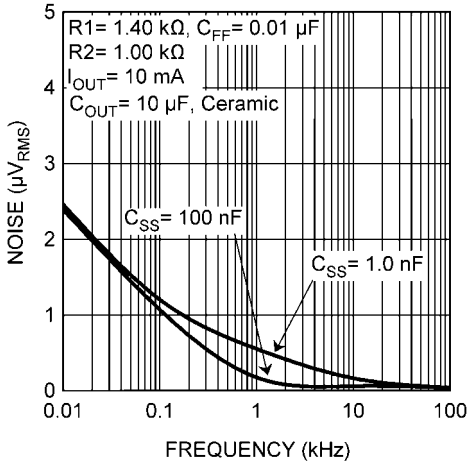
20131070

V_{IN} PSRR



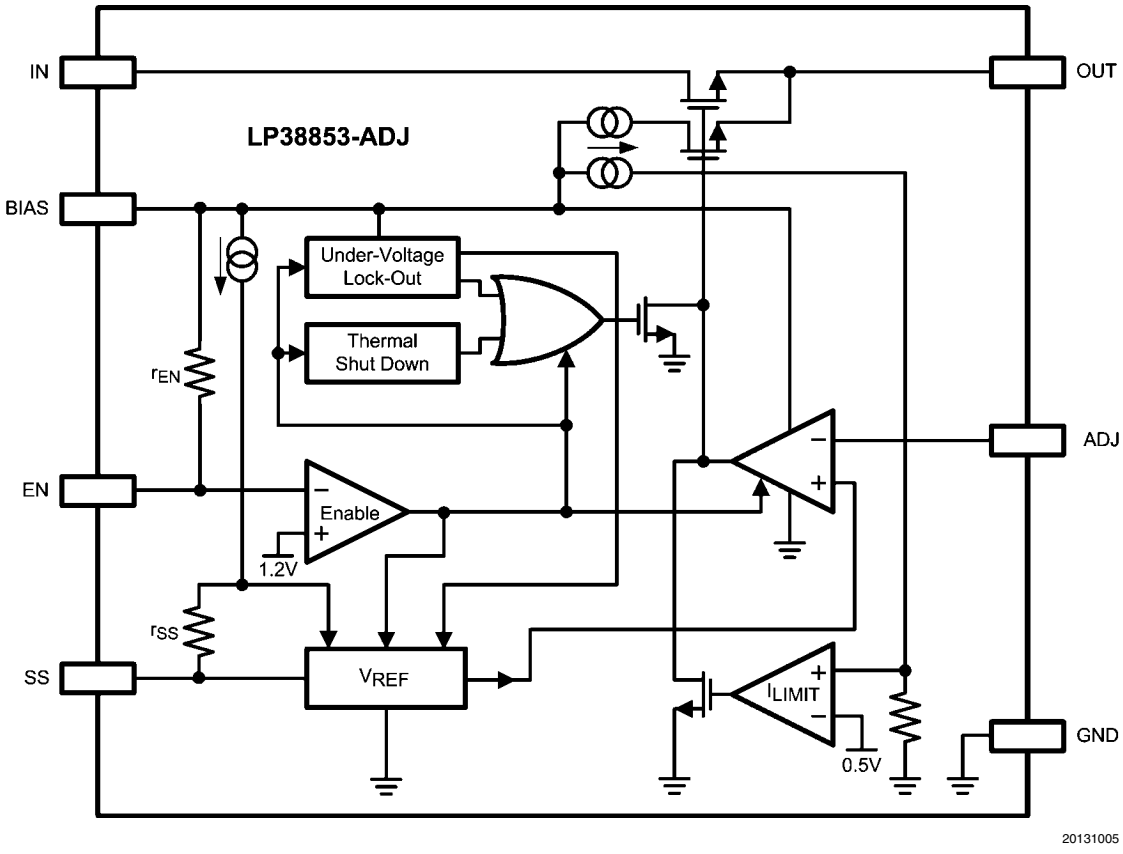
20131071

Output Noise



20131069

Block Diagram



Application Information

EXTERNAL CAPACITORS

To assure regulator stability, input and output capacitors are required as shown in the Typical Application Circuit.

Output Capacitor

A minimum output capacitance of 10 µF, ceramic, is required for stability. The amount of output capacitance can be increased without limit. The output capacitor must be located less than 1 cm from the output pin of the IC and returned to the device ground pin with a clean analog ground.

Only high quality ceramic types such as X5R or X7R should be used, as the Z5U and Y5F types do not provide sufficient capacitance over temperature.

Tantalum capacitors will also provide stable operation across the entire operating temperature range. However, the effects of ESR may provide variations in the output voltage during fast load transients. Using the minimum recommended 10 µF ceramic capacitor at the output will allow unlimited capacitance, Tantalum and/or Aluminum, to be added in parallel.

Input Capacitor

The input capacitor must be at least 10 µF, but can be increased without limit. It's purpose is to provide a low source impedance for the regulator input. A ceramic capacitor, X5R or X7R, is recommended.

Tantalum capacitors may also be used at the input pin. There is no specific ESR limitation on the input capacitor (the lower, the better).

Aluminum electrolytic capacitors can be used, but are not recommended as their ESR increases very quickly at cold temperatures. They are not recommended for any application where the ambient temperature falls below 0°C.

Bias Capacitor

The capacitor on the bias pin must be at least 1 µF, and can be any good quality capacitor (ceramic is recommended).

Feed Forward Capacitor, C_{FF} (Refer to the Typical Application Circuit)

When using a ceramic capacitor for C_{OUT}, the typical ESR value will be too small to provide any meaningful positive phase compensation, F_Z, to offset the internal negative phase shifts in the gain loop.

$$F_Z = (1 / (2 \times \pi \times C_{OUT} \times ESR)) \quad (1)$$

A capacitor placed across the gain resistor R1 will provide additional phase margin to improve load transient response of the device. This capacitor, C_{FF}, in parallel with R1, will form a zero in the loop response given by the formula:

$$F_Z = (1 / (2 \times \pi \times C_{FF} \times R1)) \quad (2)$$

For optimum load transient response select C_{FF} so the zero frequency, F_Z, falls between 10 kHz and 15 kHz.

$$(C_{FF} = (1 / (2 \times \pi \times R1 \times F_Z) \quad (3)$$

The phase lead provided by C_{FF} diminishes as the DC gain approaches unity, or V_{OUT} approaches V_{ADJ}. This is because C_{FF} also forms a pole with a frequency of:

$$F_P = (1 / (2 \times \pi \times C_{FF} \times (R1 \parallel R2))) \quad (4)$$

It's important to note that at higher output voltages, where R1 is much larger than R2, the pole and zero are far apart in frequency. At lower output voltages the frequency of the pole and the zero mover closer together. The phase lead provided from C_{FF} diminishes quickly as the output voltage is reduced, and has no effect when $V_{OUT} = V_{ADJ}$. For this reason, relying on this compensation technique alone is adequate only for higher output voltages. For the LP38853, the practical minimum V_{OUT} is 0.8V when a ceramic capacitor is used for C_{OUT}.

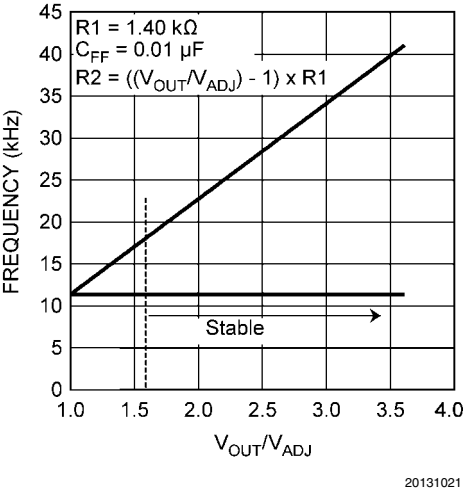


FIGURE 1. F_{ZERO} and F_{POLE} vs Gain

SETTING THE OUTPUT VOLTAGE (Refer to the Typical Application Circuit)

The output voltage is set using the external resistive divider R1 and R2. The output voltage is given by the formula:

$$V_{OUT} = V_{ADJ} \times \left(1 + \left(\frac{R1}{R2}\right)\right) \quad (5)$$

The resistors used for R1 and R2 should be high quality, tight tolerance, and with matching temperature coefficients. It is important to remember that, although the value of V_{ADJ} is guaranteed, the use of low quality resistors for R1 and R2 can easily produce a V_{OUT} value that is unacceptable.

It is recommended that the values selected for R1 and R2 are such that the parallel value is less than 10 kΩ. This is to prevent internal parasitic capacitances on the ADJ pin from interfering with the F_Z pole set by R1 and C_{FF}.

$$((R1 \times R2) / (R1 + R2)) \leq 10\ k\Omega \quad (6)$$

Table 1 lists some suggested, best fit, standard ±1% resistor values for R1 and R2, and a standard ±10% capacitor values for C_{FF}, for a range of V_{OUT} values. Other values of R1, R2, and C_{FF} are available that will give similar results.

TABLE 1.

V_{OUT}	R1	R2	C_{FF}	F_Z
0.8V	1.07 kΩ	1.78 kΩ	12 nF	12.4 kHz
0.9V	1.50 kΩ	1.87 kΩ	8.2 nF	12.9 kHz
1.0V	1.00 kΩ	1.00 kΩ	12 nF	13.3 kHz
1.1V	1.65 kΩ	1.37 kΩ	8.2 nF	11.8 kHz
1.2V	1.40 kΩ	1.00 kΩ	10 nF	11.4 kHz
1.3V	1.15 kΩ	715 Ω	12 nF	11.5 kHz
1.4V	1.07 kΩ	590 Ω	12 nF	12.4 kHz
1.5V	2.00 kΩ	1.00 kΩ	6.8 nF	11.7 kHz
1.6V	1.65 kΩ	750 Ω	8.2 nF	11.8 kHz
1.7V	2.55 kΩ	1.07 kΩ	5.6 nF	11.1 kHz
1.8V	2.94 kΩ	1.13 kΩ	4.7 nF	11.5 kHz

Please refer to Application Note AN-1378 for additional information on how resistor tolerances affect the calculated V_{OUT} value.

INPUT VOLTAGE

The input voltage (V_{IN}) is the high current external voltage rail that will be regulated down to a lower voltage, which is applied to the load. The input voltage must be at least $V_{OUT} + V_{DO}$, and no higher than whatever value is used for V_{BIAS}.

For applications where V_{BIAS} is higher than 4.5V, V_{IN} must be no greater than 4.5V, otherwise output voltage accuracy may be affected.

BIAS VOLTAGE

The bias voltage (V_{BIAS}) is a low current external voltage rail required to bias the control circuitry and provide gate drive for the N-FET pass transistor. When V_{OUT} is set to 1.20V, or less, V_{BIAS} may be anywhere in the operating range of 3.0V to 5.5V. If V_{OUT} is set higher than 1.20V , V_{BIAS} must be between 4.5V and 5.5V to ensure proper operation of the device.

UNDER VOLTAGE LOCKOUT

The bias voltage is monitored by a circuit which prevents the device from functioning when the bias voltage is below the Under-Voltage Lock-Out (UVLO) threshold of approximately 2.45V.

As the bias voltage rises above the UVLO threshold the device control circuitry becomes active. There is approximately 150 mV of hysteresis built into the UVLO threshold to provide noise immunity.

When the bias voltage is between the UVLO threshold and the Minimum Operating Rating value of 3.0V the device will be functional, but the operating parameters will not be within the guaranteed limits.

SUPPLY SEQUENCING

There is no requirement for the order that V_{IN} or V_{BIAS} are applied or removed.

One practical limitation is that the Soft-Start circuit starts charging C_{SS} when both V_{BIAS} rises above the UVLO threshold and the Enable pin is above the $V_{EN(ON)}$ threshold. If the application of V_{IN} is delayed beyond this point the benefits of Soft-Start will be compromised.

In any case, the output voltage cannot be guaranteed until both V_{IN} and V_{BIAS} are within the range of guaranteed operating values.

If used in a dual-supply system where the regulator output load is returned to a negative supply, the output pin must be diode clamped to ground. A Schottky diode is recommended for this diode clamp.

REVERSE VOLTAGE

A reverse voltage condition will exist when the voltage at the output pin is higher than the voltage at the input pin. Typically this will happen when V_{IN} is abruptly taken low and C_{OUT} continues to hold a sufficient charge such that the input to output voltage becomes reversed.

The NMOS pass element, by design, contains no body diode. This means that, as long as the gate of the pass element is not driven, there will not be any reverse current flow through the pass element during a reverse voltage event. The gate of the pass element is not driven when V_{BIAS} is below the UVLO threshold, or when the Enable pin is held low.

When V_{BIAS} is above the UVLO threshold, and the Enable pin is above the $V_{EN(ON)}$ threshold, the control circuitry is active and will attempt to regulate the output voltage. Since the input voltage is less than the output voltage the control circuit will drive the gate of the pass element to the full V_{BIAS} potential when the output voltage begins to fall. In this condition, reverse current will flow from the output pin to the input pin , limited only by the $R_{DS(ON)}$ of the pass element and the output to input voltage differential. Discharging an output capacitor up 1000 µF in this manner will not damage the device as the current will rapidly decay. However, continuous reverse current should be avoided.

SOFT-START

The LP38853 incorporates a Soft-Start function that reduces the start-up current surge into the output capacitor (C_{OUT}) by allowing V_{OUT} to rise slowly to the final value. This is accomplished by controlling V_{REF} at the SS pin. The soft-start timing capacitor (C_{SS}) is internally held to ground until both V_{BIAS} rises above the Under-Voltage Lock-Out threshold (ULVO) and the Enable pin is higher than the $V_{EN(ON)}$ threshold.

V_{REF} will rise at an RC rate defined by the internal resistance of the SS pin (r_{SS}), and the external capacitor connected to the SS pin. This allows the output voltage to rise in a controlled manner until steady-state regulation is achieved. Typically, five time constants are recommended to assure that the output voltage is sufficiently close to the final steady-state value. During the soft-start time the output current can rise to the built-in current limit.

$$\text{Soft-Start Time} = C_{SS} \times r_{SS} \times 5 \quad (7)$$

Since the V_{OUT} rise will be exponential, not linear, the in-rush current will peak during the first time constant (τ), and V_{OUT} will require four additional time constants (4τ) to reach the final value (5τ) .

After achieving normal operation, should either V_{BIAS} fall below the ULVO threshold, or the Enable pin fall below the $V_{EN(OFF)}$ threshold, the device output will be disabled and the Soft-Start capacitor (C_{SS}) discharge circuit will become active. The C_{SS} discharge circuit will remain active until V_{BIAS} falls to 500 mV (typical). When V_{BIAS} falls below 500 mV (typical), the C_{SS} discharge circuit will cease to function due to a lack of sufficient biasing to the control circuitry.

Since V_{REF} appears on the SS pin, any leakage through C_{SS} will cause V_{REF} to fall, and thus affect V_{OUT}. A leakage of 50 nA (about 10 MΩ) through C_{SS} will cause V_{OUT} to be approximately 0.1% lower than nominal, while a leakage of 500 nA (about 1 MΩ) will cause V_{OUT} to be approximately 1% lower than nominal. Typical ceramic capacitors will have a factor of

10X difference in leakage between 25°C and 85°C, so the maximum ambient temperature must be included in the capacitor selection process.

Typical C_{SS} values will be in the range of 1 nF to 100 nF, providing typical Soft-Start times in the range of 70 µs to 7 ms (5τ). Values less than 1 nF can be used, but the Soft-Start effect will be minimal. Values larger than 100 nF will provide soft-start, but may not be fully discharged if V_{BIAS} falls from the UVLVO threshold to less than 500 mV in less than 100 µs.

Figure 2 shows the relationship between the C_{OUT} value and a typical C_{SS} value.

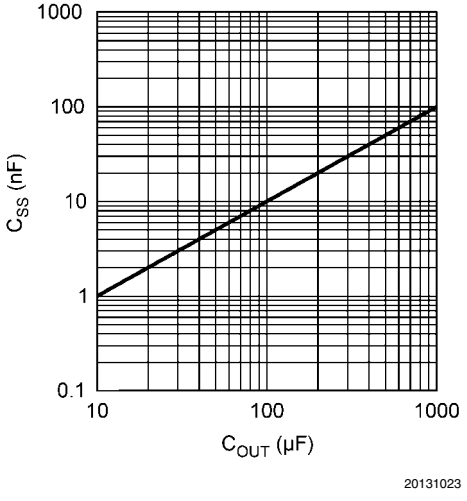


FIGURE 2. Typical C_{SS} vs C_{OUT} Values

The C_{SS} capacitor must be connected to a clean ground path back to the device ground pin. No components, other than C_{SS}, should be connected to the SS pin, as there could be adverse effects to V_{OUT}.

If the Soft-Start function is not needed the SS pin should be left open, although some minimal capacitance value is always recommended.

ENABLE OPERATION

The Enable pin (EN) provides a mechanism to enable, or disable, the regulator output stage. The Enable pin has an internal pull-up, through a typical 180 kΩ resistor, to V_{BIAS}.

If the Enable pin is actively driven, pulling the Enable pin above the V_{EN} threshold of 1.25V (typical) will turn the regulator output on, while pulling the Enable pin below the V_{EN} threshold will turn the regulator output off. There is approximately 100 mV of hysteresis built into the Enable threshold provide noise immunity.

If the Enable function is not needed this pin should be left open, or connected directly to V_{BIAS}. If the Enable pin is left open, stray capacitance on this pin must be minimized, otherwise the output turn-on will be delayed while the stray capacitance is charged through the internal resistance (r_{EN}).

POWER DISSIPATION AND HEAT-SINKING

Additional copper area for heat-sinking may be required depending on the maximum device dissipation (P_D) and the maximum anticipated ambient temperature (T_A) for the device. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.

The total power dissipation of the device is the sum of three different points of dissipation in the device.

The first part is the power that is dissipated in the NMOS pass element, and can be determined with the formula:

$$P_{D(PASS)} = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (8)$$

The second part is the power that is dissipated in the bias and control circuitry, and can be determined with the formula:

$$P_{D(BIAS)} = V_{BIAS} \times I_{GND(BIAS)} \quad (9)$$

where $I_{GND(BIAS)}$ is the portion of the operating ground current of the device that is related to V_{BIAS}.

The third part is the power that is dissipated in portions of the output stage circuitry, and can be determined with the formula:

$$P_{D(IN)} = V_{IN} \times I_{GND(IN)} \quad (10)$$

where $I_{GND(IN)}$ is the portion of the operating ground current of the device that is related to V_{IN}.

The total power dissipation is then:

$$P_D = P_{D(PASS)} + P_{D(BIAS)} + P_{D(IN)} \quad (11)$$

The maximum allowable junction temperature rise (ΔT_J) depends on the maximum anticipated ambient temperature (T_A) for the application, and the maximum allowable operating junction temperature ($T_{J(MAX)}$) .

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad (12)$$

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA}, can be calculated using the formula:

$$\theta_{JA} \leq \frac{\Delta T_J}{P_D} \quad (13)$$

Heat-Sinking The TO-220 Package

The TO220-5 package has a θ_{JA} rating of 60°C/W and a θ_{JC} rating of 3°C/W. These ratings are for the package only, no additional heat-sinking, and with no airflow. If the needed θ_{JA}, as calculated above, is greater than or equal to 60°C/W then no additional heat-sinking is required since the package can safely dissipate the heat and not exceed the operating $T_{J(MAX)}$. If the needed θ_{JA} is less than 60°C/W then additional heat-sinking is needed.

The thermal resistance of a TO-220 package can be reduced by attaching it to a heat sink or a copper plane on a PC board. If a copper plane is to be used, the values of θ_{JA} will be same as shown in next section for TO-263 package.

The heat-sink to be used in the application should have a heat-sink to ambient thermal resistance, θ_{HA}:

$$\theta_{HA} \leq \theta_{JA} - (\theta_{CH} + \theta_{JC}) \quad (14)$$

where θ_{JA} is the required total thermal resistance from the junction to the ambient air, θ_{CH} is the thermal resistance from the case to the surface of the heart-sink, and θ_{JC} is the thermal resistance from the junction to the surface of the case.

For this equation, θ_{JC} is about 3°C/W for a TO-220 package. The value for θ_{CH} depends on method of attachment, insulator, etc. θ_{CH} varies between 1.5°C/W to 2.5°C/W. Consult the heat-sink manufacturer datasheet for details and recommendations.

Heat-Sinking The TO-263 Package

The TO-263 package has a θ_{JA} rating of 60°C/W, and a θ_{JC} rating of 3°C/W. These ratings are for the package only, no additional heat-sinking, and with no airflow.

The TO-263 package uses the copper plane on the PCB as a heat-sink. The tab of this package is soldered to the copper plane for heat sinking. *Figure 3* shows a curve for the θ_{JA} of TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat-sinking.

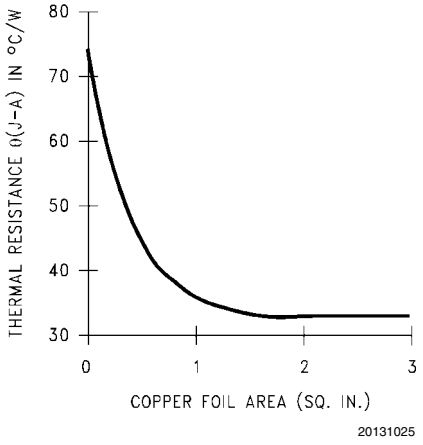


FIGURE 3. θ_{JA} vs Copper (1 Ounce) Area for the TO-263 package

Figure 3 shows that increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for θ_{JA} for the TO-263 package mounted to a PCB is 32°C/W.

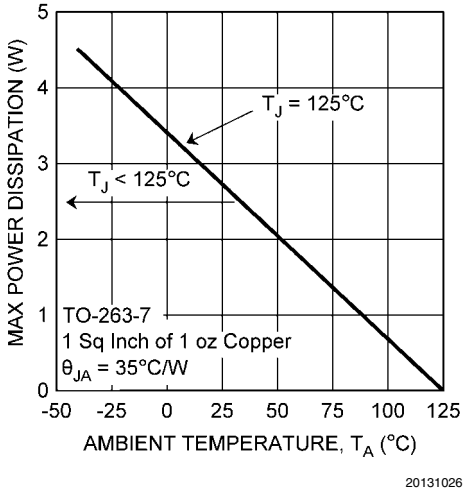


FIGURE 4. Maximum Power Dissipation vs Ambient Temperature for the TO-263 Package

Figure 4 shows the maximum allowable power dissipation for TO-263 packages for different ambient temperatures, assuming θ_{JA} is 35°C/W and the maximum junction temperature is 125°C.

Heat-Sinking The PSOP-8 Package

The LP38853MR package has a θ_{JA} rating of 168°C/W, and a θ_{JC} rating of 11°C/W. The θ_{JA} rating of 168°C/W includes the device DAP soldered to an area of 0.008 square inches (0.09 in x 0.09 in) of 1 ounce copper, with no airflow.

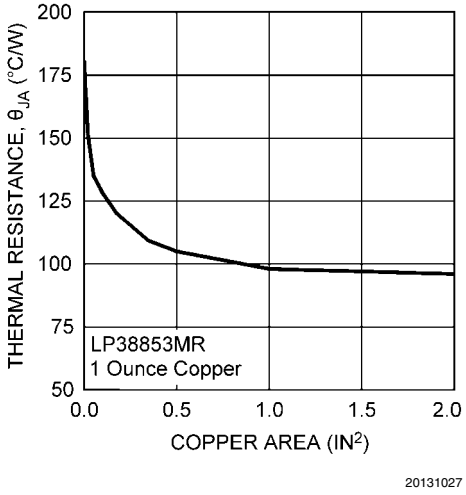


FIGURE 5. θ_{JA} vs Copper (1 Ounce) Area for the PSOP-8 Package

Increasing the copper area soldered to the DAP to 1 square inch of 1 ounce copper, using a dog-bone type layout, will improve the θ_{JA} rating to 98°C/W. *Figure 5* shows that increasing the copper area beyond 1 square inch produces very little improvement.

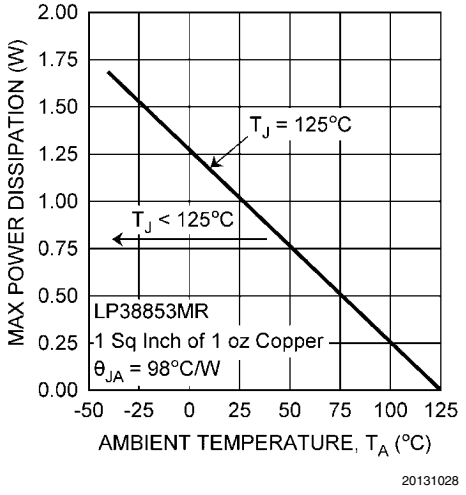
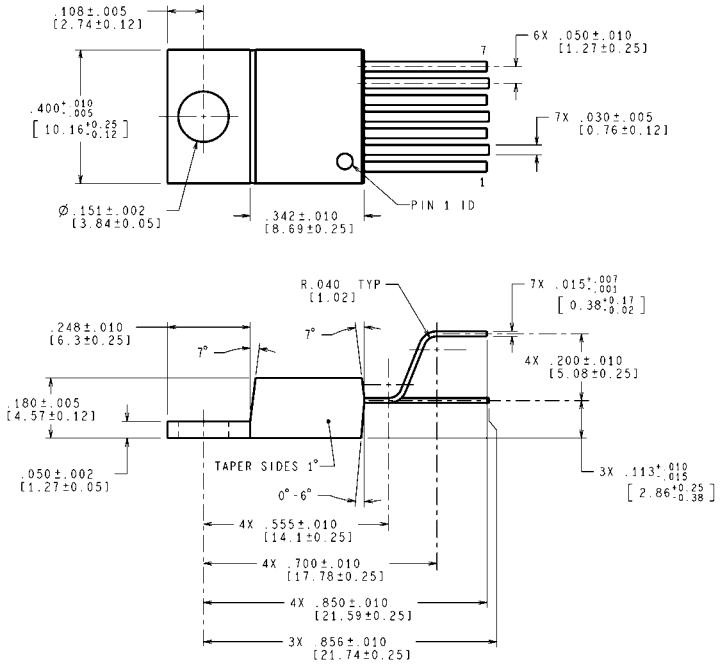


FIGURE 6. Maximum Power Dissipation vs Ambient Temperature for the PSOP-8 Package

Figure 6 shows the maximum allowable power dissipation for the PSOP-8 package for a range of ambient temperatures, assuming θ_{JA} is 98°C/W and the maximum junction temperature is 125°C.

Physical Dimensions inches (millimeters) unless otherwise noted



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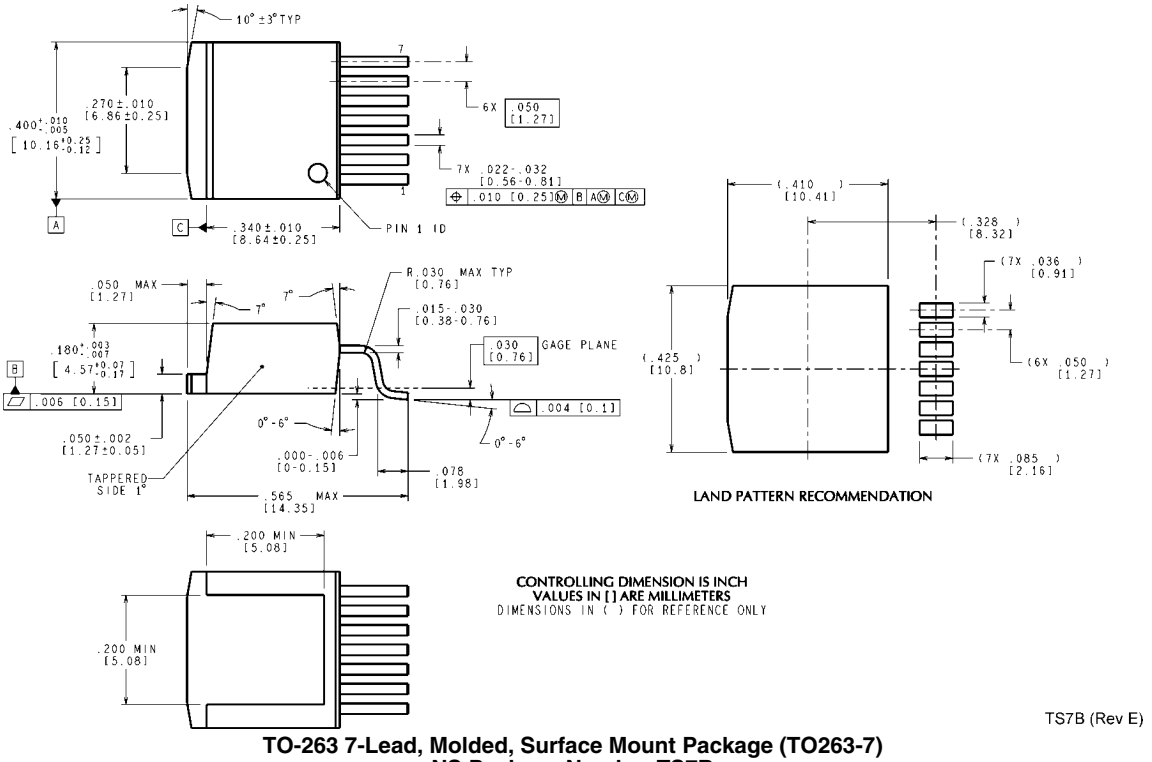
TA07B (Rev E)

TO-220 7-Lead, Stagger Bend Package (TO220-7)
NS Package Number TA07B



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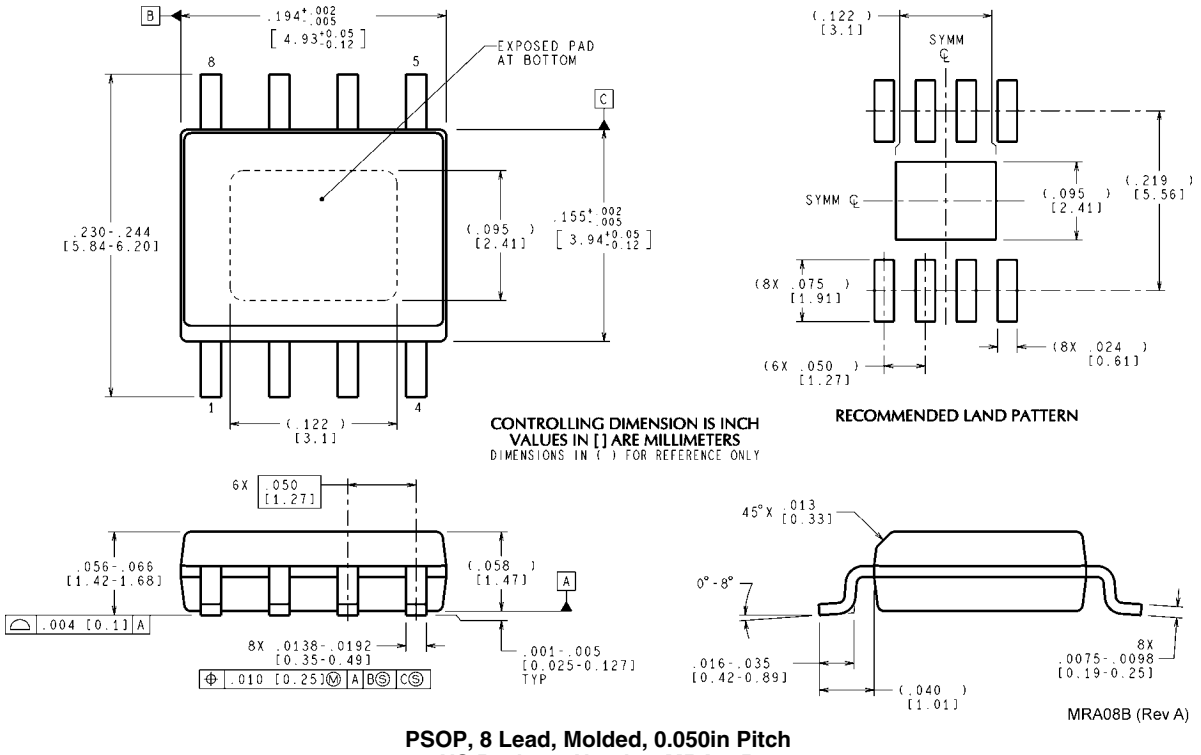
TS7B (Rev E)

TO-263 7-Lead, Molded, Surface Mount Package (TO263-7)
NS Package Number TS7B



PSOP, 8 Lead, Molded, 0.050in Pitch
NS Package Number MRA08B

Notes

Notes

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