National Semiconductor

August 26, 2008

LP3921
Battery Charger Management and Regulator Unit with Integrated Boomer® Audio Amplifier

General Description

The LP3921 is a fully integrated charger and multi-regulator unit with a fully differential Boomer audio power amplifier designed for CDMA cellular phones. The LP3921 has a high-speed serial interface which allows for the integration and control of a Li-Ion battery charger, 7 low-noise low-dropout (LDO) voltage regulators and a Boomer audio amplifier.

The Li-Ion charger integrates a power FET, reverse current blocking diode, sense resistor with current monitor output, and requires only a few external components. Charging is thermally regulated to obtain the most efficient charging rate for a given ambient temperature.

LDO regulators provide high PSRR and low noise ideally suited for supplying power to both analog and digital loads.

The Boomer Audio Amplifier is capable of delivering 1.1 watts of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N). Boomer Audio Power Amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The Boomer Audio Amplifier does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption and part count is the primary requirement. The Boomer Audio Amplifier contains advanced pop & click circuitry which eliminates noises during turn-on and turn-off transitions.

Features

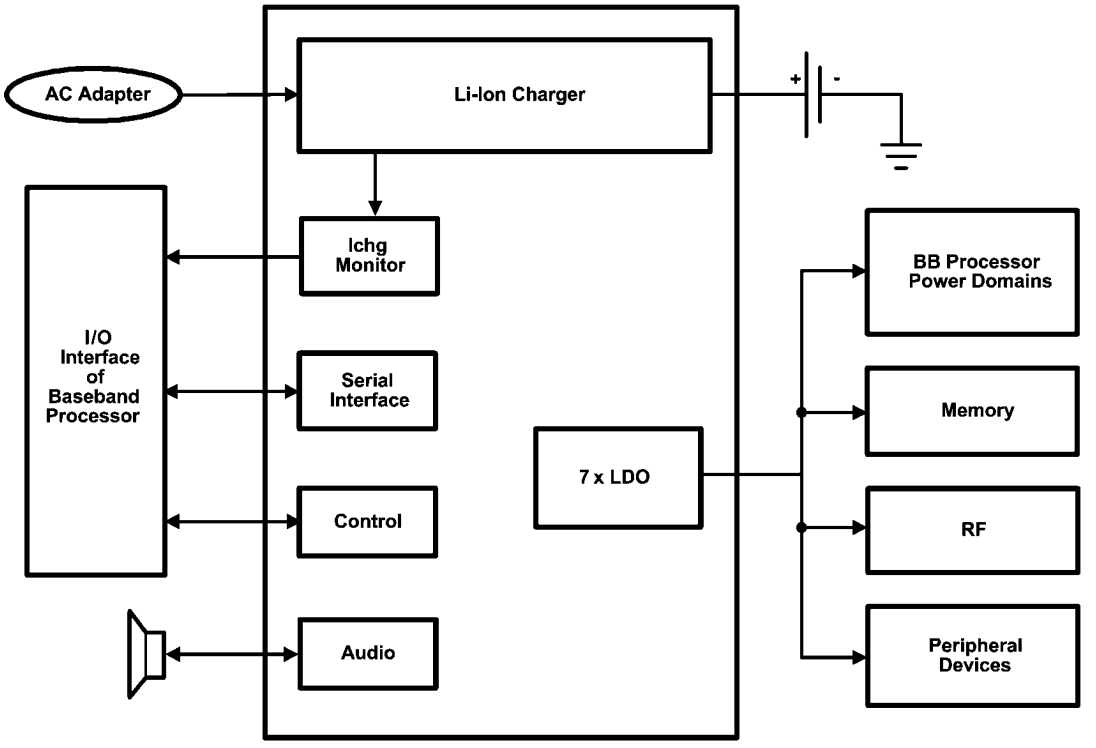
- Charger
  - — DC adapter or USB input
  - — Thermally regulated Charge Current
  - — Under Voltage Lockout
  - — 50 to 950 mA Programmable Charge Current
- 3.0V to 5.5V Input Voltage Range
- Thermal shutdown
- I²C-compatible Interface for controlling Charger, LDO outputs and enabling Audio output
- LDO's
  7 Low-Noise LDO's
  - — 2 x 300 mA
  - — 3 x 150 mA
  - — 2 x 80 mA
  2% (typ.) Output Voltage Accuracy on LDO's
- Audio
  - — Fully Differential Amplification
  - — Ability to drive capacitive loads up to 100 pF
  - — No output coupling capacitors, snubber networks or bootstrap capacitors required
- Space- Efficient 32-pin 5 x 5 mm LLP package

Applications

- CDMA Phone Handsets
- Low Power Wireless Handsets
- Handheld Information Appliances
- Personal Media Players

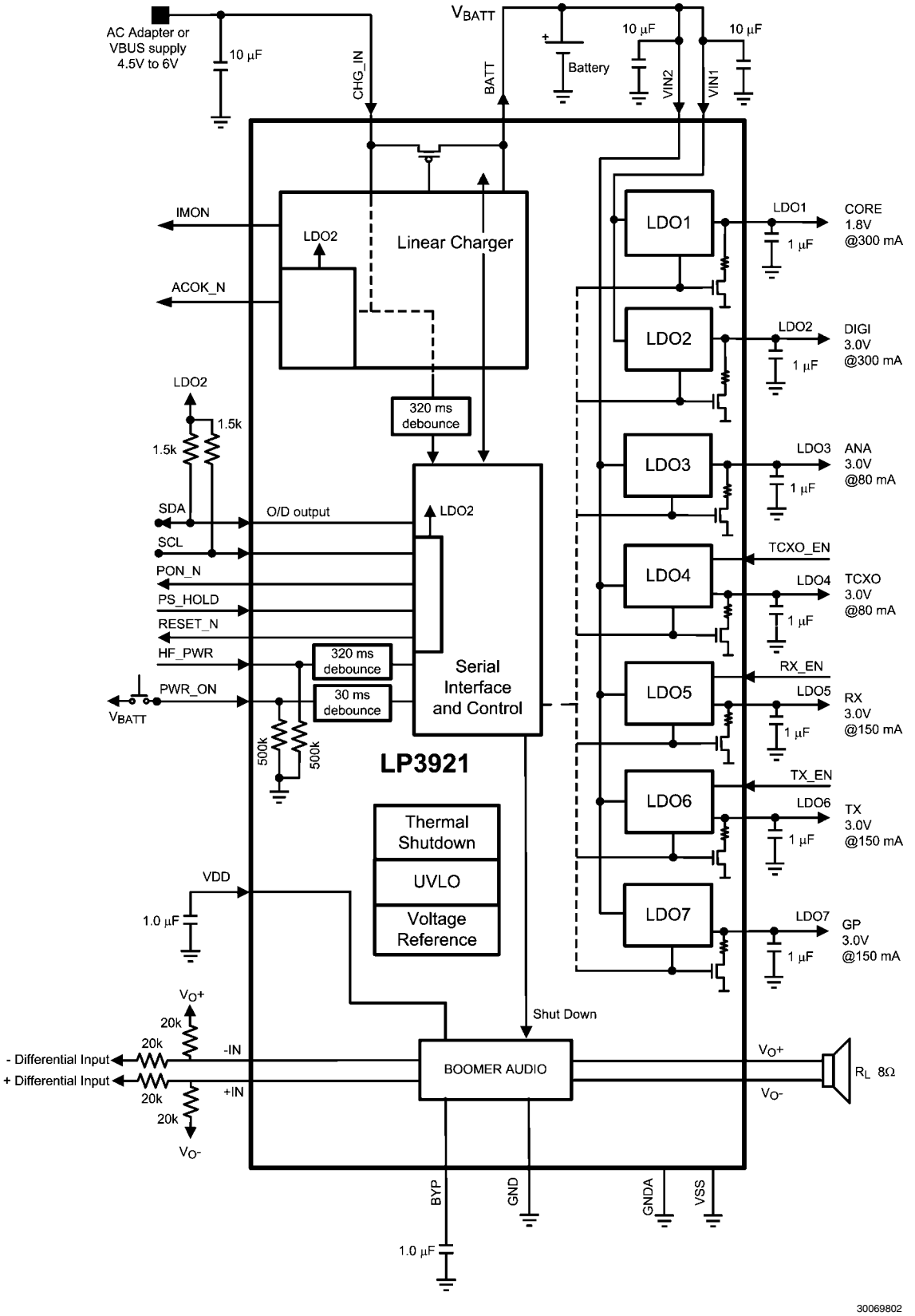
Boomer® is a registered trademark of National Semiconductor Corporation.

System Diagram

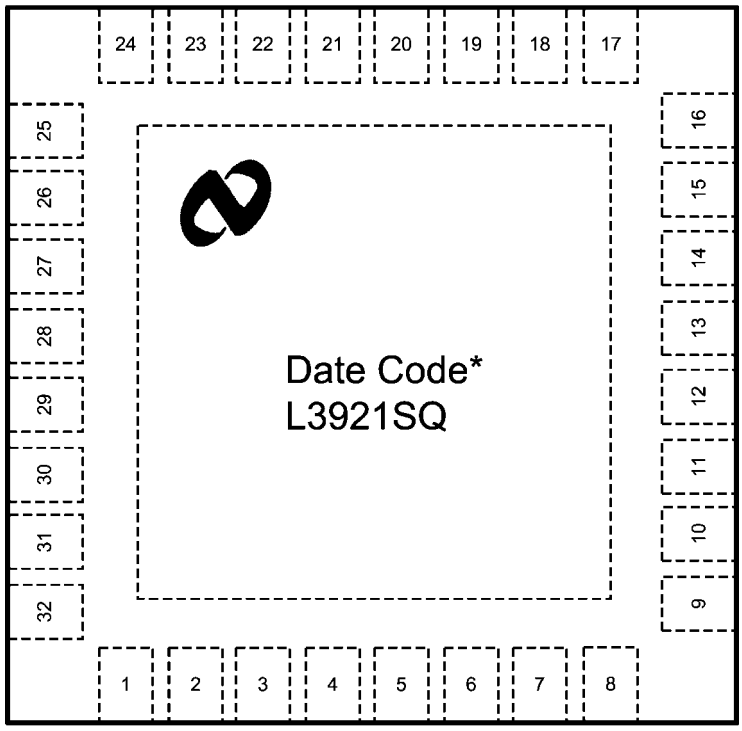


30069801

Functional Block Diagram



Connection Diagram – Device Pin Diagram



30069803

* Date code is in UZXYTT format where:

- U - Wafer Fab Code
- Z - Assembly Plant
- XY - 2-Digit Date Code
- TT - Lot Traceability

Ordering Information

Order Number	SPEC	Package Marking	Supplied As
LP3921SQE	NOPB	L3921SQ	250 units, Tape & Reel
LP3921SQ	NOPB	L3921SQ	1000 units, Tape & Reel
LP3921SQX	NOPB	L3921SQ	4500 units, Tape & Reel

Device Description

The LP3921 Charge Management and Regulator Unit is designed to supply charger and voltage output capabilities for mobile systems, e.g. CDMA handsets. The device provides a Li-Ion charging function and 7 regulated outputs. Communication with the device is via an I²C compatible serial interface that allows function control and status read-back.

The battery charge management section provides a programmable CC/CV linear charge capability. Following a normal charge cycle a maintenance mode keeps battery voltage between programmable levels. Power levels are thermally regulated to obtain optimum charge levels over the ambient temperature range.

CHARGER FEATURES

- Pre-charge, CC, CV and Maintenance modes
- USB Charge 100 mA/450 mA
- Integrated FET
- Integrated Reverse Current Blocking Diode
- Integrated Sense Resistor
- Thermal regulation
- Charge Current Monitor Output
- Programmable charge current 50 mA - 950 mA with 50 mA steps
- Default CC mode current 100 mA
- Pre-charge current fixed 50 mA
- Termination voltage 4.1V, 4.2V (default), 4.3V, and 4.4V, accuracy better than +/- 0.35% (typ.)
- Restart level 100 mV, 150 mV (default) and 200 mV below Termination voltage
- Programmable End of Charge 0.1C (default), 0.15C, 0.2C and 0.25C
- Enable Control Input
- Safety timer
- Input voltage operating range 4.5V - 6.0V

REGULATORS

Seven low-dropout linear regulators provide programmable voltage outputs with current capabilities of 80 mA, 150 mA and 300 mA as given in the table below. LDO1, LDO2 and LDO3 are powered up by default with LDO1 reaching regulation before LDO2 and LDO3 are started. LDO1, LDO3 and LDO7 can be disabled/enabled via the serial interface. LDO1 and LDO2, if enabled, must be in regulation for the device to power up and remain powered. LDO4, LDO5 and LDO6 have external enable pins and may power up following LDO2 as determined by their respective enable. Under voltage lockout oversees device start up with preset level of 2.85V (typ.).

POWER SUPPLY CONFIGURATIONS

At PMU start up, LDO1, LDO2 and LDO3 are always started with their default voltages. The start up sequence of the LDO's is given below.

Startup Sequence

LDO1 -> LDO2 -> LDO3

LDO's with external enable control (LDO4, LDO5, LDO6) start immediately after LDO2 if enabled by logic high at their respective control inputs.

LDO7 (and LDO1, LDO3) may be programmed to enable/disable once PS_HOLD has been asserted.

DEVICE PROGRAMMABILITY

An I²C compatible Serial Interface is used to communicate with the device to program a series of registers and also to read status registers. These internal registers allow control over LDO outputs and their levels. The charger functions may also be programmed to alter termination voltage, end of charge current, charger restart voltage, full rate charge current, and also the charging mode.

This device internal logic is powered from LDO2.

TABLE 1. LDO Default Voltages

LDO	Function	mA	Default Voltage (V)	Startup Default	Enable Control
1	CORE	300	**1.8**	ON	SI
2	DIGI	300	**3.0**	ON	-
3	ANA	80	**3.0**	ON	SI
4	TCXO	80	**3.0**	OFF	TCXO_EN
5	RX	150	**3.0**	OFF	RX_EN
6	TX	150	**3.0**	OFF	TX_EN
7	GP	150	**3.0**	OFF	SI

TABLE 2. LDO Output Voltages Selectable via Serial Interface

LDO		mA	1.5	1.8	1.85	2.5	2.6	2.7	2.75	2.8	2.85	2.9	2.95	3.0	3.05	3.1	3.2	3.3
1	CORE	300	+	**+**	+	+	+	+	+	+	+	+	+	+	+	+	+	+
2	DIGI	300				+	+	+	+	+	+	+	+	**+**	+	+	+	+
3	ANA	80						+	+	+	+	+	+	**+**	+			
4	TCXO	80	+	+	+	+	+	+	+	+	+	+	+	**+**	+	+	+	+
5	RX	150						+	+	+	+	+	+	**+**	+			
6	TX	150						+	+	+	+	+	+	**+**	+			
7	GP	150	+	+	+	+	+	+	+	+	+	+	+	**+**	+	+	+	+

LP3921 Pin Descriptions

Pin#	Name	Type	Description
1	LDO6	A	LDO6 Output (TX)
2	TX_EN	DI	Enable control for LDO6 (TX). HIGH = Enable, LOW = Disable
3	LDO5	A	A LDO5 Output (RX)
4	VIN2	P	Battery Input for LDO3 - LDO7
5	LDO7	A	LDO7 Output (GP)
6	OUT+	AO	Differential output +
7	VDD	P	DC power input to audio amplifier
8	OUT-	AO	Differential output -
9	IN+	AI	Differential input +
10	IN-	AI	Differential input -
11	GND	G	Analog Ground Pin
12	BYPASS	A	Amplifier bypass cap
13	LDO4	A	LDO4 Output (TCXO)
14	LDO3	A	LDO3 Output (ANA)
15	LDO2	A	LDO2 Output (DIGI)
16	LDO1	A	LDO1 Output (CORE)
17	VIN1	P	Battery Input for LDO1 and LDO2
18	GNDA	G	Analog Ground pin
19	SDA	DI/O	Serial Interface, Data Input/Output Open Drain output, external pull up resistor is needed. (typ. 1.5k)
20	SCL	DI	Serial Interface Clock input. External pull up resistor is needed. (typ. 1.5k)
21	BATT	P	Main battery connection. Used as a power connection for current delivery to the battery.
22	CHG_IN	P	DC power input to charger block from wall or car power adapters.
23	PWR_ON	DI	Power up sequence starts when this pin is set HIGH. Internal 500k. pull-down resistor.
24	IMON	A	Charge current monitor output. This pin presents an analog voltage representation of the input charging current. VIMON (mV) = (2.47 x ICHG)(mA).
25	PS_HOLD	DI	Input for power control from external processor/controller.
26	TCXO_EN	DI	Enable control for LDO4 (TX). HIGH = Enable, LOW = Disable.
27	HF_PWR	DI	Power up sequence starts when this pin is set HIGH. Internal 500k. pull-down resistor.
28	VSS	G	Digital Ground pin
29	PON_N	DO	Active low signal is PWR_ON inverted.
30	RESET_N	DO	Reset Output. Pin stays LOW during power up sequence. 60 ms after LDO1 (CORE) is stable this pin is asserted HIGH.
31	ACOK_N	DO	AC Adapter indicator, LOW when 4.5V- 6.0V present at CHG_IN.
32	RX_EN	DI	Enable control for LDO5 (RX). HIGH = Enable, LOW = Disable.

Key: A=Analog; D=Digital; I=Input; DI/O=Digital-Input/Output; G=Ground; O=Output; P=Power

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

CHG-IN	−0.3 to +6.5V
V_{BATT} =VIN1/2, BATT, VDD, HF_PWR	−0.3 to +6.0V
All other Inputs	−0.3 to V_{BATT} +0.3V, max 6.0V
Junction Temperature (T_{J-MAX})	150°C
Storage Temperature	−40°C to +150°C
Max Continuous Power Dissipation (P_{D-MAX}) (Note 3)	Internally Limited
ESD (Note 4)	
BATT, VIN1, VIN2, VDD, HF_PWR, CHG_IN, PWR_ON	8 kV HBM
All other pins	2 kV HBM

Operating Ratings (Notes 1, 2)

CHG_IN (Note 10)	4.5 to 6.0V
V_{BATT} =VIN1/2, BATT, VDD	3.0 to 5.5V
HF_PWR, PWR_ON	0V to 5.5V
ACOK_N, SDA, SCL, RX_EN, TX_EN, TCXO_EN, PS_HOLD, RESET_N	0V to (V_{LDO2} + 0.3V)
All other pins	0V to (V_{BATT} + 0.3V)
Junction Temperature (T_J)	−40°C to +125°C
Ambient Temperature (T_A) (Note 5)	-40 to 85°C

Thermal Properties (Note 9)

Junction to Ambient Thermal Resistance θ_{JA}	
4L Jedec Board	30° C/W

General Electrical Characteristics

Unless otherwise noted, V_{IN} (=VIN1=VIN2=BATT=VDD) = 3.6V, GND = 0V, C_{VIN1-2}=10 µF, C_{LDOX}=1 µF. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_A = T_J$ = −40°C to +125°C. (Note 6)

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
$I_{Q(STANDBY)}$	Standby Supply Current	V_{IN} = 3.6V, UVLO on, internal logic circuit on, all other circuits off	2		5	µA
POWER MONITOR FUNCTIONS						
Battery Under-Voltage Lockout						
V_{UVLO-R}	Under Voltage Lock-out	V_{IN} Rising	2.85	2.7	3.0	V
THERMAL SHUTDOWN						
	Higher Threshold	(Note 7)	160			°C
LOGIC AND CONTROL INPUTS						
V_{IL}	Input Low Level	PS_HOLD, SDA, SCL, RX_EN, TCXO_EN, TX_EN (Note 7)			0.25* V_{LDO2}	V
		PWR_ON, HF_PWR (Note 7)			0.25* V_{BATT}	V
V_{IH}	Input High Level	PS_HOLD, SDA, SCL, RX_EN, TCXO_EN, TX_EN (Note 7)		0.75* V_{LDO2}		V
		PWR_ON, HF_PWR (Note 7)		0.75* V_{BATT}		V
I_{IL}	Logic Input Current	All logic inputs except PWR_ON and HF_PWR 0V ≤ V_{INPUT} ≤ V_{BATT}		**-5**	**+5**	µA
R_{IN}	Input Resistance	PWR_ON, HF_PWR Pull-Down resistance to GND	500			kΩ
LOGIC AND CONTROL OUTPUTS						
V_{OL}	Output Low Level	PON_N, RESET_N, SDA, ACOK_N I_{OUT} = 2 mA			0.25* V_{LDO2}	V
V_{OH}	Output High Level	PON_N, RESET_N, ACOK_N I_{OUT} = -2 mA (Not applicable to Open Drain Output SDA)		0.75* V_{LDO2}		V

LDO1 (CORE) Electrical Characteristics

Unless otherwise noted, V_{IN} (=VIN1=VIN2=BATT=VDD) = 3.6V, GND = 0V, C_{VIN1-2}=10 µF, C_{LDOX}=1 µF. Note V_{INMIN} is the greater of 3.0V or V_{OUT1}+ 0.5V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_A = T_J$ = −40°C to +125°C. (Note 6)

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
V_{OUT1}	Output Voltage Accuracy	I_{OUT1} = 1 mA, V_{OUT1}= 3.0V		−2	+2	%
				−3	**+3**	
	Output Voltage	Default	1.8			V
I_{OUT1}	Output Current	$V_{INMIN} \leq V_{IN} \leq 5.5V$			**300**	mA
	Output Current Limit	V_{OUT1} = 0V	600			
V_{DO1}	Dropout Voltage	I_{OUT1} = 300 mA (Note 8)	220		310	mV
ΔV_{OUT1}	Line Regulation	$V_{INMIN} \leq V_{IN} \leq 5.5V$ I_{OUT1} = 1 mA	2			mV
	Load Regulation	1 mA ≤ I_{OUT1} ≤ 300 mA	10			mV
e_{n1}	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 1 µF (Note 7)	45			μV_{RMS}
PSRR	Power Supply Rejection Ratio	F = 10 kHz, C_{OUT} = 1 µF I_{OUT1} = 20 mA (Note 7)	65			dB
$t_{START-UP}$	Start-Up Time from Internal Enable	C_{OUT} = 1 µF, I_{OUT1} = 300 mA (Note 7)	60		**170**	µs
$T_{Transient}$	Start-Up Transient Overshoot	C_{OUT} = 1 µF, I_{OUT1} = 300 mA (Note 7)	60		**120**	mV

LDO2 (DIGI) Electrical Characteristics

Unless otherwise noted, V_{IN} (=VIN1=VIN2=BATT=VDD) = 3.6V, GND = 0V, C_{VIN1-2}=10 µF, C_{LDOX}=1 µF. Note V_{INMIN} is the greater of 3.0V or V_{OUT2}+ 0.5V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_A = T_J$ = −40°C to +125°C. (Note 6)

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
V_{OUT2}	Output Voltage Accuracy	I_{OUT2} = 1 mA, V_{OUT2}= 3.0V		−2	+2	%
				−3	**+3**	
	Output Voltage	Default	3			V
I_{OUT2}	Output Current	$V_{INMIN} \leq V_{IN} \leq 5.5V$			**300**	mA
	Output Current Limit	V_{OUT2} = 0V	600			
V_{DO2}	Dropout Voltage	I_{OUT2} = 300 mA (Note 8)	220		310	mV
ΔV_{OUT2}	Line Regulation	$V_{INMIN} \leq V_{IN} \leq 5.5V$ I_{OUT2} = 1mA	2			mV
	Load Regulation	1 mA ≤ I_{OUT2} ≤ 300 mA	10			mV
e_{n2}	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 1 µF (Note 7)	45			μV_{RMS}
PSRR	Power Supply Rejection Ratio	F = 10 kHz, C_{OUT} = 1 µF I_{OUT2} = 20 mA (Note 7)	65			dB
$t_{START-UP}$	Start-Up Time from Shutdown	C_{OUT} = 1 µF, I_{OUT2} = 300 mA (Note 7)	40		**60**	µs
$t_{Transient}$	Start-Up Transient Overshoot	C_{OUT} = 1 µF, I_{OUT2} = 300 mA (Note 7)	5		**30**	mV

LDO3 (ANA), LDO4 (TCXO) Electrical Characteristics

Unless otherwise noted, V_{IN} (=VIN1=VIN2=BATT=VDD) = 3.6V, GND = 0V, C_{VIN1-2}=10 µF, C_{LDOX}=1 µF. TCXO_EN high. Note V_{INMIN} is the greater of 3.0V or $V_{OUT3/4}$ + 0.5V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_A = T_J$ = −40°C to +125°C. (Note 6)

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
V_{OUT3}, V_{OUT4}	Output Voltage Accuracy	$I_{OUT3/4}$ = 1 mA, $V_{OUT3/4}$= 3.0V		−2	+2	%
				−3	**+3**	
	Output Voltage	LDO3 default	3			V
		LDO4 default	3			
I_{OUT3}, I_{OUT4}	Output Current	$V_{INMIN} \leq V_{IN} \leq 5.5V$			**80**	mA
	Output Current Limit	$V_{OUT3/4}$ = 0V	160			
V_{DO3}, V_{DO4}	Dropout Voltage	$I_{OUT3/4}$ = 80 mA (Note 8)	220		310	mV
ΔV_{OUT3} , ΔV_{OUT4}	Line Regulation	$V_{INMIN} \leq V_{IN} \leq 5.5V$ $I_{OUT3/4}$ = 1 mA	2			mV
	Load Regulation	1mA ≤ $I_{OUT3/4}$ ≤ 80 mA	5			mV
e_{n3},e_{n4}	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 1 µF (Note 7)	45			μV_{RMS}
PSRR	Power Supply Rejection Ratio	F = 10 kHz, C_{OUT} = 1 µF $I_{OUT3/4}$ = 20 mA (Note 7)	65			dB
$t_{START-UP}$	Start-Up Time from Enable (Note 7)	C_{OUT} = 1 µF, $I_{OUT3/4}$ = 80mA	40		**60**	µs
$t_{Transient}$	Start-Up Transient Overshoot	C_{OUT} = 1µF, $I_{OUT3/4}$ = 80 mA (Note 7)	5		**30**	mV

LDO5 (RX), LDO6 (TX), LDO7 (GP) Electrical Characteristics

Unless otherwise noted, V_{IN} (=VIN1=VIN2=BATT=VDD) = 3.6V, GND = 0V, C_{VIN1-2}=10 µF, C_{LDOX}=1 µF. RX_EN, TX_EN high. LDO7 Enabled via Serial Interface. Note V_{INMIN} is the greater of 3.0V or $V_{OUT5/6/7}$ + 0.5V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_A = T_J$ = −40°C to +125°C. (Note 6)

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
V_{OUT5}, V_{OUT6}, V_{OUT7}	Output Voltage	$I_{OUT5/6/7}$ = 1mA, $V_{OUT5/6/7}$= 3.0V		−2	+2	%
				−3	**+3**	
	Default Output Voltage	LDO5	3			V
		LDO6	3			
		LDO7	3			
I_{OUT5}, I_{OUT6}, I_{OUT7}	Output Current	$V_{INMIN} \le V_{IN} \le 5.5V$			**150**	mA
	Output Current Limit	$V_{OUT5/6/7}$ = 0V	300			
V_{DO5}, V_{DO6}, V_{DO7}	Dropout Voltage	$I_{OUT5/6/7}$ = 150 mA (Note 8)	200		280	mV
ΔV_{OUT5}, ΔV_{OUT6}, ΔV_{OUT7}	Line Regulation	$V_{INMIN} \le V_{IN} \le 5.5V$ $I_{OUT5/6/7}$ = 1 mA	2			mV
	Load Regulation	$1mA \le I_{OUT5/6/7} \le 150$ mA	10			mV
e_{n5}, e_{n6}, e_{n7}	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 1 µF (Note 7)	45			μV_{RMS}
PSRR	Power Supply Rejection Ratio	F = 10 kHz, C_{OUT} = 1 µF $I_{OUT5/6/7}$ = 20 mA (Note 7)	65			dB
$t_{START-UP}$	Start-Up Time from Enable	C_{OUT} = 1 µF, $I_{OUT5/6/7}$ = 150 mA (Note 7)	40		**60**	µs
$t_{Transient}$	Start-Up Transient Overshoot	C_{OUT} = 1 µF, $I_{OUT5/6/7}$ = 150 mA (Note 3)	5		**30**	mV

Charger Electrical Characteristics

Unless otherwise noted, V_{CHG-IN} = 5V, V_{IN} (=VIN1=VIN2=BATT=VDD) = 3.6V.C_{CHG_IN} = 10 µF. Charger set to default settings unless otherwise noted. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_A = T_J$ = –25°C to +85°C. (Notes 6, 9)

Symbol	Parameter	Condition		Typ	Limit		Units
					Min	Max	
V_{CHG-IN}	Input Voltage Range	(Note 7)			**4.5**	**6.5**	V
	Operating Range				**4.5**	**6**	
V_{OK_CHG}	CHG_IN OK trip-point	V_{CHG_IN} - V_{BATT} (Rising)		200			mV
		V_{CHG_IN} - V_{BATT} (Falling)		50			
V_{TERM}	Battery Charge Termination voltage	Default		4.2			V
	V_{TERM} voltage tolerance	T_J = 0°C to 85°C			**-1**	**+1**	%
I_{CHG}	Fast Charge Current Accuracy	I_{CHG} = 450 mA			**-10**	**+10**	%
	Programmable full-rate charge current range (default 100 mA)	6.0V ≥ V_{CHG_IN} ≥ 4.5V V_{BATT} < (V_{CHG_IN} - V_{OK_CHG}) V_{FULL_RATE} < V_{BATT} < V_{TERM} (Note 10)			50	950	mA
		Default		100			
	Charge current programming step			50			
$I_{PREQUAL}$	Pre-qualification current	V_{BATT} = 2V		50	**40**	**60**	mA
I_{CHG_USB}	CHG_IN programmable current in USB mode	5.5V ≥ V_{CHG_IN} ≥ 4.5V V_{BATT} < (V_{CHG_IN} - V_{OK_CHG}) V_{FULL_RATE} < V_{BATT} < V_{TERM}	Low	100			mA
			High	450			
		Default = 100 mA		100			
V_{FULL_RATE}	Full-rate qualification threshold	V_{BATT} rising, transition from pre-qual to full-rate charging		3	**2.9**	**3.1**	V
I_{EOC}	End of Charge Current, % of full-rate current	0.1C option selected		10			%
$V_{RESTART}$	Restart threshold voltage	V_{BATT} falling, transition from EOC to full-rate charge mode. Default options selected - 4.05V		4.05	**3.97**	**4.13**	V
I_{MON}	I_{MON} Voltage 1	I_{CHG} = 100 mA		0.247			V
	I_{MON} Voltage 2	I_{CHG} = 450 mA		1.112	0.947	1.277	
T_{REG}	Regulated junction temperature	(Note 7)		115			°C
Detection and Timing (Note 7)							
T_{POK}	Power OK deglitch time	V_{BATT} < (V_{CC} - V_{OK_CHG})		32			mS
T_{PQ_FULL}	Deglitch time	Pre-qualification to full-rate charge transition		230			mS
T_{CHG}	Charge timer	Precharge mode		1			Hrs
		Charging Timeout		5			
T_{EOC}	Deglitch time for end-of-charge transition			230			mS

Audio Electrical Characteristics

Unless otherwise noted, V_{DD}= 3.6V Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_A= T_J = −25°C to +85°C. (Note 6)

Symbol	Paramater	Conditions	Typical	Limit		Units
				Min	Max	
P_O	Output Power	THD = 1% (max); f = 1 kHz, R_L = 8Ω	0.375			W
THD + N	Total Harmonic Distortion + Noise	P_O = 0.25 Wrms; f = 1 kHz	0.02			%
PSRR	Power Supply Rejection Ratio	Vripple = 200 mV_{PP}				dB
		f = 217 Hz	85			
		f = 1 kHz	85		73	
CMRR	Common-Mode Rejection Ratio	f = 217 Hz, V_{CM} = 200 mV_{PP}	50			dB
V_{OS}	Output Offset	Vac_{INput} = 0V	4			mV

Serial Interface

Unless otherwise noted, V_{IN} (= VIN1 = VIN2 = BATT=VDD) = 3.6V, GND = 0V, C_{VIN1-2}=10 µF, C_{LDOX}=1 µF, and V_{LDO2} (DIGI) ≥ 1.8V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_A= T_J = −40°C to +125°C. (Notes 6, 7)

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
f_{CLK}	Clock Frequency				400	kHz
t_{BF}	Bus-Free Time between START and STOP			1.3		µs
t_{HOLD}	Hold Time Repeated START Condition			0.6		µs
t_{CLK-LP}	CLK Low Period			1.3		µs
t_{CLK-HP}	CLK High Period			0.6		µs
t_{SU}	Set-Up Time Repeated START Condition			0.6		µs
$t_{DATA-HOLD}$	Data Hold Time			50		ns
$t_{DATA-SU}$	Data Set-Up Time			100		ns
t_{SU}	Set-Up Time for STOP Condition			0.6		µs
t_{TRANS}	Maximum Pulse Width of Spikes that Must be Suppressed by the Input Filter of both DATA & CLK Signals		50			ns

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: Internal Thermal Shutdown circuitry protects the device from permanent damage.

Note 4: The human-body model is 100 pF discharged through 1.5 kΩ. The machine model is a 200 pF capacitor discharged directly into each pin, MIL-STD-883 3015.7.

Note 5: Care must be exercised where high power dissipation is likely. The maximum ambient temperature may have to be derated.

Like the Absolute Maximum power dissipation, the maximum power dissipation for operation depends on the ambient temperature. In applications where high power dissipation and/or poor thermal dissipation exists, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A_MAX}) is dependent on the maximum power dissipation of the device in the application (P_{D_MAX}), and the junction to ambient thermal resistance of the device/package in the application (θ_{JA}), as given by the following equation:

$T_{A\_MAX} = T_{J\_MAX-OP} - (\theta_{JA} \text{ X } P_{DMAX})$.

Note 6: All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 7: Guaranteed by design.

Note 8: Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply in cases it implies operation with an input voltage below the 3.0V minimum appearing under Operating Ratings. For example, this specification does not apply for devices having 1.5V outputs because the specification would imply operation with an input voltage at or about 1.5V.

Note 9: Junction-to-ambient thermal resistance (θ_{JA}) is taken from thermal modelling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The value of (θ_{JA}) of this product could fall within a wide range, depending on PWB material, layout, and environmental conditions. In applications where high maximum power dissipation exists (high $V_{IN,}$ high I_{OUT}), special care must be paid to thermal dissipation issues in board design.

Note 10: Full-charge current is guaranteed for CHG_IN = 4.5 to 6.0V. At higher input voltages, increased power dissipation may cause the thermal regulation to limit the current to a safe level, resulting in longer charging time.

Technical Description

DEVICE POWER UP AND SHUTDOWN TIMING

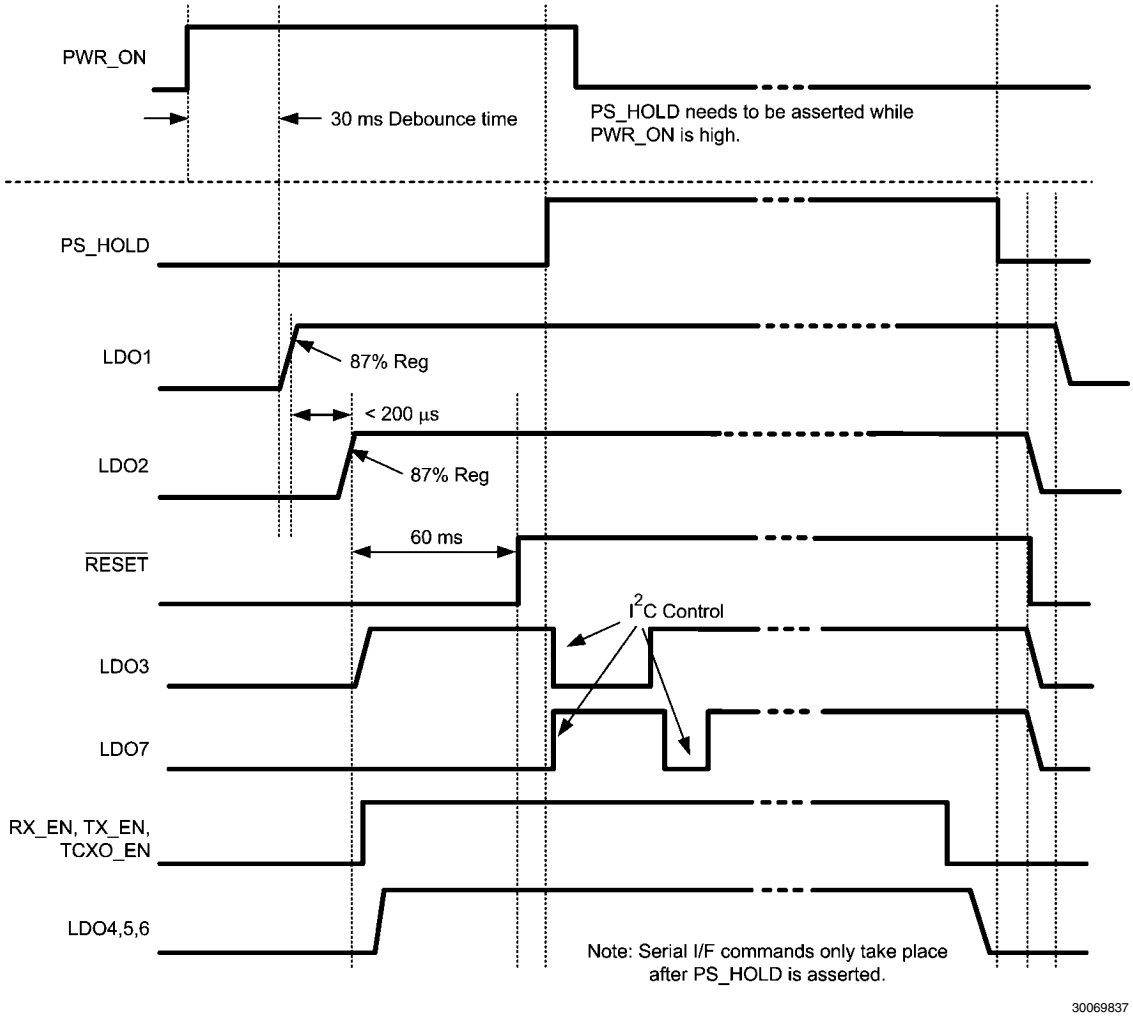


FIGURE 1. Device Power Up Logic Timing: PWR_ON

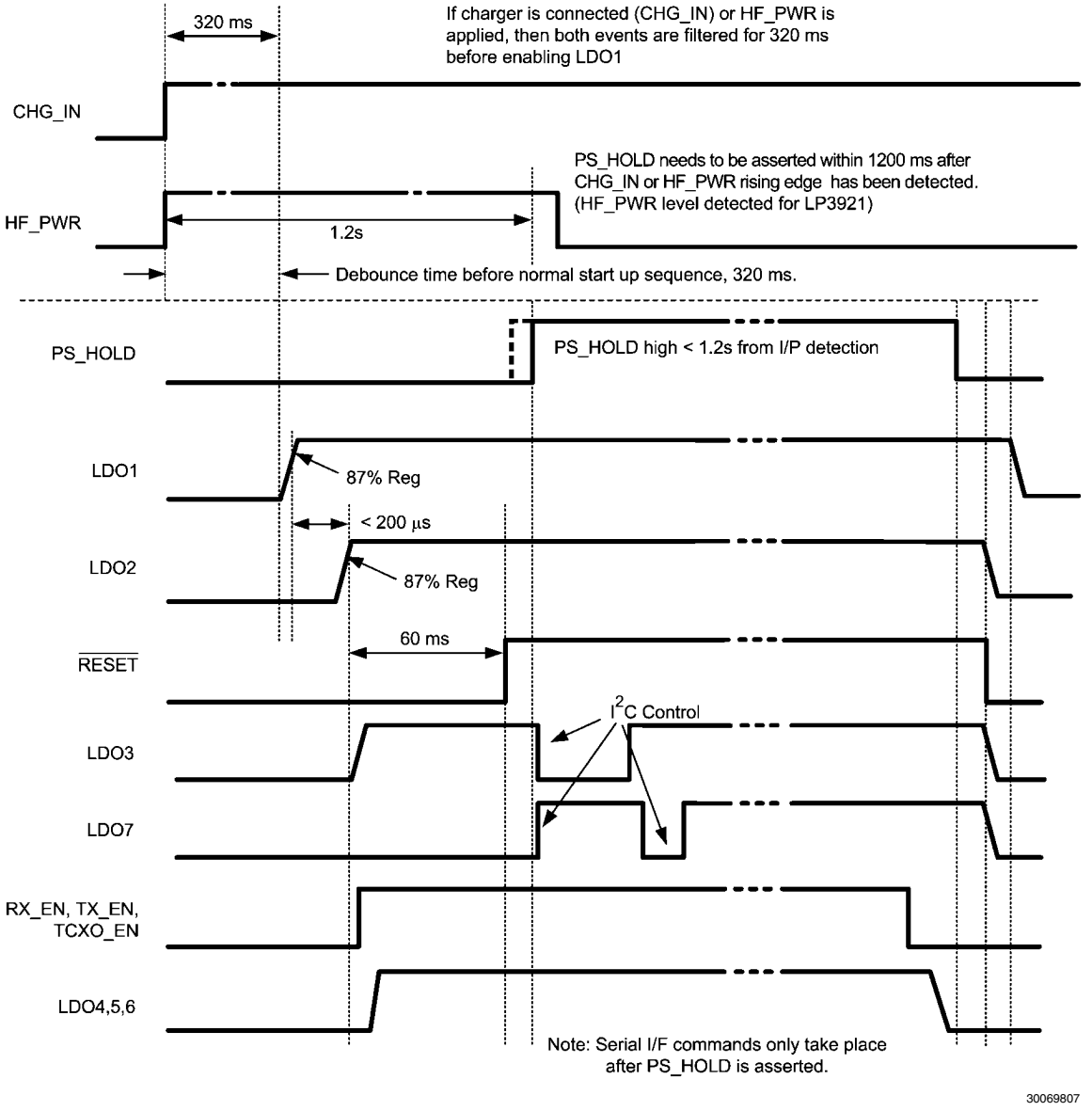


FIGURE 2. Device Power Up Logic Timing: CHG_IN, HF_PWR

START UP

Device start is initiated by any of the 3 input signals, PWR_ON, HF_PWR and CHG_IN.

PWR_ON

When PWR_ON goes high the device will remain powered up, a PS_HOLD applied will allow the device to remain powered after the PWR_ON signal has gone low.

HF_PWR, CHGIN

PS_HOLD needs to be asserted within 1200 ms after a CHG_IN or HF_PWR rising edge has been detected. For applications where a level sensitive input is required the LP3921 is available with a level detect input at HF_PWR.

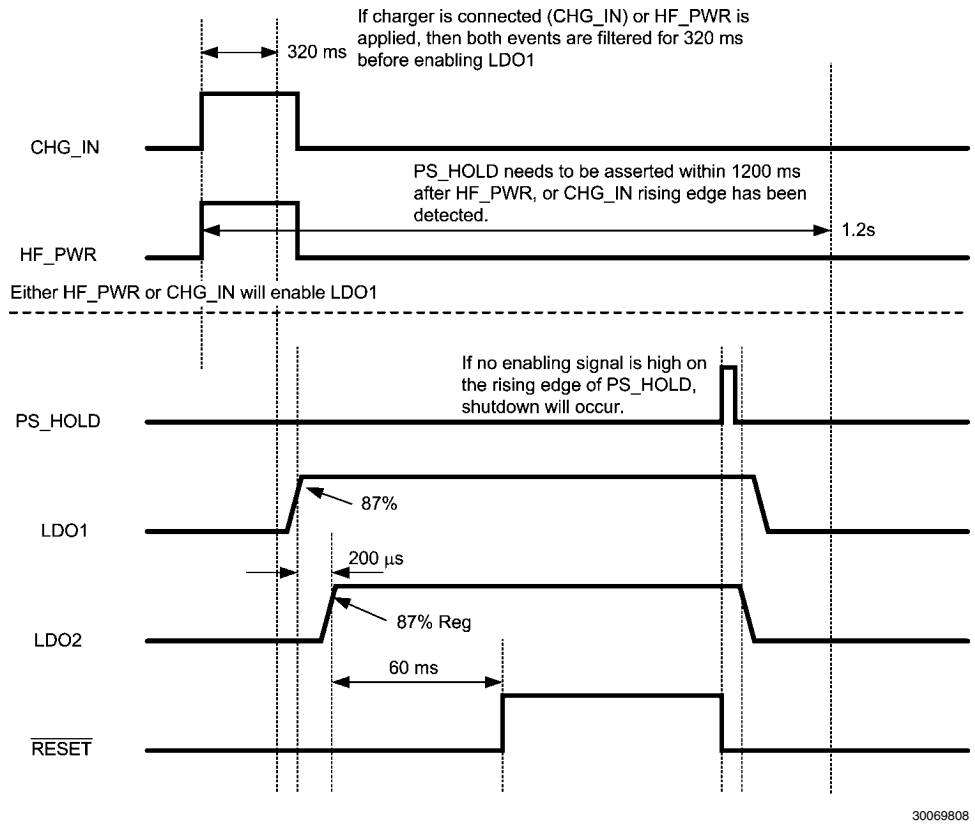


FIGURE 3. LP3921 Power On Behavior (Failed PS_Hold)

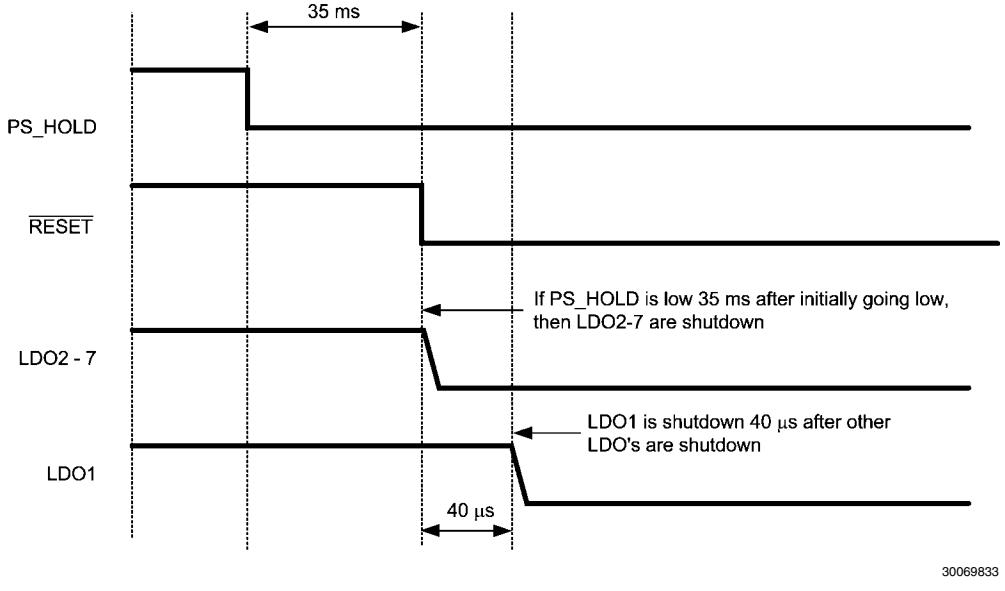


FIGURE 4. LP3921 Normal Shutdown Behavior

LP3921 Serial Port Communication

Slave Address Code 7h'7E

TABLE 3. Control Registers

Addr	Register (default value)	D7	D6	D5	D4	D3	D2	D1	D0
8h'00	OP_EN **(0000 0101)**	X	X	X	X	LDO7_EN	LDO3_EN	X	LDO1_EN
8h'01	LDO1PGM O/P **(0000 0001)**	X	X	X	X	V1_OP[3]	V1_OP[2]	V1_OP[1]	V1_OP[0]
8h'02	LDO2PGM O/P **(0000 1011)**	X	X	X	X	V2_OP[3]	V2_OP[2]	V2_OP[1]	V2_OP[0]
8h'03	LDO3PGM O/P **(0000 1011)**	X	X	X	X	V3_OP[3]	V3_OP[2]	V3_OP[1]	V3_OP[0]
8h'04	LDO4PGM O/P **(0000 1011)**	X	X	X	X	V4_OP[3]	V4_OP[2]	V4_OP[1]	V4_OP[0]
8h'05	LDO5PGM O/P **(0000 1011)**	X	X	X	X	V5_OP[3]	V5_OP[2]	V5_OP[1]	V5_OP[0]
8h'06	LDO6PGM O/P **(0000 1011)**	X	X	X	X	V6_OP[3]	V6_OP[2]	V6_OP[1]	V6_OP[0]
8h'07	LDO7PGM O/P **(0000 1011)**	X	X	X	X	V7_OP[3]	V7_OP[2]	V7_OP[1]	V7_OP[0]
8h'0C	STATUS **(0000 0000)**	**PWR_ON_ TRIB**	**HF_PWR_ TRIG**	**CHG_IN_ TRIG**	X	X	X	X	X
8h'10	CHGCNTL1 **(0000 1001)**	USBMODE _EN	CHGMODE _EN	Force EOC	TOUT_ doubling	EN_Tout	En_EOC	X	EN_CHG
8h'11	CHGCNTL2 **(0000 0001)**	X	X	X	Prog_ ICHG[4]	Prog_ ICHG[3]	Prog_ ICHG[2]	Prog_ ICHG[1]	Prog_ ICHG[0]
8h'12	CHGCNTL3 **(0001 0010)**	X	X	VTERM[1]	VTERM[0]	Prog_ EOC[1]	Prog_ EOC[0]	Prog_ VRSTRT[1]	Prog_ VRSTRT[0]
8h'13	CHGSTATUS1	**Batt_Over_ Out**	**CHGIN_ OK_Out**	**EOC**	**Tout_ Fullrate**	**Tout_ Prechg**	**LDO Mode**	**Fullrate**	**PRECHG**
8h'14	CHGSTATUS2	X	X	X	X	X	X	**Tout_ ConstV**	**Bad_Batt**
8h'19	Audio_Amp	X	X	X	X	X	X	X	amp_en
8h'1C	MISC Control1	X	X	X	X	X	X	APU_TSD_EN	PS_HOLD _DELAY

X Not Used

Bold Bits are Read Only type.

Codes other than those shown in the table are disallowed.

The following table summarizes the supported output voltages for the LP3921. Default voltages after startup are highlighted in **bold**.

TABLE 4. LDO Output Voltage Programming

Data Code LDOx PGM O/P	LDO1 (V)	LDO2 (V)	VLDO3 (V)	LDO4 (V)	LDO5 (V)	LDO6 (V)	LDO7 (V)
8h'00	1.5			1.5			1.5
8h'01	**1.8**			1.8			1.8
8h'02	1.85			1.85			1.85
8h'03	2.5	2.5		2.5			2.5
8h'04	2.6	2.6		2.6			2.6
8h'05	2.7	2.7	2.7	2.7	2.7	2.7	2.7
8h'06	2.75	2.75	2.75	2.75	2.75	2.75	2.75
8h'07	2.8	2.8	2.8	2.8	2.8	2.8	2.8
8h'08	2.85	2.85	2.85	2.85	2.85	2.85	2.85
8h'09	2.9	2.9	2.9	2.9	2.9	2.9	2.9
8h'0A	2.95	2.95	2.95	2.95	2.95	2.95	2.95
8h'0B	3.0	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**
8h'0C	3.05	3.05	3.05	3.05	3.05	3.05	3.05
8h'0D	3.1	3.1		3.1			3.1
8h'0E	3.2	3.2		3.2			3.2
8h'0F	3.3	3.3		3.3			3.3

The following table summarizes the supported charging current values for the LP3921. Default charge current after startup is 100 mA.

TABLE 5. Charging Current Programming

Prog_Ichg[4]	Prog_Ichg[3	Prog_Ichg[2]	Prog_Ichg[1]	Prog_Ichg[0]	I_Charge I mA
0	0	0	0	0	50
0	**0**	**0**	**0**	**1**	**100 (Default)**
0	0	0	1	0	150
0	0	0	1	1	200
0	0	1	0	0	250
0	0	1	0	1	300
0	0	1	1	0	350
0	0	1	1	1	400
0	1	0	0	0	450
0	1	0	0	1	500
0	1	0	1	0	550
0	1	0	1	1	600
0	1	1	0	0	650
0	1	1	0	1	700
0	1	1	1	0	750
0	1	1	1	1	800
1	0	0	0	0	850
1	0	0	0	1	900
1	0	0	1	0	950

TABLE 6. Charging Termination Voltage Control

VTERM[1]	VTERM[0]	Termination Voltage (V)
0	0	4.1
0	**1**	**4.2 (Default)**
1	0	4.3
1	1	4.4

TABLE 7. End Of Charge Current Control

PROG_EOC[1]	PROG_EOC[0]	End of Charge Current
0	**0**	**0.1 (Default)**
0	1	0.15C
1	0	0.2C
1	1	0.25C

Note: C is the set charge current.

TABLE 8. Charging Restart Voltage Programming

PROG_VRSTRT[1]	PROG_VRSTRT[1]	Restart Voltage(V)
0	0	V_{TERM} - 50 mV
0	1	V_{TERM} - 100 mV
1	**0**	**V_{TERM} - 150 mV**
1	1	V_{TERM} - 200 mV

TABLE 9. USB Charging Selection

USB_Mode_En	CHG_Mode_En	Mode	Current
0	**0**	**Fast Charge**	**Default or Selection**
1	0	Fast Charge	Default or Selection
0	1	USB	100 mA
1	1	USB	450 mA

Battery Charge Management

A charge management system allowing the safe charge and maintenance of a Li-Ion battery is implemented on the LP3921. This has a CC/CV linear charge capability with programmable battery regulation voltage and end of charge current threshold. The charge current in the constant current mode is programmable and a maintenance mode monitors for battery voltage drop to restart charging at a preset level. A USB charging mode is also available with 2 charge current levels.

CHARGER FUNCTION

Following the correct detection of an input voltage at the charger pin the charger enters a pre-charge mode. In this mode a constant current of 50 mA is available to charge the battery to 3.0V. At this voltage level the charge management applies the default (100 mA) full rate constant current to raise the battery voltage to the termination voltage level (default 4.2V). The full rate charge current may be programmed to a different level at this stage. When termination voltage (V_{TERM}) is reached, the charger is in constant voltage mode and a constant voltage of 4.2V is maintained. This mode is complete when the end of charge current (default 0.1C) is detected and the charge management enters the maintenance mode. In maintenance mode the battery voltage is monitored for the restart level (4.05V at the default settings) and the charge cycle is re-initiated to re-establish the termination voltage level. For start up the EOC function is disabled. This function should be enabled once start up is complete and a battery has been detected. EOC is enabled via register CHGCNTL1, *Table 10*.

The full rate constant current rate of charge may be programmed to 19 levels from 50 mA to 950 mA. These values are given in *Table 5* and *Table 13*.

The charge mode may be programmed to USB mode when the charger input is applied and the battery voltage is above 3.0V. This provides two programmable current levels of 100 mA and 450 mA for a USB sourced supply input at CHG_IN. *Table 9*.

EOC

EOC is disabled by default and should be enabled when the system processor is awake and the system detects that a battery is present.

PROGRAMMING INFORMATION

TABLE 10. Register Address 8h'10: CHGCNTL1

BIT	NAME	FUNCTION
2	En_EOC	Enables the End Of Charge current level threshold detection. When set to '0' the EOC is disabled.

The **E**nd **O**f **C**harge current threshold default setting is at 0.1C. This EOC value is set relative to C the set full rate con-

stant current. This threshold can be set to 0.1C, 0.15C, 0.2C or 0.25C by changing the contents of the PROG_EOC[1:0] register bits.

TABLE 11. Register Address 8h'12: CHGCNTL3

BIT	NAME	FUNCTION
2	Prog_EOC[0]	Set the End Of Charge Current. See *Table 7*.
3	Prog_EOC[1]	

TERMINATION AND RESTART

The termination and restart voltage levels are determined by the data in the VTERM[1:0] and PROG_VSTRT[1:0] bits in the control register. The restart voltage is programmed relative to the selected termination voltage.

The Termination voltages available are 4.1V, 4.2V (default), 4.3V, and 4.4V.

The Restart voltages are determined relative to the termination voltage level and may be set to 50 mV, 100 mV, 150 mV (default), and 200 mV below the set termination voltage level.

TABLE 12. Register Address 8h'12: CHGCNTL3

BIT	NAME	FUNCTION
4	VTERM[0]	Set the charging termination voltage. See *Table 6*.
5	VTERM[1]	
0	VRSTR[0]	Set the charging restart voltage. See *Table 8*.
1	VRSTR[1]	

CHARGER FULL RATE CURRENT

Programming Information

TABLE 13. Register Address 8h'11: CHGCNTL2

Data BITs	HEX	NAME	FUNCTION
000**[00000]**	00	Prog_ICHG	50 mA
000**[00001]**	01		**100 mA**
000**[00010]**	02		150 mA
000**[00011]**	03		200 mA
000**[00100]**	04		250 mA
000**[00101]**	05		300 mA
000**[00110]**	06		350 mA
000**[00111]**	07		400 mA
000**[01000]**	08		450 mA
000**[01001]**	09		500 mA
000**[01010]**	0A		550 mA
000**[01011]**	0B		600 mA
000**[01100]**	0C		650 mA
000**[01101]**	0D		700 mA
000**[01110]**	0E		750 mA
000**[01111]**	0F		800 mA
000**[10000]**	10		850 mA
000**[10001]**	11		900 mA
000**[10010]**	12		950 mA

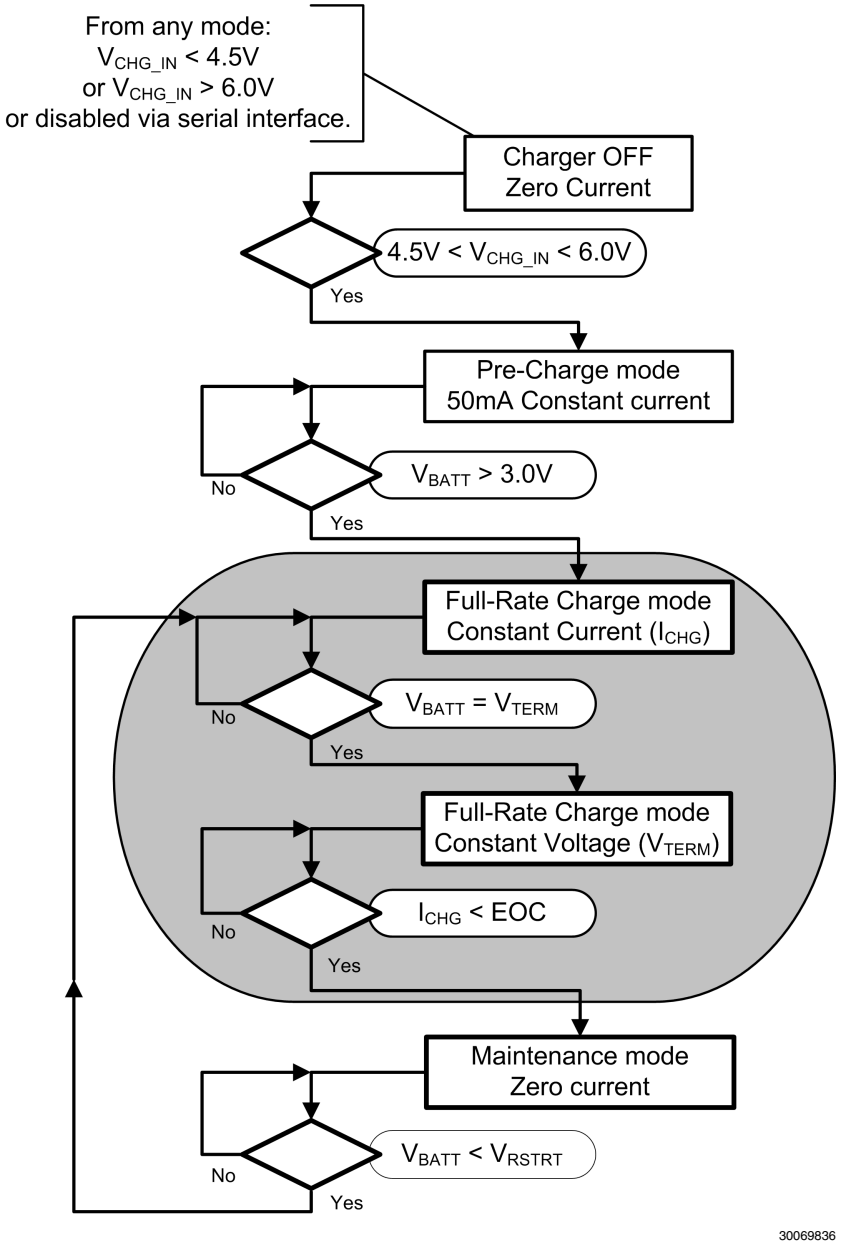


FIGURE 5. Simplified Charger Functional State Diagram (EOC is enabled)

The charger operation may be depicted by the following graphical representation of the voltage and current profiles.

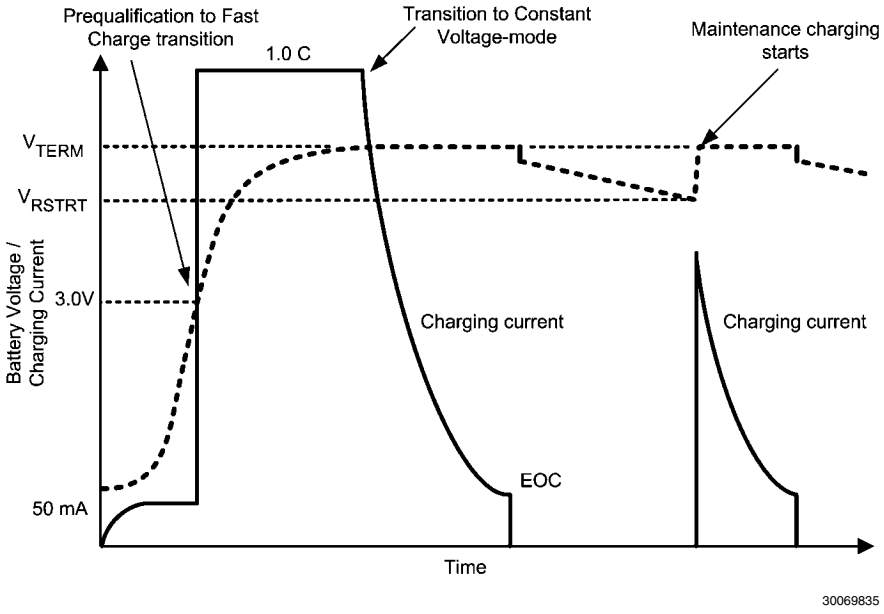


FIGURE 6. Charge Cycle Diagram

Further Charger Register Information

CHARGER CONTROL REGISTER 1

TABLE 14. Register Address 8h'10: CHGCNTL1

BIT	NAME	FUNCTION (if bit = '1')
7	USB_MODE _EN	Sets the Current Level in USB mode.
6	CHG_MODE _EN	Forces the charger into USB mode when active high. If low, charger is in normal charge mode.
5	FORCE _EOC	Forces an EOC event.
4	TOUT_ Doubling	Doubles the timeout delays for all timeout signals.
3	EN_Tout	Enables the timeout counters. When set to '0' the timeout counters are disabled.
2	EN_EOC	Enables the End of Charge current level threshold detection. When set to '0' the functions are disabled.
1	Set_ LDOmode	Forces the charger into LDO mode.
0	EN_CHG	Charger enable.

TABLE 15. Register Address 8h'13: CHGSTATUS1

BIT	NAME	FUNCTION (if bit = '1')
7	BAT_OVER _OUT	Is set when battery voltage exceeds 4.7V.
6	CHGIN_ OK_Out	Is set when a valid input voltage is detected at CHG_IN pin.
5	EOC	Is set when the charging current decreases below the programmed End Of Charge level.
4	Tout_ Fullrate	Set after timeout on full rate charge.
3	Tout_ Precharge	Set after timeout for precharge mode.
2	LDO_Mode	This bit is disabled in LP3921. Contact NSC sales if this option is required as in LP3918–L.
1	Fullrate	Set when the charger is in CC/CV mode.
0	PRECHG	Set during precharge.

Charger Status Register 2 Read only

TABLE 16. Register Address 8h'13: CHGSTATUS2

BIT	NAME	FUNCTION (if bit = '1')
1	Tout_ConstV	Set after timeout in CV phase.
0	BAD_BATT	Set at bad battery state.

IMON CHARGE CURRENT MONITOR

Charge current is monitored within the charger section and a proportional voltage representation of the charge current is presented at the IMON output pin. The output voltage relationship to the actual charge current is represented in the following graph and by the equation:

$$V_{IMON}(mV) = (2.47 \times I_{CHG})(mA)$$

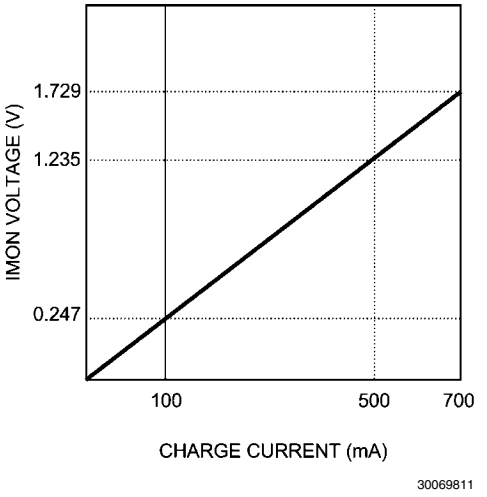


FIGURE 7. IMON Voltage vs. Charge Current

Note that this function is not available if there is no input at CHG_IN or if the charger is off due to the input at CHG_IN being less than the compliance voltage.

LDO Information

OPERATIONAL INFORMATION

The LP3921 has 7 LDO's of which 3 are enabled by default, LDO's 1,2 and 3 are powered up during the power up sequence. LDO's 4, 5 and 6 are separately, externally enabled and will follow LDO2 in start up if their respective enable pin is pulled high. LDO2, LDO3 and LDO7 can be enabled/disabled via the serial interface.

LDO2 must remain in regulation otherwise the device will power down. While LDO1 is enabled this must also be in regulation for the device to remain powered. If LDO1 is disabled via I²C interface the device will not shut down.

INPUT VOLTAGES

There are two input voltage pins used to power the 7 LDO's on the LP3921. $V_{IN2}$is the supply for LDO3, LDO4, LDO5, LDO6 and LDO7. $V_{IN1}$is the supply for LDO1 and LDO2.

PROGRAMMING INFORMATION

Enable via Serial Interface

TABLE 17. Register Address 8h'00: OP_EN

BIT	NAME	FUNCTION
0	LDO1_EN	Bit set to '0' - LDO disabled Bit set to '1' - LDO enabled
2	LDO3_EN	
3	LDO7_EN	

Note that the default setting for this Register is **[0000 0101]**. This shows that LDO1 and LDO3 are enabled by default whereas LDO7 is not enabled by default on start up.

TABLE 18. LDO Output Programming

Register Add (hex)	Name	Data Range (hex)	Output Voltage
01	LDO1PGM O/P	03 - 0F	1.5V to 3.3V (def. 1.8V)
02	LDO2PGM O/P	00 - 0F	2.5V to 3.3V (def 3.0V)
03	LDO3PGM O/P	05 - 0C	2.7V to 3.05V (def 3.0V)
04	LDO4PGM O/P	00 - 0F	1.5V to 3.3V (def 3.0V)
05	LDO5PGM O/P	05 - 0C	2.7V to 3.05V (def 3.0V)
06	LDO6PGM O/P	05 - 0C	2.7V to 3.05V (def 3.0V)
07	LDO7PGM O/P	00 - 0F	1.5V to 3.3V (def 3.0V)

See *Table 4* for full programmable range of values.

EXTERNAL CAPACITORS

The Low Drop Out Linear Voltage regulators on the LP3921 require external capacitors to ensure stable outputs. The LDO's on the LP3921 are specifically designed to use small surface mount ceramic capacitors which require minimum board space. These capacitors must be correctly selected for good performance

INPUT CAPACITOR

Input capacitors are required for correct operation. It is recommended that a 10 µF capacitor be connected between each of the voltage input pins and ground (this capacitance value may be increased without limit). This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analogue ground. A ceramic capacitor is recommended although a good quality tantalum or film capacitor may be used at the input.

Warning: **Important:** Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have surge current rating sufficient for the application. There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain within its operational range over the entire operating temperature range and conditions.

OUTPUT CAPACITOR

Correct selection of the output capacitor is critical to ensure stable operation in the intended application. The output capacitor must meet all the requirements specified in the recommended capacitor table over all conditions in the application. These conditions include DC-bias, frequency and temperature. Unstable operation will result if the capacitance drops below the minimum specified value.

The LP3921 is designed specifically to work with very small ceramic output capacitors. The LDO's on the LP3921 are specifically designed to be used with X7R and X5R type capacitors. With these capacitors selection of the capacitor for the application is dependant on the range of operating conditions and temperature range for that application. (See section on Capacitor Characteristics).

It is also recommended that the output capacitor be placed within 1 cm from the output pin and returned to a clean ground line.

CAPACITOR CHARACTERISTICS

The LDO's on the LP3921 are designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values around 1 µF, ceramic capacitors give the circuit designer the best design options in terms of low cost and minimal area.

Generally speaking, input and output capacitors require careful understanding of the capacitor specification to ensure stable and correct device operation. Capacitance value can vary with DC bias conditions as well as temperature and frequency of operation.

Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size with smaller sizes giving poorer performance figures in general.

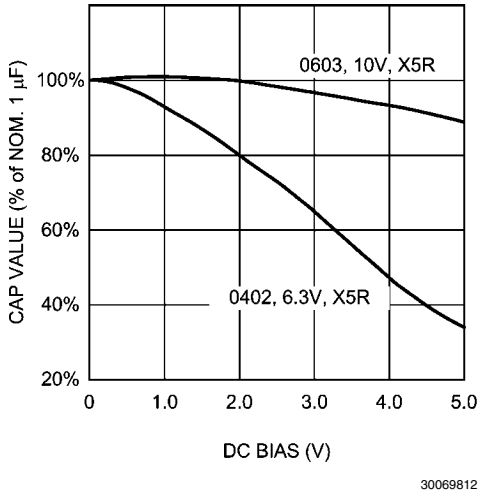


FIGURE 8. DC Bias (V)

As an example, *Figure 8* shows a typical graph showing a comparison of capacitor case sizes in a Capacitance vs DC Bias plot. As shown in the graph, as a result of DC Bias condition the capacitance value may drop below minimum capacitance value given in the recommended capacitor table (0.7 µF in this case). Note that the graph shows the capacitance out of spec for 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers specifications for the nominal value capacitor are consulted for all conditions as some capacitor sizes (e.g., 0402) may not be suitable in the actual application. Ceramic capacitors have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1 µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, and also meets the ESR requirements for stability. The temperature performance of ceramic capacitors varies by type. Capacitor type X7R is specified with a tolerance of ±15% over temperature range -55ºC to +125ºC. The X5R has similar tolerance over the reduced temperature range -55ºC to +85ºC. Most large value ceramic capacitors (<2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25ºC to 85ºC. Therefore X7R is recommended over these other capacitor types in applications

where the temperature will change significantly above or below 25ºC.

NO-LOAD STABILITY

The LDO's on the LP3921 will remain stable in regulation with no external load.

TABLE 19. LDO Output Capacitors Recommended Specification

Symbol	Parameter	Capacitor Type	Typ	Limit		Units
				Min	Max	
$C_{o(LDO1)}$	Capacitance	X5R. X74	1.0	0.7	2.2	µF
$C_{o(LDO2)}$	Capacitance	X5R. X74	1.0	0.7	2.2	µF
$C_{o(LDO3)}$	Capacitance	X5R. X74	1.0	0.7	2.2	µF
$C_{o(LDO4)}$	Capacitance	X5R. X74	1.0	0.7	2.2	µF
$C_{o(LDO5)}$	Capacitance	X5R. X74	1.0	0.7	2.2	µF
$C_{o(LDO6)}$	Capacitance	X5R. X74	1.0	0.7	2.2	µF
$C_{o(LDO7)}$	Capacitance	X5R. X74	1.0	0.7	2.2	µF

Note: The capacitor tolerance should be 30% or better over the full temperature range. X7R or X5R capacitors should be used. These specifications are given to ensure that the capacitance remains within these values over all conditions within the application. See Capacitor Characteristics section in Application Information.

Thermal Shutdown

The LP3921 has internal limiting for high on-chip temperatures caused by high power dissipation etc. This Thermal Shutdown, TSD, function monitors the temperature with respect to a threshold and results in a device power-down.

If the threshold of +160°C has been exceeded then the device will power down. Recovery from this TSD event can only be initiated after the chip has cooled below +115°C. This device recovery is controlled by the APU_TSD_EN bit (bit 1) in control register MISC, 8h'1C. **See *Table 21*.** If the APU_TSD_EN is set low then the device will shutdown requiring a new start up event initiated by PWR_ON, HF_PWR, or CHG_IN. If APU_TSD_EN is set high then the device will power up automatically when the shutdown condition clears. In this case the control register settings are preserved for the device restart.

The threshold temperature for the device to clear this TSD event is 115°C. This threshold applies for any start up thus the device temperature must be below this threshold to allow a start up event to initiate power up.

Further Register Information

STATUS REGISTER READ ONLY

TABLE 20. Register Address 8h'0C: Status

Bit	Name	Function (if bit = '1')
7	PWR_ON_TRIG	PMU startup is initiated by PWR_ON.
6	HF-PWR-TRIG	PMU startup is initiated by PWR_TRIG.
5	CHG_IN_TRIG	PMU startup is initiated by CHG_IN.

Bits <4...0> are not used.

MISC CONTROL REGISTER

TABLE 21. Register Address 8h'1C: Misc.

Bit	Name	Function (if bit = '1')
1	APU_TSD_EN	1b'0: Device will shut down completely if thermal shutdown occurs. Requires a new startup event to restart the PMU. 1b'1: Device will start up automatically after thermal shutdown condition is removed. (Device tries to keep its internal state.)
0	PWR_HOLD_DELAY	1b'0: If PWR_HOLD is low for 35 ms, the device will shutdown. (Default) 1b'1: If PWR_HOLD is low for 350 ms, the device will shut down.

Bits <7...2> are not used.

Differential Amplifier Explanation

TABLE 22. Register Address 8h'19 Audio_Amp

Bit	Name	Function (if the powerup default is "amplifier disabled")
0	amp_en	Bit set to '0' - amplifier disabled Bit set to '1' - amplifier enabled

The LP3921 contains a fully differential audio amplifier that features differential input and output stages. Internally this is accomplished by two circuits: a differential amplifier and a common mode feedback amplifier that adjusts the output voltages so that the average value remains VDD/2. When setting the differential gain, the amplifier can be considered to have "halves". Each half uses an input and feedback resistor (Ri1 and RF1) to set its respective closed-loop gain. (See *Figure 9*.) With Ri1 = Ri2 and RF1 = RF2, the gain is set at -RF / Ri for each half. This results in a differential gain of:

$$AVD = -RF/Ri \quad (1)$$

It is extremely important to match the input resistors to each other, as well as the feedback resistors to each other for best amplifier performance. A differential amplifier works in a manner where the difference between the two input signals is amplified. In most applications, this would require input sig-

nals that are 180° out of phase with each other. The LP3921 can be used, however, as a single ended input amplifier while still retaining its fully differential benefits. In fact, completely unrelated signals may be placed on the input pins. The LP3921 simply amplifies the difference between them.

A bridged configuration, such as the one used in the LP3921, also creates a second advantage over single ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This assumes that the input resistor pair and the feedback resistor pair are properly matched. BTL configuration eliminates the output coupling capacitor required in single supply, single-ended amplifier configurations. If an output coupling capacitor is not used in a single-ended output configuration, the half-supply bias across the load would result in both increased internal IC power dissipation as well as permanent loudspeaker damage. Further advantages of bridged mode operation specific to fully differential amplifiers like the LP3921 include increased power supply rejection ratio, common-mode noise reduction, and click and pop reduction.

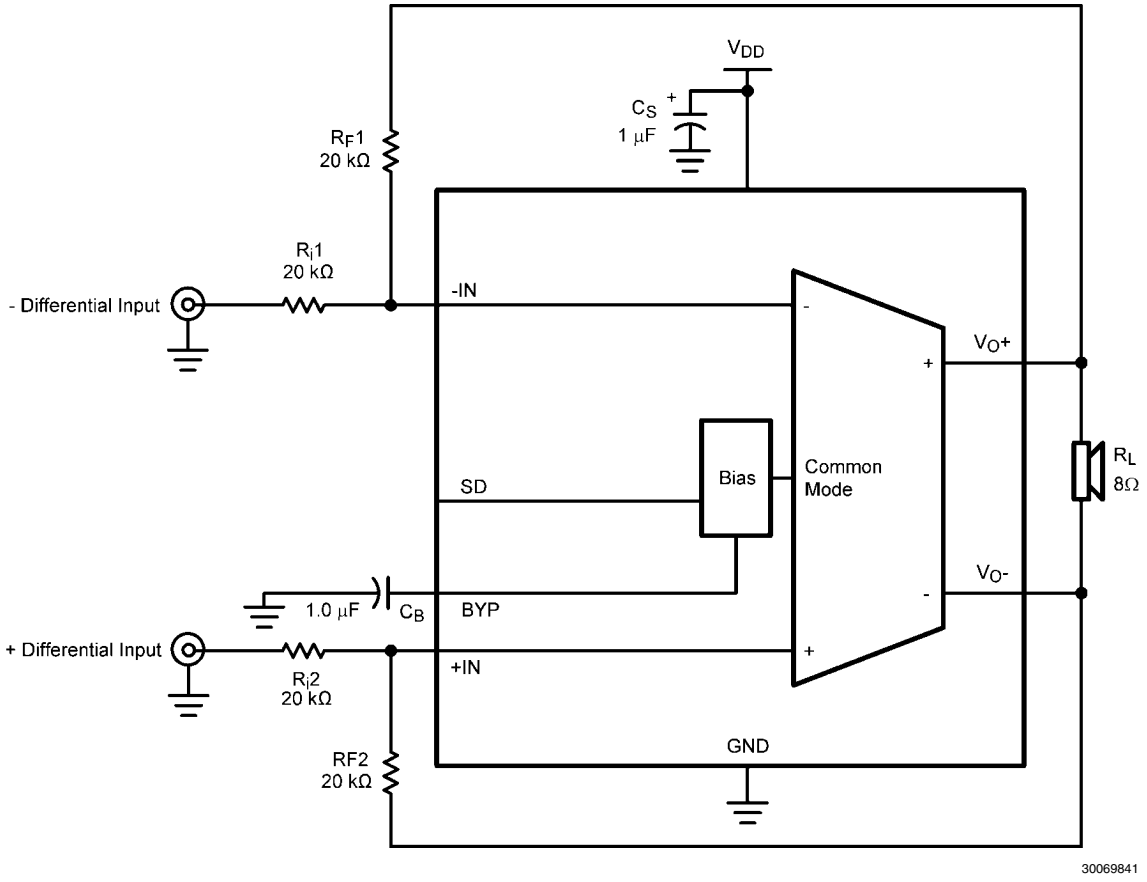


FIGURE 9. Audio Block

EXPOSED-DAP PACKAGE MOUNTING CONSIDERATIONS

The LP3921's exposed-DAP (die attach paddle) package (LLP) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. this allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air. Failing to optimize thermal design may compromise the LP3921's high-power performance and activate unwanted, though necessary, thermal shutdown protection. The LLP package must have its DAP soldered to a copper pad on the PCB> The DAP's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass and heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers. Connect the DAP copper pad to the inner layer or backside copper heat sink area with a thermal via. The via diameter should be 0.012 in. to 0.013 in. Ensure efficient thermal conductivity by plating-through and solder-filling the vias.

Best thermal performance is achieved with the largest practical copper heat sink area. In all circumstances and conditions, the junction temperature must be held below 150°C to prevent activating the LP3921's thermal shutdown protection. Further detailed and specific information concerning PCB layout, fabrication, and mounting an LLP package is available from National Semiconductor's package Engineering Group under application note AN1187.

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power

dissipated in the trace and not in the load as desired. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

POWER DISSIPATION

Power dissipation might be a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \text{ Single-Ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation versus a single-ended amplifier operating at the same conditions.

$$P_{DMAX} = 4 * (V_{DD})^2 / (2\pi^2 R_L) \text{ Bridge Mode} \quad (3)$$

Since the LP3921 has bridged outputs, the maximum internal power dissipation is 4 times that of a single-ended amplifier. Even with this substantial increase in power dissipation, the LP3921 does not require additional heat sinking under most operating conditions and output loading. From Equation 3, assuming a 5V power supply and an 8Ω load, the maximum power dissipation contribution from the audio amplifier is 625 mW. To this must be added the power dissipated from the power management blocks. The maximum power dissipation thus obtained (P_{TOT}) must not be greater than the power dissipation results from Equation 4:

$$P_{TOT} = P_{PDMU} + P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \quad (4)$$

P_{DPMU} is mainly the sum of power dissipated in the charger and LDO blocks as shown in Equation 5:

$$P_{DPMU} = I_{CHG} (V_{CHG\_IN} - V_{BATT}) + (I_{OUT1} (V_{BATT} - V_{OUT1}) + (I_{OUT2} (V_{BATT} - V_{OUT2}) + (I_{OUT3} (V_{BATT} - V_{OUT3}) + \ldots \text{ (approx.)} \quad (5)$$

The LP3921's θ_{JA} in an SQA32A package is 30°C/W. Depending on the ambient temperature, T_A, of the system surroundings, Equation 4 can be used to find the maximum internal power dissipation supported by the IC packaging.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection ratio (PSRR). The capacitor location on both the bypass and power supply pins should be as close to the device as possible. A larger half-supply bypass capacitor improves PSRR because it increases half-supply stability. Typical applications employ a 5V regulator with 10 µF and 0.1 µF bypass capacitors that increase supply stability. This, however, does not eliminate the need for bypassing the supply nodes of the LP3921. The LP3921 will operate without the bypass capacitor C_B, although the PSRR may decrease. A 1 µF capacitor is recommended for C_B. This value maximizes PSRR performance. Lesser values may be used, but PSRR decreases at frequencies below 1 kHz. The issue of C_B selection is thus dependant upon desired PSRR and click and pop performance as explained in the section **Proper Selection of External Components**.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the audio amplifier can be shut down by setting amp_en to 0 in the Audio_Amp register. On power-up, the audio amplifier is in shut down until enabled. (Contact NSC sales for a different option.) (See *Table 22*.)

Thermal shutdown of the PMU will shut down the audio amplifier. (See Thermal Shutdown for recovery options.) Independent temperature sensing within the audio amplifier may also shut down the audio amplifier alone, without affecting PMU control logic.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical when optimizing device and system performance. Although the LP3921 is tolerant to a variety of external component combinations, consideration of component values must be made when maximizing overall system quality.

The LP3921 is unity-gain stable, giving the designer maximum system flexibility. The LP3921 should be used in low closed-loop gain configurations to minimize THD+N values and maximize signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1 Vrms are available from sources such as audio codecs. Please refer to the Audio Power Amplifier Design section for a more complete explanation of proper gain selection. When used in its typical application as a fully differential power amplifier the LP3921 does not require input coupling capacitors for input sources with DC common-mode voltages of less than V_{DD}. Exact allowable input common-mode voltage levels are actually a function of V_{DD}, R_i, and R_f and may be determined by Equation 5:

$$V_{CMi} < (V_{DD}-1.2)*((R_f+(R_i)/(R_f)-V_{DD}*(R_i / 2R_f) \quad (6)$$

$$-R_F / R_I = A_{VD} \quad (7)$$

Special care must be taken to match the values of the feedback resistors (R_{F1} and R_{F2}) to each other as well as matching the input resistors (R_{i1} and R_{i2}) to each other (see *Figure 9*) more in front. Because of the balanced nature of differential amplifiers, resistor matching differences can result in net DC currents across the load. This DC current can increase power consumption, internal IC power dissipation, reduce PSRR, and possibly damaging the loudspeaker. *Table 23* demonstrates this problem by showing the effects of differing values between the feedback resistors while assuming that the input resistors are perfectly matched. The results below apply to the application circuit shown in *Figure 9*, and assumes that

V_{DD} = 5V, R_L = 8Ω, and the system has DC coupled inputs tied to ground.

TABLE 23. Feedback Resistor Mis-match

Tolerance	R_{F1}	R_{F2}	V_{02} - V_{01}	I_{LOAD}
20%	0.8R	1.2R	-0.500V	62.5 mA
10%	0.9R	1.1R	-0.250V	31.25 mA
5%	0.95R	1.05R	-0.125V	15.63 mA
1%	0.99R	1.01R	-0.025V	3.125 mA
0%	R	R	0	0

Similar results would occur if the input resistors were not carefully matched. Adding input coupling capacitors in between the signal source and the input resistors will eliminate this problem, however, to achieve best performance with minimum component count it is highly recommended that both the feedback and input resistors matched to 1% tolerance or better.

AUDIO POWER AMPLIFIER DESIGN

Design a 1W/8Ω Audio Amplifier

Given:

Power Output	1 Wrms
Load Impedance	8Ω
Input Level	1 Vrms
Input Impedance	20 kΩ
Bandwidth	100 Hz–20 kHz ± 0.25 dB

A designer must first determine the minimum supply rail to obtain the specified output power. The supply rail can easily be found by extrapolating from the Output Power vs Supply Voltage graphs in the **Typical Performance Characteristics** section. A second way to determine the minimum supply rail is to calculate the required V_{OPEAK} using Equation 8 and add the dropout voltages. Using this method, the minimum supply voltage is (V_{OPEAK} + ($V_{DO\ TOP}$ + ($V_{DO\ BOT}$)), where $V_{DO\ BOT}$ and $V_{DO\ TOP}$ are extrapolated from the Dropout Voltage vs Supply Voltage curve in the **Typical Performance Characteristics** section.

$$V_{opeak} = \sqrt{(2R_L P_O)} \quad (8)$$

Using the Output Power vs. Supply Voltage graph for an 8Ω load, the minimum supply rail just about 5V. Extra supply voltage creates headroom that allows the LP3921 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section. Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 9.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (9)$$

$$R_f / R_i = A_{VD} \quad (10)$$

From Equation 10, the minimum A_{VD} is 2.83. Since the desired input impedance was 20 kΩ, a ratio of 2.83:1 of R_f to R_i results in an allocation of R_i = 20 kΩ for both input resistors and R_f = 60 kΩ for both feedback resistors. The final design step is to address the bandwidth requirement which must be stated as a single -3 dB frequency point. Five times away from a -3 dB point is 0.17 dB down from pass band response which is better than the required ±0.25 dB specified.

$$f_H = 20\ kHz * 5 = 100\ kHz \quad (11)$$

The high frequency pole is determined by the product of the desired frequency pole, f_H , and the differential gain, A_{VD}. With A_{VD} = 2.83 and f_H = 100 kHz, the resulting GBWP = 150 kHz which is much smaller than the LP3921 GBWP of 10 MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the LP3921 can still be used without running into bandwidth limitations.

I²C Compatible Serial Bus Interface

INTERFACE BUS OVERVIEW

The I²C compatible synchronous serial interface provides access to the programmable functions and registers on the device.

This protocol uses a two-wire interface for bi-directional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). These lines should be connected to a positive supply, via a pull-up resistor of 1.5 kΩ, and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock (SCL).

DATA TRANSACTIONS

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

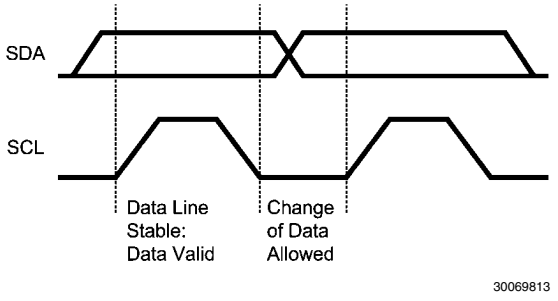


FIGURE 10. Bit Transfer

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

START AND STOP

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCL is high indicates a Stop Condition.

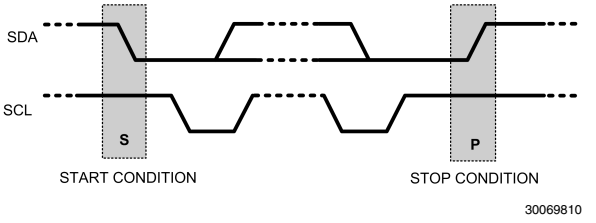


FIGURE 11. Start and Stop Conditions

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

ACKNOWLEDGE CYCLE

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

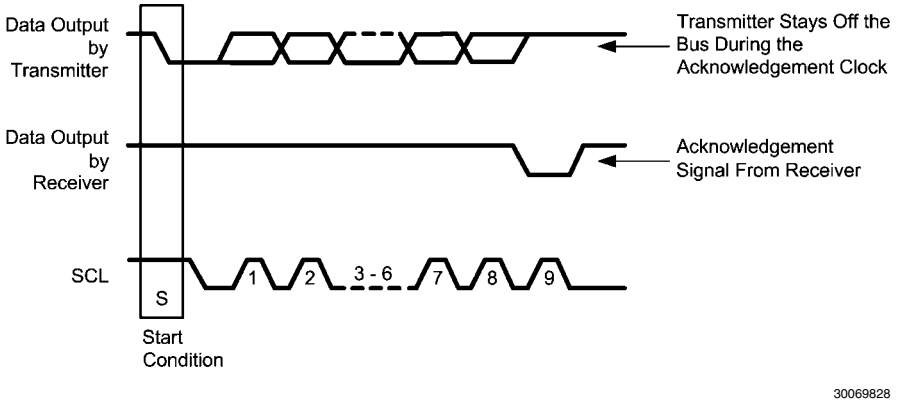


FIGURE 12. Bus Acknowledge Cycle

"ACKNOWLEDGE AFTER EVERY BYTE" RULE

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the "acknowledge after every byte" rule.

When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging ("negative acknowledge") the last byte clocked out of the slave. This "negative acknowledge" still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

ADDRESSING TRANSFER FORMATS

Each device on the bus has a unique slave address. The LP3921 operates as a slave device with the address 7h'7E (binary 1111110). Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.

CONTROL REGISTER WRITE CYCLE

- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (R/W = "0").
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes the control register address will be incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

CONTROL REGISTER READ CYCLE

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (R/W = "0").
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (R/W = "1").
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

TABLE 24. I²C Read/Write Sequences

	Address Mode
Data Read	<Start Condition> <Slave Address><r/w = '0'>[Ack] <Register Addr.>[Ack] <Repeated Start Condition> <Slave Address><r/w = '1'>[Ack] [Register Date]<Ack or nAck> … additional reads from subsequent register address possible <Stop Condition>
Data Write	<Start Condition> <Slave Address><r/w = '0'>[Ack] <Register Addr.>[Ack] <Register Data>[Ack] … additional writes to subsequent register address possible <Stop Condition>

< > Data from master [ ] Data from slave

REGISTER READ AND WRITE DETAIL

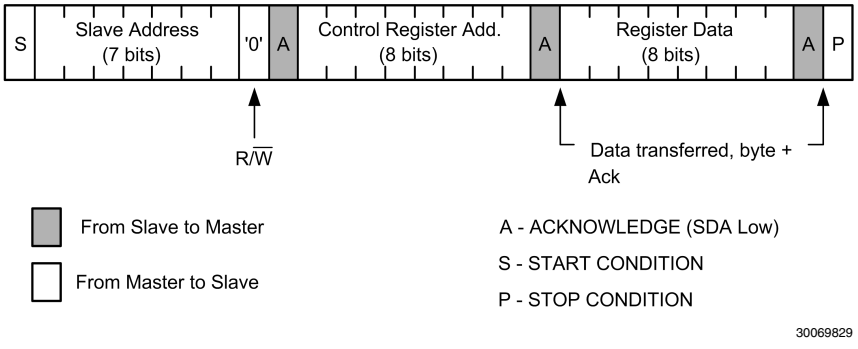


FIGURE 13. Register Write Format

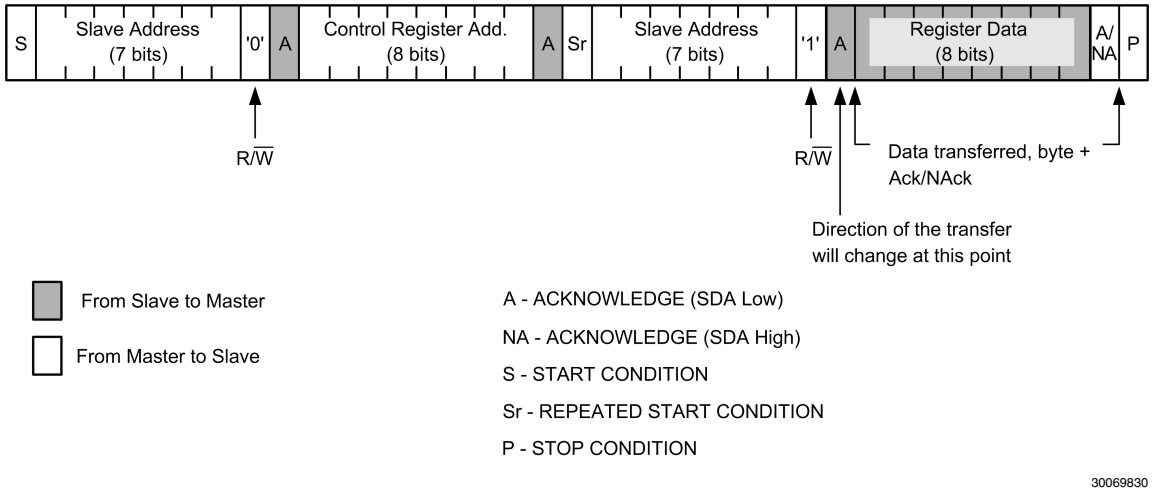
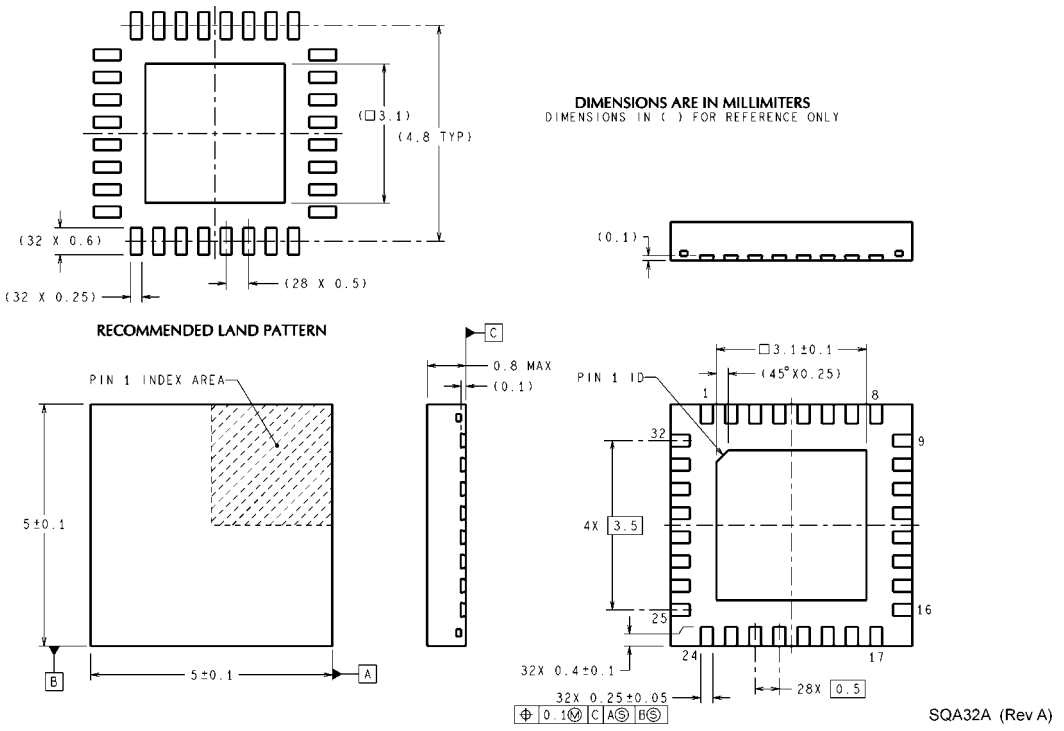


FIGURE 14. Register Read Format

Physical Dimensions inches (millimeters) unless otherwise noted



32–pin LLP Package
NS Package Number MKT-SQA32A

Notes

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH	www.national.com/webench
Audio	www.national.com/audio	Analog University	www.national.com/AU
Clock Conditioners	www.national.com/timing	App Notes	www.national.com/appnotes
Data Converters	www.national.com/adc	Distributors	www.national.com/contacts
Displays	www.national.com/displays	Green Compliance	www.national.com/quality/green
Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
LVDS	www.national.com/lvds	Reference Designs	www.national.com/refdesigns
Power Management	www.national.com/power	Feedback	www.national.com/feedback
Switching Regulators	www.national.com/switchers		
LDOs	www.national.com/ldo		
LED Lighting	www.national.com/led		
PowerWise	www.national.com/powerwise		
Serial Digital Interface (SDI)	www.national.com/sdi		
Temperature Sensors	www.national.com/tempsensors		
Wireless (PLL/VCO)	www.national.com/wireless		

National Semiconductor Americas Technical Support Center
Email: support@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center
Email: europe.support@nsc.com
German Tel: +49 (0) 180 5010 771
English Tel: +44 (0) 870 850 4288

National Semiconductor Asia Pacific Technical Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Technical Support Center
Email: jpn.feedback@nsc.com