LP3933 Lighting Management System for Six White LEDs and Two RGB or FLASH LEDs

Check for Samples: LP3933

FEATURES

- **High Efficiency Programmable 300 mA Magnetic Boost DC-DC converter**
- **2 separately controlled PWM RGB LED drivers with programmable color, brightness, turn on/off slopes and blinking patterns**
- **FLASH function with up to 6 outputs, each up to 120 mA**
- **4 constant current LED drivers with programmable 8-bit adjustment (0 … 25 mA/LED)**
- **2 constant current LED drivers with programmable 8-bit adjustment (0 … 25 mA/LED)**
- **Functions software controlled through SPI interface**
- **Additional LED on/off and dimming hardware control**
- **Programmable low current Standby mode**
- **Low voltage digital interface down to 1.8V**
- **Space efficient 32-pin thin CSP laminate package**

APPLICATIONS

- **Cellular Phones**
- **PDAs**

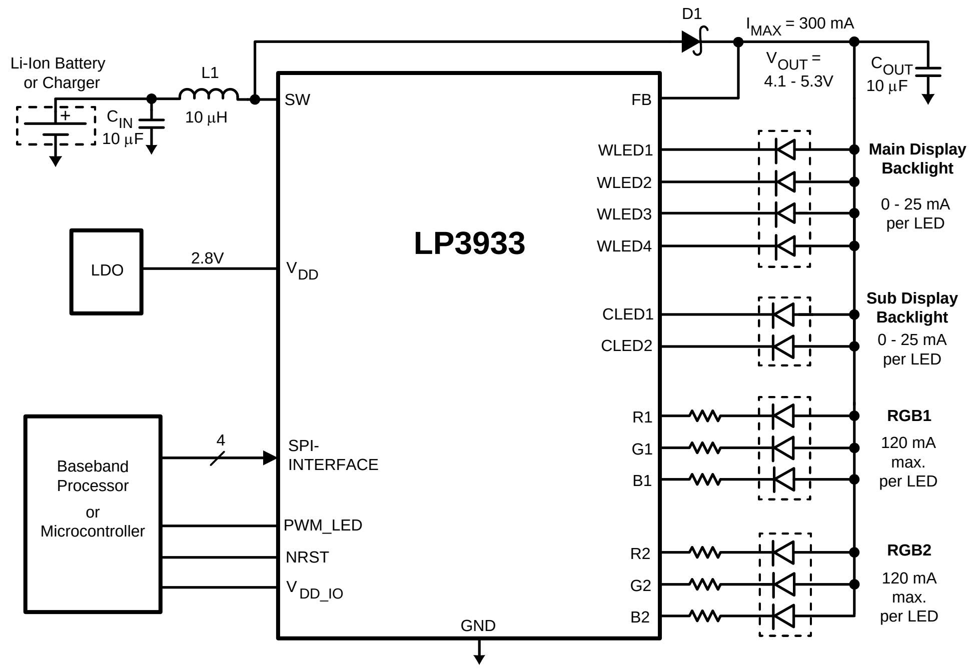
DESCRIPTION

The LP3933 is a complete lighting management system designed for portable wireless applications. It contains a boost DC/DC converter, 4 white-LED drivers to drive the main LCD panel backlight, 2 white-LED drivers for the sub-LCD panel and two sets of RGB/FLASH LED drivers.

Both backlight drivers have 8-bit constant current drivers that are separately adjustable and matched to 0.5% (typ.). The RGB LED drivers are PWM-driven with programmable color, intensity and blinking patterns. In addition, they feature a FLASH function to support picture taking with camera-enabled cellular phones.

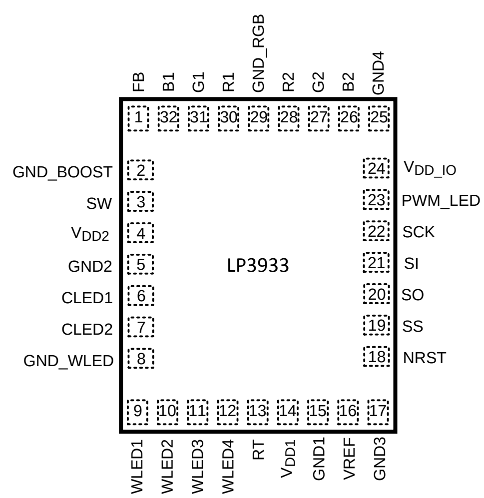
An efficient magnetic boost DC/DC converter provides the required bias for LEDs, operating from a single Li-Ion battery. The DC/DC converter output voltage is user programmable from 4.1V to 5.3V for adapting to different LED types and for efficiency optimization. All functions are software controllable through a SPI interface and 19 internal registers.

Typical Application

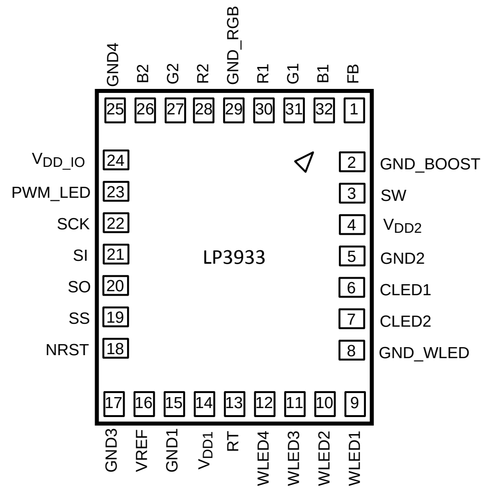


Connection Diagrams and Package Mark Information

32-Lead Thin CSP Package, 4.5 x 5.5 x 0.8 mm, 0.5 mm pitch: Package Number SLE32A



TOP VIEW



BOTTOM VIEW

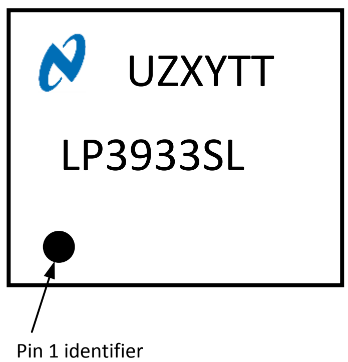


Figure 1. Package Mark—TOP VIEW

Note: The actual physical placement of the package marking will vary from part to part. The package marking “XY” designates the date code. “UZ” and “TT” are NSC internal codes for die manufacturing and assembly traceability. Both will vary considerably.

Table 1. Ordering Information(1.8V ≤ V_{DD_IO} ≤ $V_{DD1,2}$)

Order Number	Package Marking	Supplied As
LP3933SL	LP3933SL	1000 units, Tape-and-Reel
LP3933SLX	LP3933SL	2500 units, Tape-and-Reel

Table 2. Pin Description(1.8V ≤ V_{DD_IO} ≤ $V_{DD1,2}$)

Pin #	Name	Type	Description
1	FB	Input	Boost Converter Feedback
2	GND_BOOST	Ground	Power Switch Ground
3	SW	Output	Open Drain, Boost Converter Power Switch
4	V_{DD2}	Power	Supply Voltage for Internal Digital Circuits
5	GND2	Ground	Ground Return for V_{DD2} (Internal Digital)
6	CLED1	Output	Open Drain, CLED1 Output
7	CLED2	Output	Open Drain, CLED2 Output
8	GND_WLED	Ground	Ground for WLED and CLED Drivers

Table 2. Pin Description(1.8V ≤ V_{DD_IO} ≤ $V_{DD1,2}$) (continued)

Pin #	Name	Type	Description
9	WLED1	Output	Open Drain, White LED1 Output
10	WLED2	Output	Open Drain, White LED2 Output
11	WLED3	Output	Open Drain, White LED3 Output
12	WLED4	Output	Open Drain, White LED4 Output
13	RT	Input	Oscillator Resistor
14	V_{DD1}	Power	Supply Voltage for Internal Analog Circuits
15	GND1	Ground	Ground
16	V_{REF}	Output	Internal Reference Bypass Capacitor
17	GND3	Ground	Ground
18	NRST	Logic Input	Low Active Reset Input
19	SS	Logic Input	SPI Slave Select
20	SO	Logic Output	SPI Serial Data Output
21	SI	Logic Input	SPI Serial Data Input
22	SCK	Logic Input	SPI Clock
23	PWM_LED	Logic Input	LED Control for On/Off or Dimming Control
24	V_{DD_IO}	Power	Supply Voltage for Logic IO Signals
25	GND4	Ground	Ground
26	B2	Output	Open Drain Output, Blue LED 2
27	G2	Output	Open Drain Output, Green LED 2
28	R2	Output	Open Drain Output, Red LED 2
29	GND_RGB	Ground	RGB Driver Ground
30	R1	Output	Open Drain Output, Red LED 1
31	G1	Output	Open Drain Output, Green LED 1
32	B1	Output	Open Drain Output, Blue LED 1

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1] [2] ($1.8V \leq V_{DD\_IO} \leq V_{DD1,2}$)

V (SW, FB, WLED1-4, CLED1-2, R1-2, G1-2, B1-2) pins: Voltage to GND [3] [4]	−0.3V to +7.2V
V_{DD1}, V_{DD2}, V_{DD_IO}	−0.3V to +6.0V
Voltage on Logic Pins	-0.3V to V_{DD_IO} + 0.3V, with 6.0V max
I (R1, G1, B1, R2, G2, B2) [5]	150 mA
I (V_{REF})	10 µA
Continuous Power Dissipation [6]	Internally Limited
Junction Temperature (T_{J-MAX})	125°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Reflow soldering, 3 times) [7]	260°C
ESD Rating [8] [9]	
Human Body Model:	2 kV
Machine Model:	200V

(1) All voltages are with respect to the potential at the GND pins (GND1-4, GND_BOOST, GND_WLED, GND_RGB).
(2) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(3) Battery/Charger voltage should be above 6V no more than 10% of the operational lifetime.
(4) Voltage tolerance of LP3933 above 6.0V relies on fact that V_{DD1} and V_{DD2} (2.775V) are available (ON) at all conditions. If V_{DD1} and V_{DD2} are not available (ON) at all conditions, National Semiconductor does not guarantee any parameters or reliability for this device.
(5) The total load current of the boost converter should be limited to 300 mA.
(6) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 160°C (typ.) and disengages at T_J = 140°C (typ.).
(7) For detailed soldering specifications and information, please refer to National Semiconductor Application Note 1125: Laminate CSP/FBGA.
(8) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7
(9) ESD susceptibility for pin 11 and 12 is 500V for the human body model and 150V for the machine model.

Operating Ratings [1] [2] ($1.8V \leq V_{DD\_IO} \leq V_{DD1,2}$)

V (SW, FB, WLED1-4, CLED1-2, R1-2, G1-2, B1-2)	3.0V to 6.0V
V_{DD1}, V_{DD2} [3]	2.65 to 2.9V
V_{DD_IO}	1.8V to $V_{DD1,2}$
Recommended Load Current	0 mA to 300 mA
Junction Temperature (T_J) Range	−40°C to +125°C
Ambient Temperature (T_A) Range [4]	−40°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins (GND1-4, GND_BOOST, GND_WLED, GND_RGB).
(3) Voltage tolerance of LP3933 above 6.0V relies on fact that V_{DD1} and V_{DD2} (2.775V) are available (ON) at all conditions. If V_{DD1} and V_{DD2} are not available (ON) at all conditions, National Semiconductor does not guarantee any parameters or reliability for this device.
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Table 3. Thermal Properties($1.8V \leq V_{DD\_IO} \leq V_{DD1,2}$)

Junction-to-Ambient Thermal Resistance (θ_{JA}),	
SLE32A Package [1]	72°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

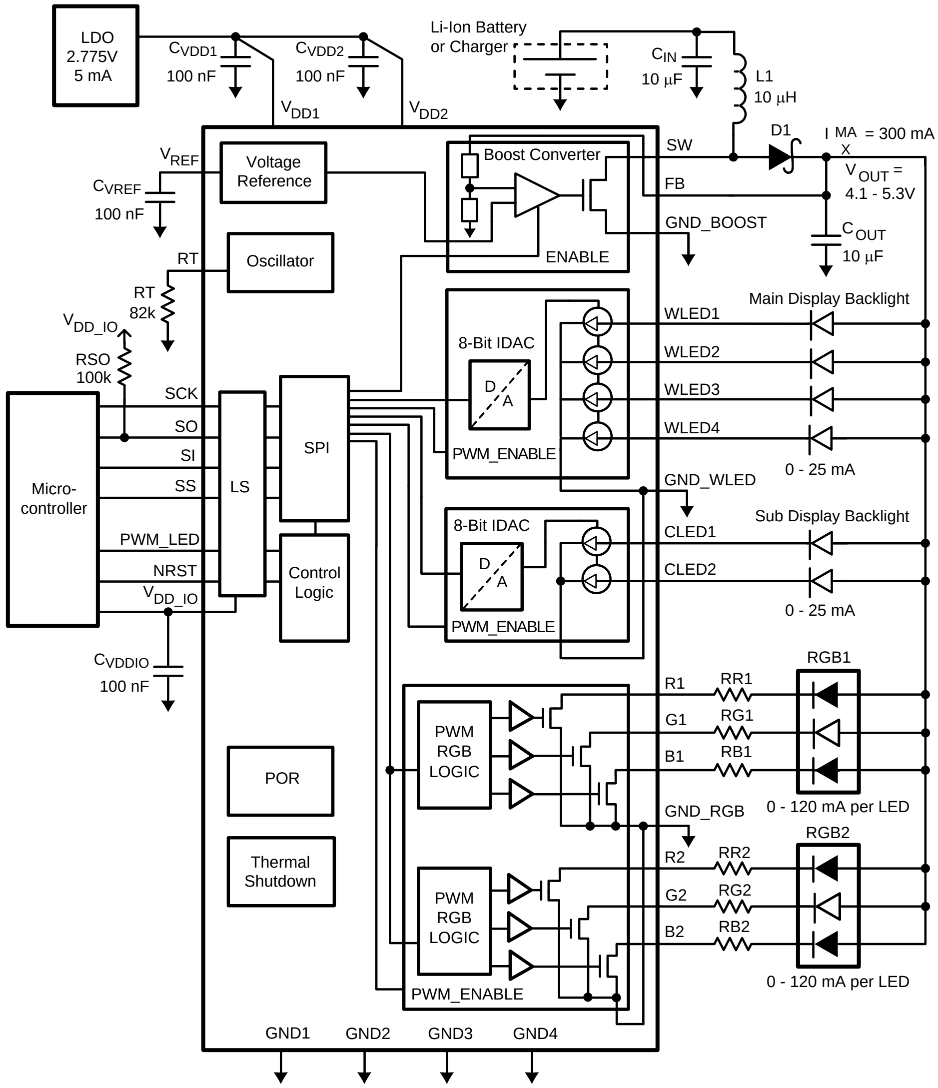
Electrical Characteristics [1] [2] ($1.8V \leq V_{DD\_IO} \leq V_{DD1,2}$)

Limits in standard typeface are for T_J = 25°C. Limits in **boldface** type apply over the operating ambient temperature range (−40°C ≤ T_A ≤ +85°C). Unless otherwise noted, specifications apply to the LP3933 Functional Block Diagram (pg. 5) with: $V_{DD1} = V_{DD2}$ = 2.775V, $C_{VDD1} = C_{VDD2} = C_{VDDIO}$ = 0.1 µF, $C_{OUT} = C_{IN}$ = 10 µF, C_{VREF} = 0.1 µF, L_1 = 10 µH [3].

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DD}	Standby Supply Current (V_{DD1} and V_{DD2} current)	NSTBY = L (register) SCK, SS, SI, NRST = H		1	**5**	µA
	No-Load Supply Current (V_{DD1} and V_{DD2} current, boost off)	NSTBY = H (reg.) EN_BOOST = L (reg.) SCK, SS, SI, NRST = H		170	**300**	µA
	Full Load Supply Current (V_{DD1} and V_{DD2} current, boost on)	NSTBY = H (reg.) EN_BOOST = H (reg.) SCK, SS, SI, NRST = H All Outputs Active		1		mA
I_{DD_IO}	V_{DD_IO} Standby Supply Current	NSTBY = L (register) SCK, SS, SI, NRST = H		1	**5**	µA
	V_{DD_IO} Operating Supply Current	1 MHz Clock Frequency C_L = 50 pF at SO pin		20		µA
V_{REF}	Reference Voltage [4]	$I(V_{REF}) \leq 1$ nA, Test Purposes Only	**1.205** **−2**	1.23	**1.255** **+2**	V %

(1) All voltages are with respect to the potential at the GND pins (GND1-4, GND_BOOST, GND_WLED, GND_RGB).
(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.
(3) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(4) V_{REF} pin (Bandgap reference output) is for internal use only. A capacitor should always be placed between V_{REF} and GND1.

Block Diagram(1.8V ≤ V_{DD_IO} ≤ $V_{DD1,2}$)



Modes of Operation(1.8V ≤ V_{DD_IO} ≤ $V_{DD1,2}$)

RESET: In the RESET mode all the internal registers are reset to the default values (Boost output register 3Fh (5.0V), all other registers 00h). Reset is entered always if input NRST is LOW or internal Power On Reset is active.

STANDBY: The STANDBY mode is entered if the register bit NSTBY is LOW and Reset is not active. This is the low power consumption mode, when all circuit functions are disabled. Registers can be written in this mode and the control bits are effective immediately after start up.

STARTUP: INTERNAL STARTUP SEQUENCE powers up all the needed internal blocks (V_{REF}, Bias, Oscillator etc.). To ensure the correct oscillator initialization, a 10 ms delay is generated by the internal state-machine. Thermal shutdown (THSD) disables the chip operation and Startup mode is entered until *no* thermal shutdown event is present.

BOOST STARTUP: Soft start for boost output is generated in the BOOST STARTUP mode. In this mode the boost output is raised in PFM mode during the 10 ms delay generated by the state-machine. The Boost startup is entered from Internal Startup Sequence if EN_BOOST is HIGH or from Normal mode when EN_BOOST is written HIGH.

NORMAL: During NORMAL mode the user controls the chip using the *Control Registers*. The registers can be written in any sequence and any number of bits can be altered in a register in one write.

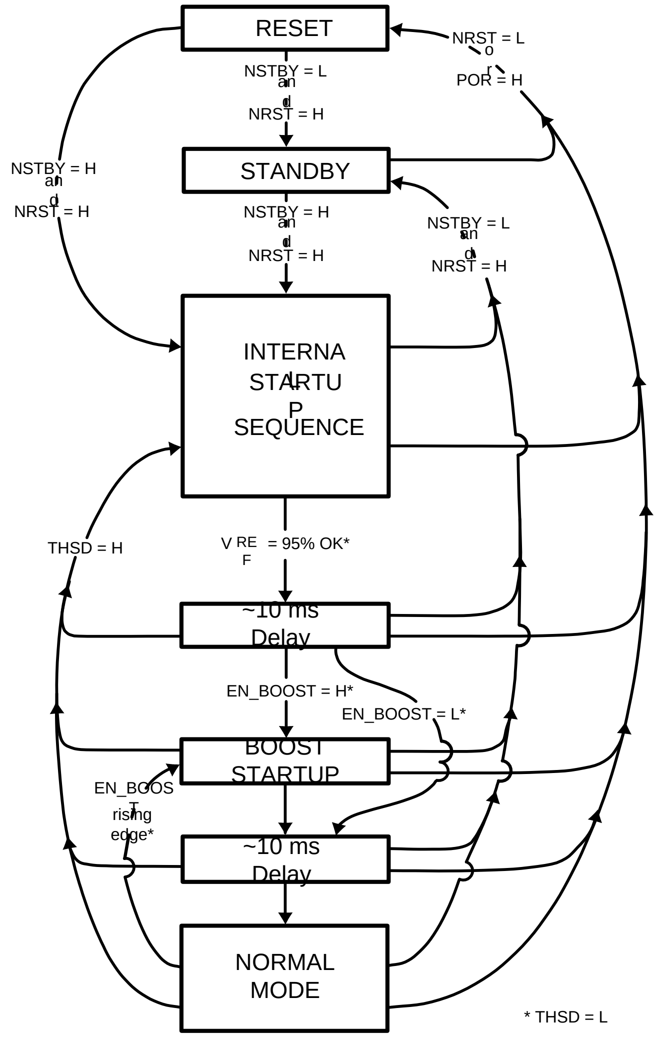


Table 4. Logic Interface Characteristics($1.8V \le V_{DD\_IO} \le V_{DD1,2}$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LOGIC INPUTS SS, SI, SCK, PWM_LED						
V_{IL}	Input Low Level				**0.5**	V
V_{IH}	Input High Level		**V_{DD_IO} − 0.5**			V
I_I	Logic Input Current		**−1.0**		**1.0**	µA
f_{SCK}	Clock Frequency	V_{DD_IO} = 2.775V			**13**	MHz
LOGIC INPUT NRST						
V_{IL}	Input Low Level				**0.5**	V
V_{IH}	Input High Level		**1.5**			V
I_I	Logic Input Current		**−1.0**		**1.0**	µA
t_{NRST}	Reset Pulse Width		10			µs
LOGIC OUTPUT SO						
V_{OL}	Output Low Level	I_{SO} = 3 mA		0.3	**0.5**	V
V_{OH}	Output High Level	I_{SO} = − 3 mA	**V_{DD_IO} − 0.5**	V_{DD_IO} − 0.3		V
I_L	Output Leakage Current	V_{SO} = 2.8V			**1.0**	µA

SPI Interface

LP3933 is compatible with the SPI serial bus specification and it operates as a slave. The transmission consists of 16-bit Write and Read Cycles. One cycle consists of 7 Address bits, 1 Read/Write (R/W) bit and 8 Data bits. R/W bit high state defines a Write Cycle and low defines a Read Cycle. SO output is normally in high-impedance state and it is active only when Data is sent out during a Read Cycle. A pull-up or pull-down resistor may be needed in SO line, if a floating logic signal can cause unintended current consumption in the input where SO is connected. The Address and Data are transmitted MSB first. The Slave Select signal SS must be low during the Cycle transmission. SS resets the interface when high and it has to be taken high between successive Cycles. Data is clocked in on the rising edge of the SCK clock signal, while data is clocked out on the falling edge of SCK.

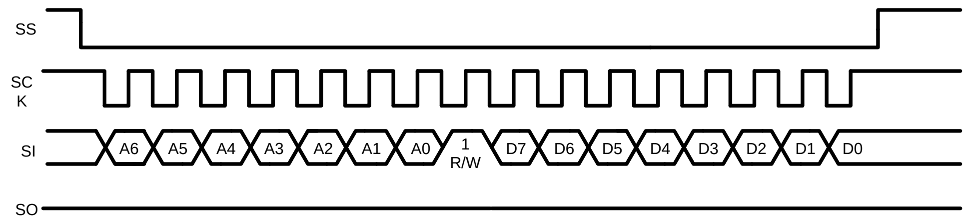


Figure 2. SPI Write Cycle

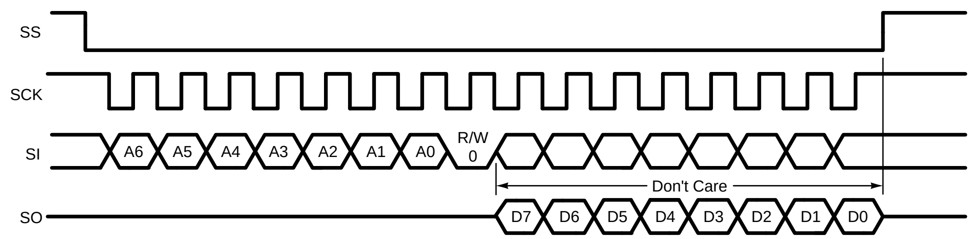


Figure 3. SPI Read Cycle

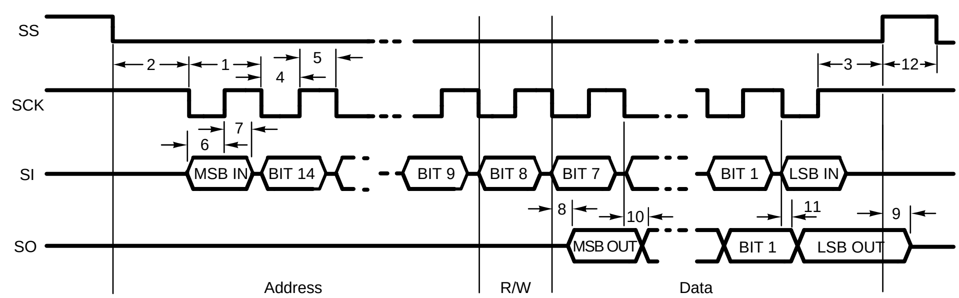


Figure 4. SPI Timing Diagram

SPI Timing Parameters

$V_{DD1,2} = V_{DD\_IO} = 2.775V$

Symbol	Parameter	Limit		Units
		Min	Max	
1	Cycle Time	70		ns
2	Enable Lead Time	35		ns
3	Enable Lag Time	35		ns
4	Clock Low Time	35		ns
5	Clock High Time	35		ns
6	Data Setup Time	0		ns

Symbol	Parameter	Limit		Units
		Min	Max	
7	Data Hold Time	20		ns
8	Data Access Time		20	ns
9	Output Disable Time		10	ns
10	Output Data Valid		20	ns
11	Output Data Hold Time	0		ns
12	SS Inactive Time	10		ns

Magnetic Boost DC/DC Converter

The LP3933 boost DC/DC Converter generates 4.1V–5.3V supply voltage for the LEDs from single Li-Ion battery (3V…4.5V). The output voltage is controlled with 8-bit register in 9 steps. The converter is a magnetic switching PWM mode DC/DC converter with a current limit. The converter has 1 MHz switching frequency when timing resistor RT is 82 KΩ.

The topology of the magnetic boost converter is called CPM control, current programmed mode, where the inductor current is measured and controlled with the feedback. The user can program the output voltage of the boost converter. The control changes the resistor divider in the feedback loop.

The following figure shows the boost topology with the protection circuitry. Three different protection schemes are implemented:

1. Over voltage protection, limits the maximum output voltage
   - Keeps the output below breakdown voltage.
   - Prevents boost operation if battery voltage is much higher than desired output.
2. Over current protection, limits the maximum inductor current
   - Voltage over switching NMOS is monitored, too high voltages turn the switch off.
3. Duty cycle limiting, done with digital control.

Figure 5. Boost Converter Topology

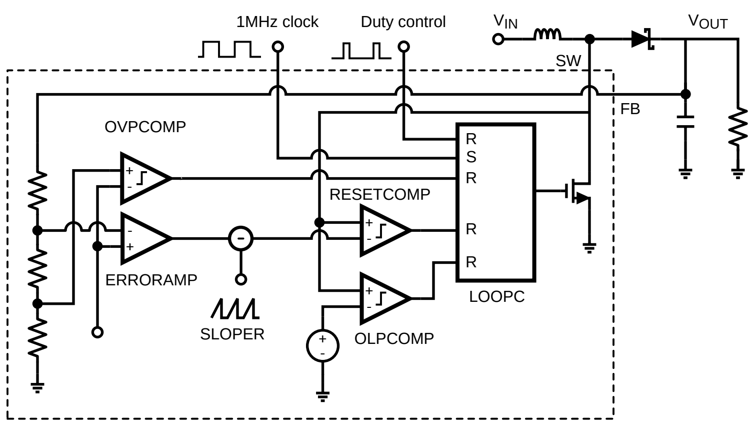


Table 5. Magnetic Boost DC/DC Converter Electrical Characteristics (R1, G1, B1, R2, G2, B2 outputs)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LOAD}	Load Current	$3.0V \leq V_{IN} \leq 4.5V$ $V_{OUT} = 5V$	0		300	mA

Table 5. Magnetic Boost DC/DC Converter Electrical Characteristics (R1, G1, B1, R2, G2, B2 outputs) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{FB}	Output Voltage Accuracy (FB Pin)	1 mA ≤ I_{LOAD} ≤ 300 mA 3.0V ≤ V_{IN} ≤ V_{OUT} − 0.5V V_{OUT} = 5V	**−5**		**+5**	%
	Voltage at FB Pin (Boost Converter Output Voltage)	1 mA ≤ I_{LOAD} ≤ 300 mA 3.0V < V_{IN} < 5V + $V_{(SCHOTTKY)}$		5		V
		1 mA ≤ I_{LOAD} ≤ 300 mA V_{IN} > 5V + $V_{(SCHOTTKY)}$		V_{IN}–$V_{(SCHOTTKY)}$		V
RDS_{ON}	Switch ON Resistance	$V_{DD1,\ 2}$ = 2.775V, I_{SW} = 0.5A		0.4	**0.7**	Ω
f_{PWF}	PWM Mode Switching Frequency	RT = 82 kΩ		1		MHz
	Frequency Accuracy	2.65 ≤ $V_{DD1,\ 2}$ ≤ 2.9	−6	±3	+6	%
		RT = 82 kΩ	**−9**		**+9**	%
$t_{STARTUP}$	Startup Time			25		ms
I_{CL_OUT}	SW Pin Current Limit		670	800	915	mA
			530		**995**	mA

Boost Standby Mode (R1, G1, B1, R2, G2, B2 outputs)

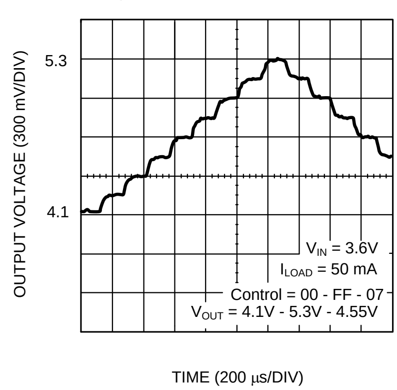
User can set the Boost Converter to STANDBY mode by writing the register bit EN_BOOST low. When EN_BOOST is written high, the converter starts for 10 ms in PFM mode and then goes to PWM mode.

Boost Output Voltage Control (R1, G1, B1, R2, G2, B2 outputs)

User can control the boost output voltage by boost output 8-bit register.

Boost [7:0] Register 0Dh		BOOST Output Voltage (typical)
Bin	Hex	
0000 0000	00	4.10
0000 0001	01	4.25
0000 0011	03	4.40
0000 0111	07	4.55
0000 1111	0F	4.70
0001 1111	1F	4.85
0011 1111	**3F**	**5.00 Default**
0111 1111	7F	5.15
1111 1111	FF	5.30

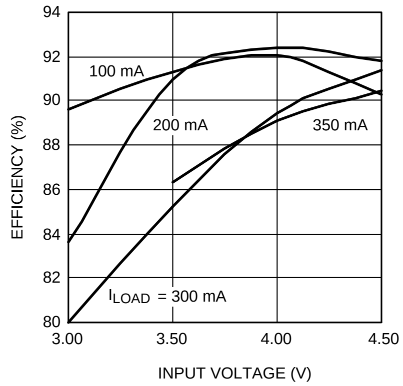
Figure 6. Boost Output Voltage Control (R1, G1, B1, R2, G2, B2 outputs)



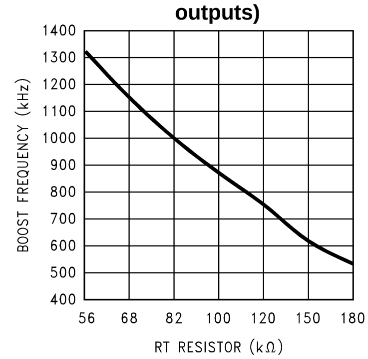
Boost Converter Typical Performance Characteristics (R1, G1, B1, R2, G2, B2 outputs)

V_{IN} = 3.6V, V_{OUT} = 5.0V if not otherwise stated.

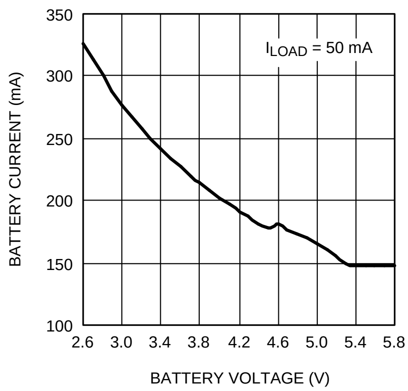
Boost Converter Efficiency (R1, G1, B1, R2, G2, B2 outputs)



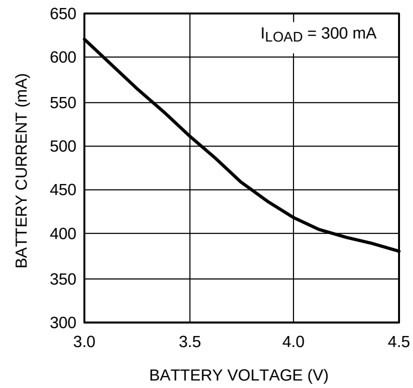
Boost Frequency vs RT Resistor (R1, G1, B1, R2, G2, B2 outputs)



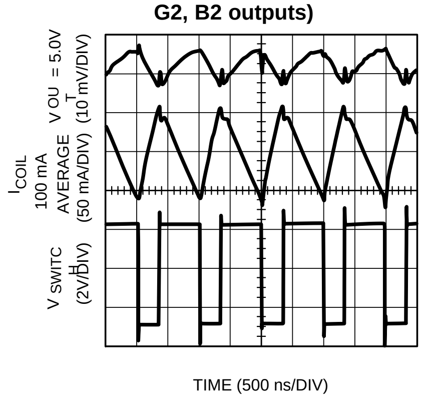
Battery Current vs Voltage (R1, G1, B1, R2, G2, B2 outputs)



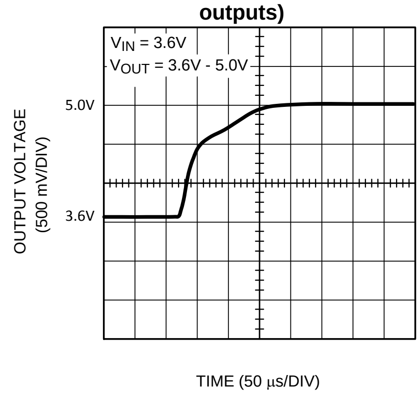
Battery Current vs Voltage (R1, G1, B1, R2, G2, B2 outputs)



Boost Typical Waveforms at 100 mA Load (R1, G1, B1, R2, G2, B2 outputs)



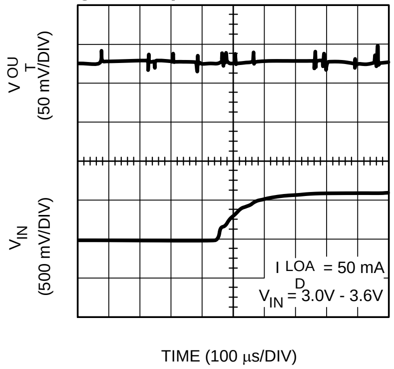
Boost Startup with No Load (R1, G1, B1, R2, G2, B2 outputs)



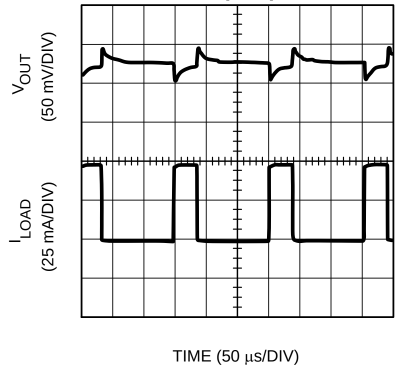
Boost Converter Typical Performance Characteristics (R1, G1, B1, R2, G2, B2 outputs) (continued)

V_{IN} = 3.6V, V_{OUT} = 5.0V if not otherwise stated.

Boost Line Regulation (R1, G1, B1, R2, G2, B2 outputs)



Boost Load Regulation, 50 mA–100 mA (R1, G1, B1, R2, G2, B2 outputs)



Dual RGB LED Driver (R1, G1, B1, R2, G2, B2 outputs)

The RGB driver has six outputs that can independently drive 2 separate RGB LEDs or six LEDs of any kind. User has control over the following parameters separately for each LED:

- **ON and OFF** (start and stop time in blinking cycle)
- **DUTY** (PWM brightness control)
- **SLOPE** (turn-on and turn-off slope)
- **ENABLE** (output enable control)

The main blinking cycle is controlled with 2-bit CYCLE control (0.25 / 0.5 / 1.0 / 2.0s).

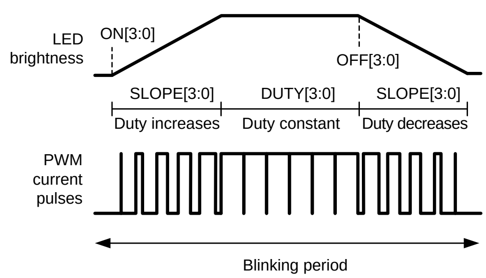


Figure 7. RGB PWM Operating Principle

RGB_START is the master enable control for the whole RGB function. The internal PWM and blinking control can be disabled by setting the RGB_PWM control LOW. In this case the individual enable controls can be used to switch outputs on and off. PWM_LED input can be used for external hardware PWM control.

In the normal PWM mode the R, G and B switches are controlled in 3 phases (one phase per driver). During each phase the peak current set by external resistor is driven through the LED for the time defined by DUTY setting (0 µs–50 µs). As a time averaged current this means 0%–33% of the peak current. The PWM period is 150 µs and the pulse frequency is 6.7 kHz in normal mode.

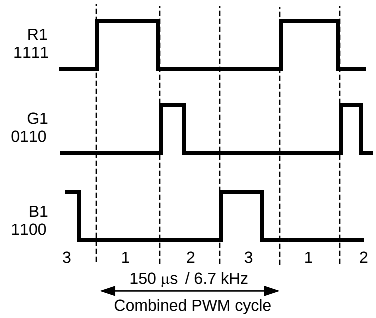


Figure 8. Normal Mode PWM Waveforms at Different Duty Settings

In the FLASH mode all the outputs are controlled in one phase and the PWM period is 50 µs. The time averaged FLASH mode current is three times the normal mode current at the same DUTY value.

Blinking can be controlled separately for each output. On and OFF times determine, when a LED turns on and off within the blinking cycle. When both ON and OFF are 0, the LED is on and doesn't blink. If ON equals OFF but is not 0, the LED is permanently off.

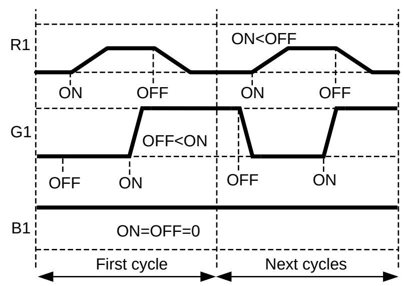


Figure 9. Example Blinking Waveforms

Table 6. RGB Driver Electrical Characteristics (R1, G1, B1, R2, G2, B2 outputs)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{DS-ON}	ON Resistance	I = 75 mA		3.5	**6**	Ω
$I_{LEAKAGE}$	Off State Leakage Current	V_{FB} = 5V, LED driver off		0.03	**1**	µA
I_{MAX}	Maximum Sink Current	(1)			**120**	mA
T_{SMAX}	Maximum Slope Period	At Maximum Duty Setting		0.93		s
T_{SMIN}	Minimum Slope Period	At Maximum Duty Setting		31		ms
T_{SRES}	Slope Resolution	At Maximum Duty Setting		62		ms
$T_{START/STOP}$	Start/Stop Resolution	Cycle 1s		1/16		s
Duty	Duty Step Size			6.25		%
T_{BLINK}	Blinking Cycle Accuracy		−6	±3	+6	%
D_{CYCF}	Duty Cycle Range	FLASH_MODE = 1	0		99.6	%
D_{CYC}	Duty Cycle Range	FLASH_MODE = 0	0		33.2	%
D_{RESF}	Duty Resolution	FLASH_MODE = 1 (4 bit)		6.64		%
D_{RES}	Duty Resolution	FLASH_MODE = 0 (4 bit)		2.21		%
F_{PWMF}	PWM Frequency	FLASH_MODE = 1		20		kHz
F_{PWM}	PWM Frequency	FLASH_MODE = 0		6.67		kHz

(1) The total load current of the boost converter should be limited to 300 mA.

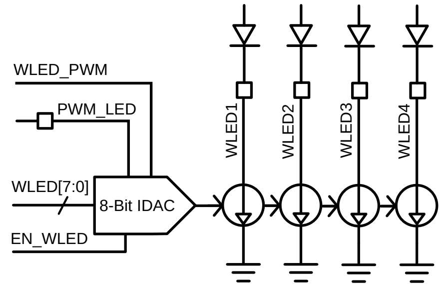
Table 7. RGB LED PWM Control (1)

R1DUTY[3:0] G1DUTY[3:0] B1DUTY[3:0] R2DUTY[3:0] G2DUTY[3:0] B2DUTY[3:0]	DUTY sets the brightness of the LED by adjusting the duty cycle of the PWM driver. The minimum duty cycle is 0% [0000] and the maximum in the FLASH mode is 100% [1111] of the peak pulse current. The peak pulse current is determined by the external resistor, LED voltage drop and the boost voltage. In normal mode the maximum duty cycle is 33%.
R1SLOPE[3:0] G1SLOPE[3:0] B1SLOPE[3:0] R2SLOPE[3:0] G2SLOPE[3:0] B2SLOPE[3:0]	SLOPE sets the turn-on and turn-off slopes. Fastest slope is set by [0000] and slowest by [1111]. SLOPE changes the duty cycle at constant, programmable rate. For each slope setting the maximum slope time appears at maximum DUTY setting. When DUTY is reduced, the slope time decreases proportionally. For example, in case of maximum DUTY, the sloping time can be adjusted from 31 ms [0000] to 930 ms [1111]. For 50% DUTY [0111] the sloping time is 14 ms [0000] to 434 ms [1111]. The blinking cycle has **no** effect on SLOPE.
R1ON[3:0] G1ON[3:0] B1ON[3:0] R2ON[3:0] G2ON[3:0] B2ON[3:0]	ON sets the beginning time of the turn-on slope. The on-time is relative to the selected blinking cycle length. On-setting N (N = 0–15) sets the on-time to N/16 * cycle length.
R1OFF[3:0] G1OFF[3:0] B1OFF[3:0] R2OFF[3:0] G2OFF[3:0] B2OFF[3:0]	OFF sets the beginning time of the turn-off slope. Off-time is relative to the blinking cycle length in the same way as the on-time.
	If **ON = 0, OFF = 0** and **RGB_PWM = 1**, then RGB outputs are continuously on (no blinking), the DUTY setting controls the brightness and the SLOPE setting is ignored. **If ON and OFF are the same, but not 0, the RGB outputs are turned off.**
CYCLE[1:0]	CYCLE sets the blinking cycle: [00] for 0.25s, [01] for 0.5s, [10] for 1s and [11] for 2s. CYCLE effects to all RGB LEDs.
RSW1 GSW1 BSW1 RSW2 GSW2 BSW2	Enable for R1 switch Enable for G1 switch Enable for B1 switch Enable for R2 switch Enable for G2 switch Enable for B2 switch
RGB_START	Master Switch for both RGB Drivers: RGB_START = 0 → RGB OFF RGB_START = 1 → RGB ON, starts the new cycle from t = 0
RGB_PWM	RGB_PWM = 0 → RSW, GWS and BSW control directly the RGB outputs (on/off control only) RGB_PWM = 1 → Normal PWM RGB functionality (duty, slope, on/off times, cycle)
EN_FLASH1 EN_FLASH2	Flash Mode enable controls for RGB1 and RGB2. In Flash mode (EN_FLASH = 1) RGB outputs are PWM controlled simultaneously, not in 3-phase system as in the Normal Mode.
R1_PWM G1_PWM B1_PWM R2_PWM G2_PWM B2_PWM	XX_PWM = 0 → External PWM control from PWM_LED pin is disabled XX_PWM = 1 → External PWM control from PWM_LED pin is enabled Internal PWM control (DUTY) can be used independently of external PWM control. External PWM has the same effect on all enabled outputs.

(1) Application Note 1291, “Driving RGB LEDs Using LP3933 Lighting Management System” contains a thorough description of the RGB driver functionality including programming examples.

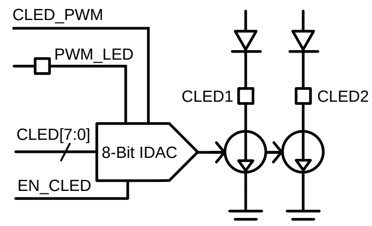
WLED Driver (WLED1...4)

White LED (WLED) driver drives each white LED with a regulated constant current. The amount of the current is controlled by the 8-bit current mode DAC from 0 to 25.5mA in 0.1mA steps.



CLED Driver (CLED1…2)

The current of CLEDs (Caller ID display backlight LEDs) can be adjusted by 8-bit current mode DAC. WLED and CLED can be used to drive any kind of LED.



Enables

WLED and CLED enable is controlled from user register.

PWM control of WLED and CLED (for dimming etc.) is possible using PWM_LED pin together with WLED_PWM and CLED_PWM enable control from user register.

Table 8. WLED and CLED Driver Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{RANGE}	Sink Current Range	V_{FB} = 5V, Control 00h–FFh		0–25.5		mA
I_{MAX}	Maximum Sink Current	(1)		25.5	**30**	mA
$I_{LEAKAGE}$	Leakage Current	V_{FB} = 5V		0.03	**1**	µA
I_{MATCH} 1–4	Sink Current Matching (2)	I_{SINK} = 13 mA, between WLED1...4 or CLED1...2		0.5	**2.7**	%

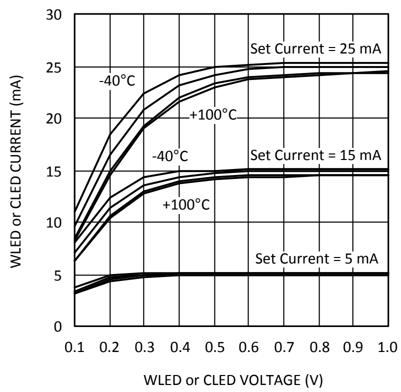
(1) A minimum voltage, Dropout Voltage, is required on the WLED and CLED outputs for maintaining the LED current. The current reduction at lower voltages is shown in the graph *WLED Output Current vs Voltage*
(2) Match % = 100% * (Max − Min)/Min

Adjustment

WLED[7:0] or CLED[7:0]	WLED or CLED Current (Typical)	Units
0000 0000	0	mA
0000 0001	0.1	mA
0000 0010	0.2	mA
0000 0011	0.3	mA
•	•	•
•	•	•

WLED[7:0] or CLED[7:0]	WLED or CLED Current (Typical)	Units
1111 1101	25.3	mA
1111 1110	25.4	mA
1111 1111	25.5	mA

Figure 10. WLED or CLED Output Current vs Voltage Temperatures −40°C, 25°C, 85°C, 100°C



Recommended External Components

OUTPUT CAPACITOR, C_{OUT}

The output capacitor C_{OUT} directly affects the magnitude of the output ripple voltage. In general, the higher the value of C_{OUT}, the lower the output ripple magnitude. Multilayer ceramic capacitors with low ESR are the best choice. At the lighter loads, the low ESR ceramics offer a much lower V_{OUT} ripple than the higher ESR tantalums of the same value. At the higher loads, the ceramics offer a slightly lower V_{OUT} ripple magnitude than the tantalums of the same value. However, the dv/dt of the V_{OUT} ripple with the ceramics is much lower than the tantalums under all load conditions. Capacitor voltage rating must be sufficient, 10V is recommended.

INPUT CAPACITOR, C_{IN}

The input capacitor C_{IN} directly affects the magnitude of the input ripple voltage and to a lesser degree the V_{OUT} ripple. A higher value C_{IN} will give a lower V_{IN} ripple. Capacitor voltage rating must be sufficient, 10V is recommended.

OUTPUT DIODE, D_{OUT}

A Schottky diode should be used for the output diode. To maintain high efficiency the average current rating of the schottky diode should be larger than the peak inductor current (1A). Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown of the schottky diode larger than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

INDUCTOR, L

The LP3933's high switching frequency enables the use of the small surface mount inductor. A 10 µH shielded inductor is suggested. Values below 4.7 µH should not be used. The inductor should have a saturation current rating higher than the peak current it will experience during circuit operation (1A). Less than 300 mΩ ESR is suggested for high efficiency. Open core inductors cause flux linkage with circuit components and interfere with the normal operation of the circuit. This should be avoided. For high efficiency, choose an inductor with a high frequency core material such as ferrite to reduce the core losses. To minimize radiated noise, use a toroid, pot core or shielded core inductor. The inductor should be connected to the SW pin as close to the IC as possible. Examples of suitable inductors are TDK types LLF4017T-100MR90C and VLF4012AT-100MR79 and Coilcraft type DO3314T-103.

Table 9. List of Recommended External Components

Symbol	Symbol Explanation	Value	Unit	Type
C_{VDD1}	V_{DD1} Bypass Capacitor	100	nF	Ceramic, X7R
C_{VDD2}	V_{DD2} Bypass Capacitor	100	nF	Ceramic, X7R
C_{OUT}	Output Capacitor from FB to GND	10	µF	Ceramic, X7R/Y5V
C_{IN}	Input Capacitor from Battery Voltage to GND	10	µF	Ceramic, X7R/Y5V
C_{VDDIO}	V_{DD_IO} Bypass Capacitor	100	nF	Ceramic, X7R
RT	Oscillator Frequency Bias Resistor	82	kΩ	1% (1)
RSO	SO Output Pull-up Resistor	100	kΩ	
C_{VREF}	Reference Voltage Capacitor, between V_{REF} and GND	100	nF	Ceramic, X7R
L_{BOOST}	Boost Converter Inductor	10	µH	Shielded, Low ESR, I_{SAT}1A
D_{OUT}	Rectifying Diode, V_F @ Maxload	0.3	V	Schottky Diode
RGB1	RGB LED1	User Defined (See Application Note 1291 for resistor size calculation)		
RGB2	RGB LED2			
R_{R1}, R_{G1}, R_{B1}	Current Limit Resistor			
R_{R2}, R_{G2}, R_{B2}	Current Limit Resistor			
LEDs	White LEDs			

(1) Resistor RT tolerance change will change the timing accuracy of RGB block. Also the boost converter switching frequency will be affected.

Control Registers

Control registers and register bits are shown in the following table.

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
00H	**RGB Control register1**	rgb pwm	rgb start	rsw1	gsw1	bsw1	rsw2	gsw2	bsw2
01H	**red1_on_off**	r1_on[3]	r1_on[2]	r1_on[1]	r1_on[0]	r1_off[3]	r1_off[2]	r1_off[1]	r1_off[0]
02H	**green1_on_off**	g1_on[3]	g1_on[2]	g1_on[1]	g1_on[0]	g1_off[3]	g1_off[2]	g1_off[1]	g1_off[0]
03H	**blue1_on_off**	b1_on[3]	b1_on[2]	b1_on[1]	b1_on[0]	b1_off[3]	b1_off[2]	b1_off[1]	b1_off[0]
04H	**r1slope, r1duty**	r1slope[3]	r1slope[2]	r1slope[1]	r1slope[0]	r1duty[3]	r1duty[2]	r1duty[1]	r1duty[0]
05H	**g1slope, g1duty**	g1slope[3]	g1slope[2]	g1slope[1]	g1slope[0]	g1duty[3]	g1duty[2]	g1duty[1]	g1duty[0]
06H	**b1slope, b1duty**	b1slope[3]	b1slope[2]	b1slope[1]	b1slope[0]	b1duty[3]	b1duty[2]	b1duty[1]	b1duty[0]
07H	**RGB Control register2**	cycle[1]	cycle[0]	r1_pwm	g1_pwm	b1_pwm	r2_pwm	g2_pwm	b2_pwm
08H	**wled control reg**					wled_pwm	cled_pwm	en_wled	en_cled
09H	**WLED1–4**	wled[7]	wled[6]	wled[5]	wled[4]	wled[3]	wled[2]	wled[1]	wled[0]
0AH	**CLED1–2**	cled[7]	cled[6]	cled[5]	cled[4]	cled[3]	cled[2]	cled[1]	cled[0]
0BH	**enables**		nstby	en_boost	en_flash1	en_flash2			

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
0DH	**boost output**	boost[7]	boost[6]	boost[5]	boost[4]	boost[3]	boost[2]	boost[1]	boost[0]
2AH	**red2_on_off**	r2_on[3]	r2_on[2]	r2_on[1]	r2_on[0]	r2_off[3]	r2_off[2]	r2_off[1]	r2_off[0]
2BH	**green2_on_off**	g2_on[3]	g2_on[2]	g2_on[1]	g2_on[0]	g2_off[3]	g2_off[2]	g2_off[1]	g2_off[0]
2CH	**blue2_on_off**	b2_on[3]	b2_on[2]	b2_on[1]	b2_on[0]	b2_off[3]	b2_off[2]	b2_off[1]	b2_off[0]
2DH	**r2slope, r2duty**	r2slope[3]	r2slope[2]	r2slope[1]	r2slope[0]	r2duty[3]	r2duty[2]	r2duty[1]	r2duty[0]
2EH	**g2slope, g2duty**	g2slope[3]	g2slope[2]	g2slope[1]	g2slope[0]	g2duty[3]	g2duty[2]	g2duty[1]	g2duty[0]
2FH	**b2slope, b2duty**	b2slope[3]	b2slope[2]	b2slope[1]	b2slope[0]	b2duty[3]	b2duty[2]	b2duty[1]	b2duty[0]