National Semiconductor

October 2005

LP5550
PowerWise™ Technology Compliant Energy Management Unit

General Description

The LP5550 is a PWI 1.0 compliant Energy Management System for reducing power consumption of stand-alone mobile phone processors such as base-band or applications processors.

The LP5550 contains an advanced, digitally controlled switching regulator for supplying variable voltage to processor core and memory. The device also incorporates 3 programmable LDO-regulators for powering I/O, PLLs and maintaining memory retention in shutdown-mode.

The device is controlled via the PWI open-standard interface. The LP5550 operates cooperatively with PowerWise technology compatible processors to optimize supply voltages adaptively over process and temperature variations or dynamically using frequency/voltage pre-characterized look-up tables.

Features

- Supports high-efficiency PowerWise Technology Adaptive Voltage Scaling
- PWI open standard interface for system power management
- Digitally controlled intelligent voltage scaling
- 1 MHz PWM switching frequency
- Auto or PWI controlled PFM mode transition
- Internal soft start/startup sequencing.
- 3 programmable LDOs for I/O, PLL, and memory retention supply generation.
- Power OK output.

Applications

- GSM/GPRS/EDGE & UMTS cellular handsets
- Hand-held radios
- PDAs
- Battery powered devices
- Portable instruments

System Diagram

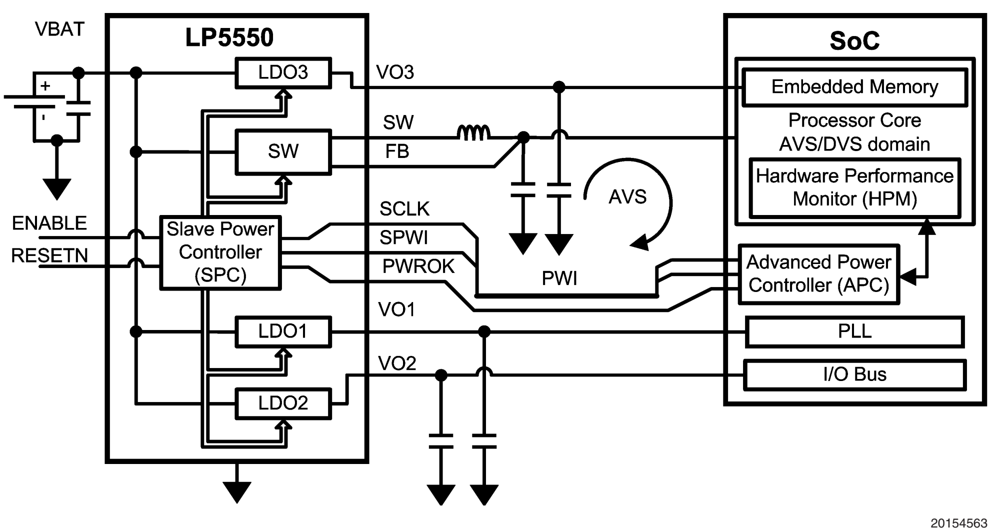


FIGURE 1. System Diagram

Connection Diagrams and Package Mark Information

16 - Pin LLP
NS Package Number SQA16A

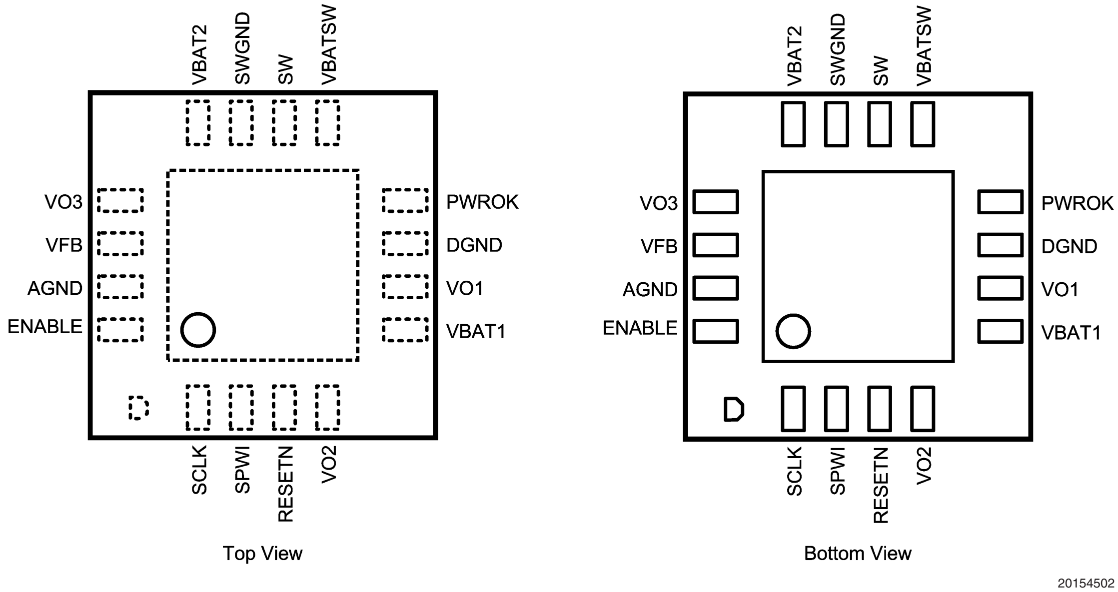
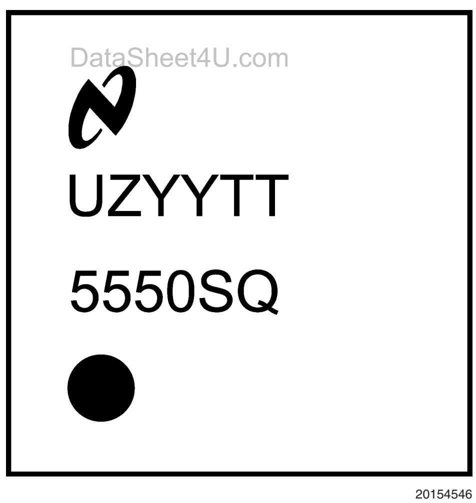


FIGURE 2. LP5550 Pinout

Package Mark



Note: The actual physical placement of the package marking will vary from part to part.

FIGURE 3. Top View

Typical Application

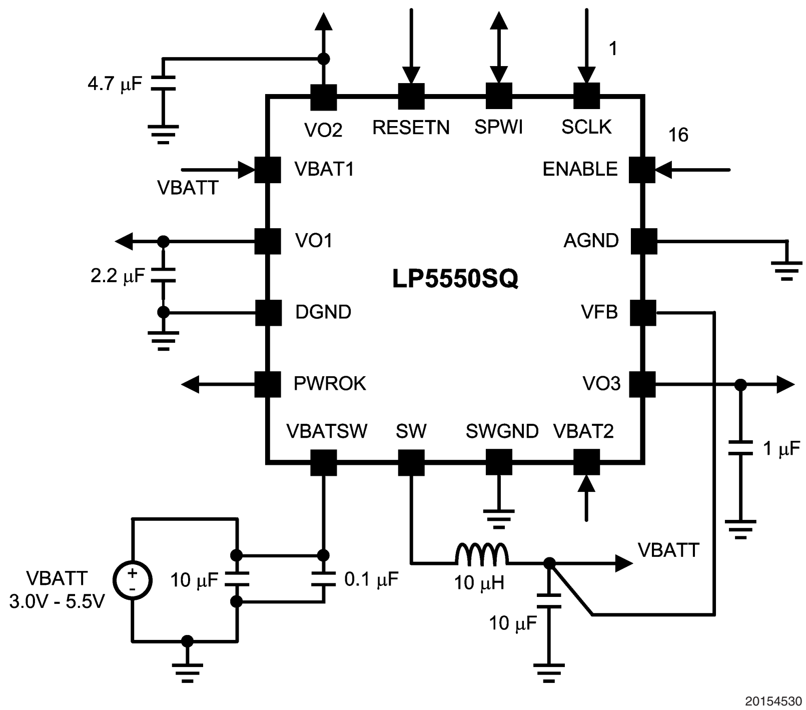


FIGURE 4. Typical Application Circuit

Pin Descriptions

Pin #	Name	I/O	Type	Description
1	SCLK	I	D	PowerWise Interface (PWI) clock input
2	SPWI	I/O	D	PowerWise Interface (PWI) bi-directional data
3	RESETN	I	D	Reset, active low
4	VO2	O	A	LDO2 output, for supplying the I/O voltage on the SoC
5	VBAT1	P	P	Battery supply voltage
6	VO1	O	A	LDO1 output, for supplying a fixed voltage to a PLL etc. on the SoC
7	DGND	G	G	Digital ground
8	PWROK	O	D	Power OK, active high output signal
9	VBATSW	P	P	Battery supply voltage for switching regulator
10	SW	O	A	Switcher pin connected to coil
11	SWGND	G	G	Switcher ground
12	VBAT2	P	P	Battery supply voltage
13	VO3	O	A	LDO3 output, on-chip memory supply voltage
14	VFB	I	A	Switcher output voltage for supplying SoC core logic
15	AGND	G	G	Analog Ground
16	ENABLE	I	D	Enable, active high

A: Analog Pin

D: Digital Pin

I: Input Pin

O: Output Pin

I/O: Input/Output Pin

P: Power Pin

G: Ground Pin

Ordering Information

Voltage Option	Order Number	Package Marking	Supplied As
	LP5550SQ	LP5550SQ	1000 units, Tape-and-Reel
	LP5550SQX	LP5550SQ	4500 units, Tape-and-Reel

*Released. Samples available.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VBAT1, VBAT2, VBATSW	-0.3 to +6.0V
VO1, VO2, VO3 to GND	-0.3 to +VBAT1+0.3V
ENABLE, RESETN, VFB, SW, SPWI, SCLK, PWROK	-0.3 to VBAT2+0.3V
DGND, AGND, SWGND to GND SLUG	±0.3V
Junction Temperature (TJ-MAX)	150˚C
Storage Temperature Range	-65˚C to 150˚C
Maximum Continuous Power Dissipation (PD-MAX) (Note 3)	1.0 W
Maximum Lead Temperature (Soldering)	Note 4
ESD Rating (Note 3)	
Human Body Model:	
SW pin	1.0kV
All other pins	2.0kV

Operating Ratings (Notes 1, 2)

VBAT1, VBAT2, VBATSW	3.0V to 5.5V
Junction Temperature (T_J) Range	–40˚C to +125˚C
Ambient Temperature (T_A) Range(Note 5)	–40˚C to +85˚C

Thermal Properties (Note 6)

Junction-to-Ambient Thermal Resistance (θ_{JA})	39.8˚C/W

General Electrical Characteristics

Unless otherwise noted, $V_{BAT1,2,SW}$, RESETN, ENABLE = 3.6V. Typical values and limits appearing in normal type apply for TJ = 25˚C. Limits appearing in boldface type apply over the entire junction temperature range for operation, -40 to +125˚C. (Notes 2, 7, 8, 9)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_Q	Shutdown Supply current	$V_{BAT1,2,SW}$ = 2.0V, all circuits off.		1	**6**	µA
	Sleep State Supply Current (V_{O3} load 1 mA)	$V_{BAT1,2,SW}$ = 3.6V, LDO3 (V_{O3}) on, PWI on. All other circuits off.		70	**85**	µA
	Acitve State Supply Current (No load, PFM mode)	$V_{BAT1,2,SW}$ = 3.6V, LDOs 1 and 2 on, Switcher on, PWI on.		140	**165**	µA
T_{SD}	Thermal Shutdown Threshold			160		˚C
	Thermal Shutdown Hysteresis			10		

LDO1 (PLL/Fixed Voltage) Characteristics

Unless otherwise noted, $V_{BAT1,2,SW}$, RESETN, ENABLE = 3.6V. Typical values and limits appearing in normal type apply for TJ = 25˚C. Limits appearing in boldface type apply over the entire junction temperature range for operation, -40 to +125˚C. (Notes 2, 7, 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage	1mA ≤ IOUT ≤ 100mA,V_{OUT} = 2V, 3.0V ≤ $V_{BAT1,2,SW}$ ≤ 5.5V	**-3%**	2	**3%**	V
V_{OUT} Range	Programmable Output Voltage Range	0µA ≤ I_{OUT} ≤ 100mA, Programming Resolution=100mV	0.7	1.2	2.2	V
I_{OUT}	Recommended Output Current	3.0V ≤ VBAT1,2,SW ≤ 5.5V		100		mA
	Short Circuit Current Limit	V_{OUT} = 0V			**350**	
I_Q	Quiescent Current	I_{OUT} = 0mA(Note 11)		35	**45**	µA
ΔV_{OUT}	Line Regulation	3.0V ≤ $V_{BAT1,2,SW}$ ≤ 5.5V, I_{OUT} = 50mA	**-0.0125**		**0.0125**	%/V
	Load Regulation	V_{IN} = 3.6V, 1mA ≤ I_{OUT} ≤ 100mA	**-0.0085**		**0.0085**	%/mA
	Line Transient Regulation	3.6V ≤ V_{IN} ≤ 3.9V, TRISE,FALL = 10 µs		27		mV
	Load Transient Regulation	V_{IN} = 3.6V, 10mA ≤ I_{OUT} ≤ 90 mA, TRISE,FALL = 100 ns		86		mV
eN	Output Noise Voltage	10Hz ≤ f ≤ 100kHz,C_{OUT} = 2.2µF		0.103		mVRMS

LDO1 (PLL/Fixed Voltage) Characteristics

Unless otherwise noted, $V_{BAT1,2,SW}$, RESETN, ENABLE = 3.6V. Typical values and limits appearing in normal type apply for TJ = 25˚C. Limits appearing in boldface type apply over the entire junction temperature range for operation, -40 to +125˚C. (Notes 2, 7, 8) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PSRR	Power Supply Ripple Rejection Ratio	f = 1kHz, C_{OUT} = 2.2µF		56		dB
		f = 10kHz, C_{OUT} = 2.2µF		36		dB
C_{OUT}	Output CapacitanceOutput Capacitor ESR	0µA ≤ I_{OUT} ≤ 100mA	1	2.2	20	µF
			5		500	mΩ
$t_{START-UP}$	Start-Up Time from Shut-down	C_{OUT} = 1µF, I_{OUT} = 100mA		54		µs

LDO2 (I/O Voltage) Characteristics

Unless otherwise noted, $V_{BAT1,2,SW}$, RESETN, ENABLE = 3.6V. Typical values and limits appearing in normal type apply for TJ = 25˚C. Limits appearing in boldface type apply over the entire junction temperature range for operation, -40 to +125˚C. (Notes 2, 7, 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage	1mA ≤ I_{OUT} ≤ 250mA, V_{OUT} = 3.3V, V_{OUT} +0.4V ≤ $V_{BAT1,2,SW}$ ≤ 5.5V	**-3%**	3.3	**3%**	V
V_{OUT} Range	Programmable Output Voltage Range	0µA ≤ I_{OUT} ≤ 250mA, 1.5-2.3V =100mV step, 2.5V, 2.8V, 3.0V and 3.3V	1.5	3.3	3.3	V
I_{OUT}	Recommended Output Current	V_{OUT} +0.4V ≤ $V_{BAT1,2,SW}$ ≤ 5.5V		250		mA
	Output Current Limit	V_{OUT} = 0V			**740**	
	Dropout Voltage(Note 10)	I_{OUT} = 125mA		70	**260**	mV
I_Q	Quiescent Current	I_{OUT} = 0mA (Note 11)		55	**60**	µA
ΔV_{OUT}	Line Regulation	V_{OUT} +0.4V ≤ $V_{BAT1,2,SW}$ ≤ 5.5V, I_{OUT} = 125mA	**-0.0125**		**0.0125**	%/V
	Load Regulation	V_{IN} = 3.6V, 1mA ≤ I_{OUT} ≤ 250mA	**-0.011**		**0.011**	%/mA
	Line Transient Regulation	3.6V ≤ V_{IN} ≤ 3.9V, $T_{RISE,FALL}$ = 10 us		24		mV
	Load Transient Regulation	V_{IN} = 3.6V, 25mA ≤ I_{OUT} ≤ 225 mA, $T_{RISE,FALL}$ = 100 ns		246		mV
eN	Output Noise Voltage	10Hz ≤ f ≤ 100kHz, C_{OUT} = 4.7µF		0.120		mVRMS
PSRR	Power Supply Ripple Rejection Ratio	f = 1kHz, C_{OUT} = 4.7µF		46		dB
		f = 10kHz, C_{OUT} = 4.7µF		34		
C_{OUT}	Output Capacitance	0µA ≤ I_{OUT} ≤ 250mA	2	4.7	20	µF
	Output Capacitor ESR		5		500	mΩ
$t_{START-UP}$	Start-Up Time from Shut-down	C_{OUT} = 4.7µF, I_{OUT} = 250mA		144		µs

LDO3 (Memory Retention Voltage) Characteristics

Unless otherwise noted, $V_{BAT1,2,SW}$, RESETN, ENABLE = 3.6V. Typical values and limits appearing in normal type apply for TJ = 25˚C. Limits appearing in boldface type apply over the entire junction temperature range for operation, -40 to +125˚C. (Notes 2, 7, 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage Active state: Tracking V_{AVS}	I_{OUT} ≤ 50mA, VOUT = 1.2V, 3.0V ≤ $V_{BAT1,2,SW}$ ≤ 5.5V	**-3%**	1.2	**3%**	V
	Sleep state: Memory retention voltage regulation	I_{OUT} ≤ 5mA, V_{OUT} = 1.2V, 3.0V ≤ $V_{BAT1,2,SW}$ ≤ 5.5V	**-3%**	1.2	**3%**	V
V_{OFFSET}	Active State Buffer offset (= V_{O3}-V_{FB})	I_{OUT} = 50 mA, V_{OUT} = 0.6 V		13		mV
		I_{OUT} = 50 mA, V_{OUT} = 1.2V		28		mV
V_{OUT} Range	Programmable Output Voltage Range (Sleep state)	0µA ≤ I_{OUT} ≤ 5mA, Programming Resolution=50mV	0.6	1.2	1.35	V
I_Q	Quiescent Current	Active mode, I_{OUT} = 10µA (Note 11)		33	44	µA
		Sleep mode, I_{OUT} = 10µA (Note 11)		10	16	µA

LDO3 (Memory Retention Voltage) Characteristics

Unless otherwise noted, $V_{BAT1,2,SW}$, RESETN, ENABLE = 3.6V. Typical values and limits appearing in normal type apply for TJ = 25˚C. Limits appearing in boldface type apply over the entire junction temperature range for operation, -40 to +125˚C. (Notes 2, 7, 8) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OUT}	Recommended Output Current, Active state	3.0V ≤ $V_{BAT1,2,SW}$ ≤ 5.5V		50		mA
	Recommended Output Current, Sleep state	3.0V ≤ $V_{BAT1,2,SW}$ ≤ 5.5V		5		
	Short Circuit Current Limit, Active state	V_{OUT} = 0V			**230**	
eN	Output Voltage Noise	10Hz ≤ f ≤ 100kHz,C_{OUT} = 1µF		0.158		mVRMS
PSRR	Power Supply Ripple Rejection Ratio	f = 217Hz, C_{OUT} = 1.0µF		36		dB
COUT	Output Capacitance	0µA ≤ I_{OUT} ≤ 5mA	0.7	1	2.2	µF
	Output Capacitor ESR		5		500	mΩ

Switcher (Core Voltage) Characteristics

Unless otherwise noted, $V_{BAT1,2,SW}$, RESETN, ENABLE = 3.6V. Typical values and limits appearing in normal type apply for TJ = 25˚C. Limits appearing in boldface type apply over the entire junction temperature range for operation, -40 to +125˚C. (Notes 2, 7, 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage	I_{OUT} = 1 mA, V_{OUT} = 1.2V, 3.0V < $V_{BAT1,2,SW}$ <5.5V	1.53%		2.70%	V
		I_{OUT} = 1-300 mA, 3.0V < $V_{BAT1,2,SW}$ <5.5V	-0.44%		2.70%	
V_{OUT} Range	Programmable Output Voltage Range	0mA ≤ I_{OUT} ≤ 300mA, Programming Resolution = 4.7mV	0.6	1.2	1.2	V
ΔV_{OUT}	Line regulation	3.0V < $V_{BAT1,2,SW}$ <5.5V, I_{OUT} = 10 mA		0.18		%/V
	Load regulation	$V_{BAT1,2,SW}$ = 3.6V I_{OUT} = 100-300mA		0.0019		%/mA
I_Q	Quiescent current consumption	I_{OUT} = 0mA		15	**30**	µA
$R_{DSON(P)}$	P-FET resistance	$V_{BAT1,2,SW}$ = VGS = 3.6V		360	**690**	mΩ
$R_{DSON(N)}$	N-FET resistance	$V_{BAT1,2,SW}$ = VGS = 3.6V		250	**660**	mΩ
I_{LIM}	Switch peak current limit	3.0V < $V_{BAT1,2,SW}$ <5.5V	**400**	620	**750**	mA
f_{OSC}	Internal oscillator frequency	PWM-mode	800	1000	1360	kHz
C_{OUT}	Output Capacitance	0mA ≤ I_{OUT} ≤ 300mA	5	10	22	µF
	Output Capacitor ESR		5		500	mΩ
L	Inductor inductance	0uA ≤ I_{OUT} ≤ 300mA		4.7 / 10		µH
R_{VFB}	V_{FB} pin resistance to ground		150		650	kΩ

Logic and Control Inputs

Unless otherwise noted, $V_{BAT1,2,SW}$, RESETN, ENABLE = 3.6V. Typical values and limits appearing in normal type apply for TJ = 25˚C. Limits appearing in boldface type apply over the entire junction temperature range for operation, -40 to +125˚C. (Notes 2, 7, 8, 9)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Level	ENABLE, RESETN, SPWI, SCLK 3.0V ≤ V_{BAT1} ≤ 5.5V			**0.2**	V
V_{IH}	Input High Level	ENABLE, RESETN 3.0V ≤ V_{BAT1} ≤ 5.5V	**2**			V
V_{IH_PWI}	Input High Level, PWI	SPWI, SCLK, 1.5V ≤V_{O2} ≤ 3.3V	**V_{O2}-0.2V**			V
I_{IL}	Logic Input Current	ENABLE, RESETN, 0V ≤ V_{BAT1} ≤ 5.5V	**-5**		**5**	µA
I_{IL_PWI}	Logic Input Current, PWI	SPWI, SCLK, 1.5V ≤ V_{O2} ≤ 3.3V	**-5**		**15**	µA

Logic and Control Inputs

Unless otherwise noted, $V_{BAT1,2,SW}$, RESETN, ENABLE = 3.6V. Typical values and limits appearing in normal type apply for TJ = 25˚C. Limits appearing in boldface type apply over the entire junction temperature range for operation, -40 to +125˚C. (Notes 2, 7, 8, 9) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{PD_PWI}	Pull-down resistance for PWI signals		**0.5**	1	**2**	MΩ
T_{EN_LOW}	Minimum low pulse width to enter STARTUP state	ENABLE pulsed high - low - high from SHUTDOWN state		100		μsec
		ENABLE pulsed high - low - high from SLEEP or ACTIVE state		4		

Logic and Control Outputs

Unless otherwise noted, $V_{BAT1,2,SW}$, RESETN, ENABLE = 3.6V. Typical values and limits appearing in normal type apply for TJ = 25˚C. Limits appearing in boldface type apply over the entire junction temperature range for operation, -40 to +125˚C. (Notes 2, 7, 8, 9)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Output low level	PWROK, SPWI, $I_{SINK} \leq 1$ mA			**0.4**	V
V_{OH}	Output high level	PWROK, $I_{SOURCE} \leq 1$ mA	**V_{BAT1}-0.4V**			V
V_{OH_PWI}	Output high level, PWI	SPWI, $I_{SOURCE} \leq 1$ mA	**V_{O2}-0.4V**			V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

The amount of Absolute Maximum power dissipation allowed for the device depends on the ambient temperature and can be calculated using the formula P = (TJ – TA)/θ_{JA}, (1) where TJ is the junction temperature, TA is the ambient temperature, and JA is the junction-to-ambient thermal resistance.

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at TJ=150˚C (typ.) and disengages at TJ=140˚C (typ.).

Note 4: For detailed soldering specifications and information, please refer to National Semiconductor Application Note 1187: Leadless Leadframe Package (LLP) (AN-1187).

Note 5: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (TA-MAX) is dependent on the maximum operating junction temperature (TJ-MAX-OP = 125˚C), the maximum power dissipation of the device in the application (PD-MAX), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: TA-MAX = TJ-MAX-OP – (θJA x PD-MAX).

Note 6: Junction-to-ambient thermal resistance (θJA) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 102mm x 76mm x 1.6mm with a 2x1 array of thermal vias. The ground plane on the board is 50mm x 50mm. Thickness of copper layers are 36µm/18µm/18µm/36µm (1.5oz/1oz/1oz/1.5oz). Ambient temperature in simulation is 22˚C, still air. Power dissipation is 1W.

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

The value of θ_{JA} of this product can vary significantly, depending on PCB material, layout, and environmental conditions. In applications where high maximum power dissipation exists (high VIN, high IOUT), special care must be paid to thermal dissipation issues. For more information on these topics, please refer to Application Note 1187: Leadless Leadframe Package (LLP) and the Power Efficiency and Power Dissipation section of this datasheet.

Note 7: All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with TJ = 25C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 8: Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics

Note 9: Guaranteed by design.

Note 10: Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value. This specification does not apply in cases it implies operation with an input voltage below the 3.0V minimum appearing under Operating Ratings. For example, this specification does not apply for devices having 1.5V outputs because the specification would imply operation with an input voltage at or about 1.5V

Note 11: Quiescent current for LDO1, LDO2, and LDO3 do not include shared functional blocks such as the bandgap reference.

Simplified Functional Diagram

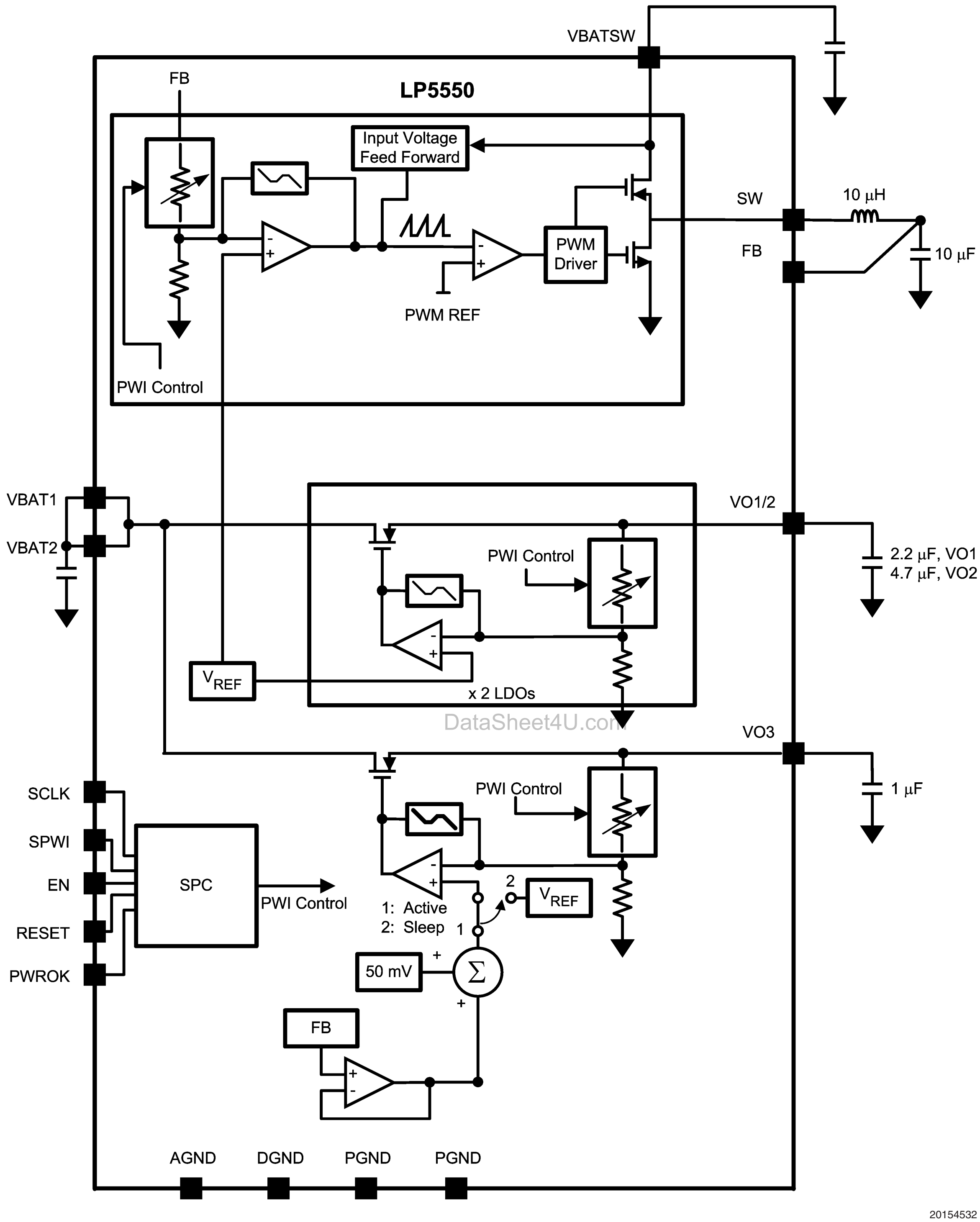
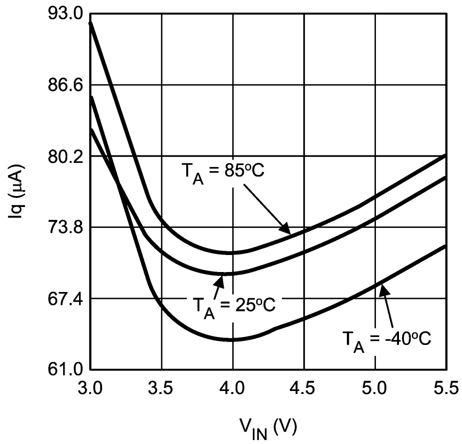


FIGURE 5. Simplified Functional Diagram

Typical Performance Characteristics Unless otherwise stated: V_{IN}=3.6V

I_Q vs. V_{IN}
Sleep, no load on LDO3



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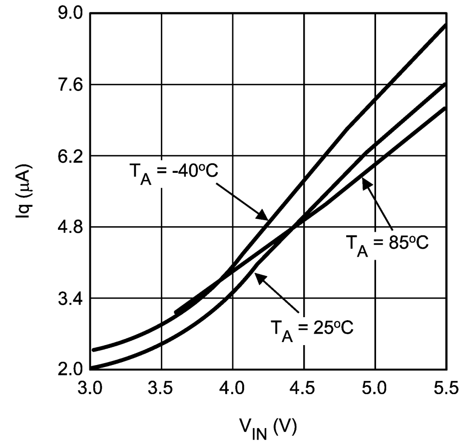
I_Q vs. V_{IN}
Shutdown



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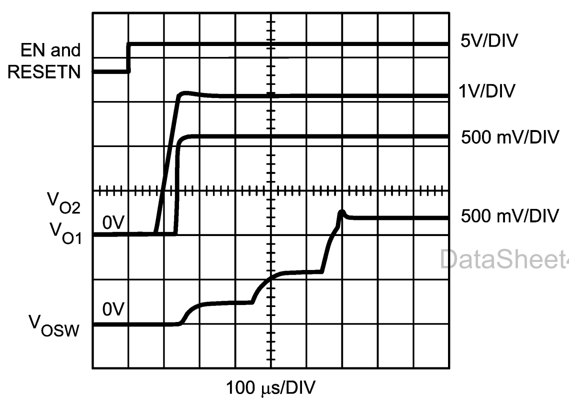
Start-up Sequence
V_{O1}, V_{O2}, V_{OSW}



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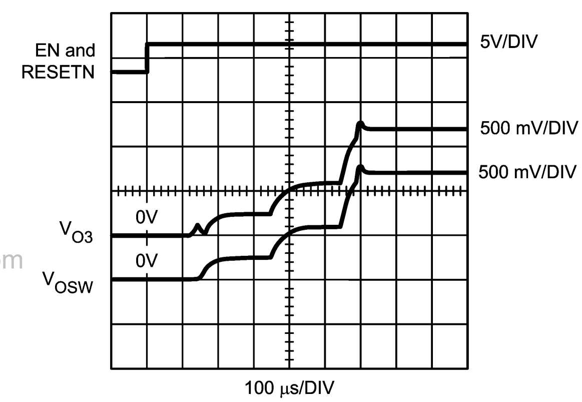
Start-up Sequence
V_{OSW}, V_{O3}



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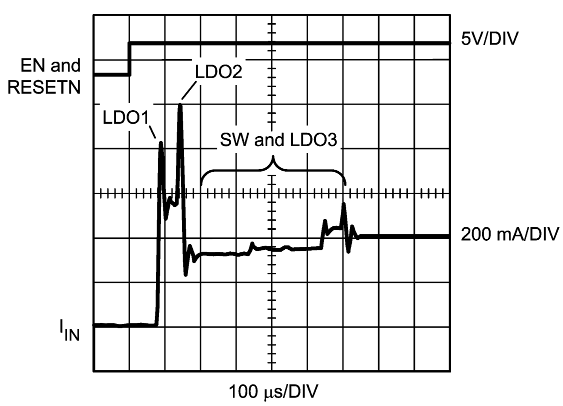
Start-up Sequence
Inrush Current



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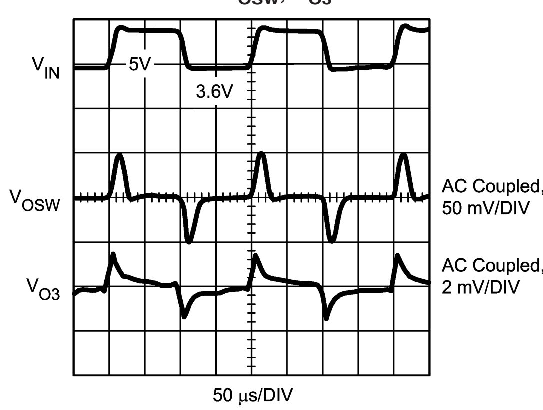
Line Transient Response
V_{OSW}, V_{O3}



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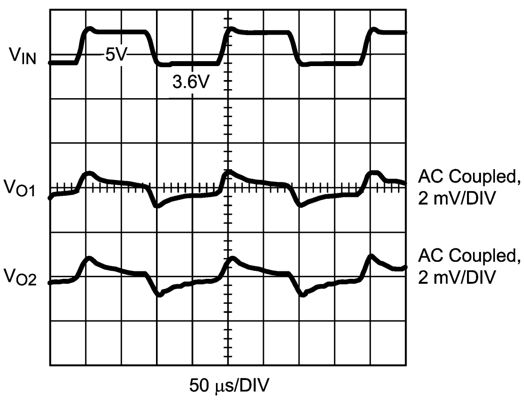
Typical Performance Characteristics Unless otherwise stated: V_{IN}=3.6V (Continued)

Line Transient Response
V_{O1}, V_{O2}



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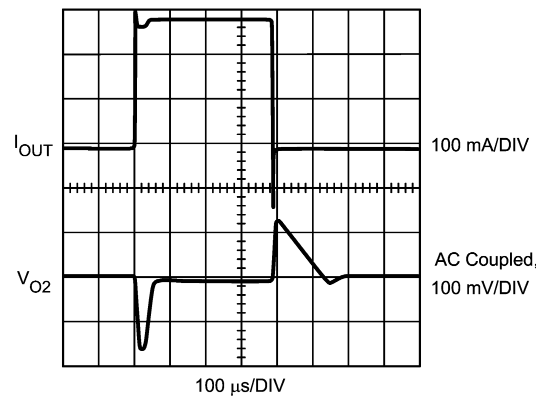
Load Transient Response
V_{O2}



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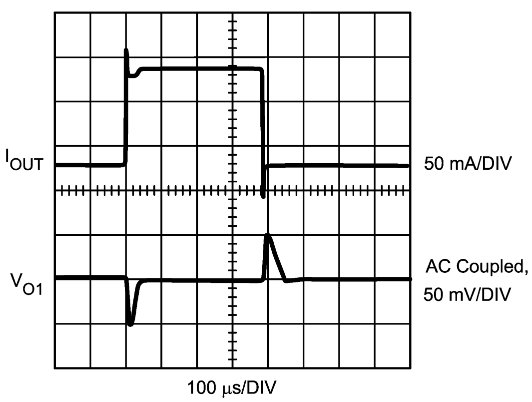
Load Transient Resoponse
V_{O1}



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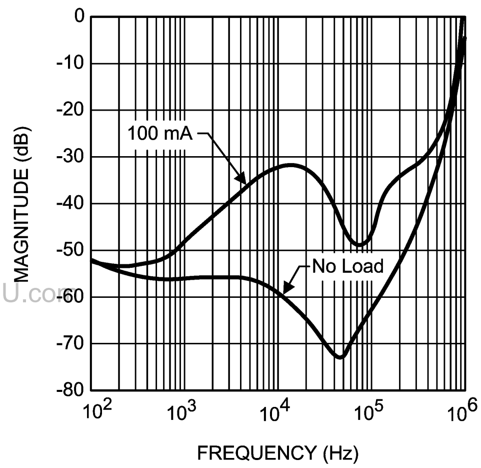
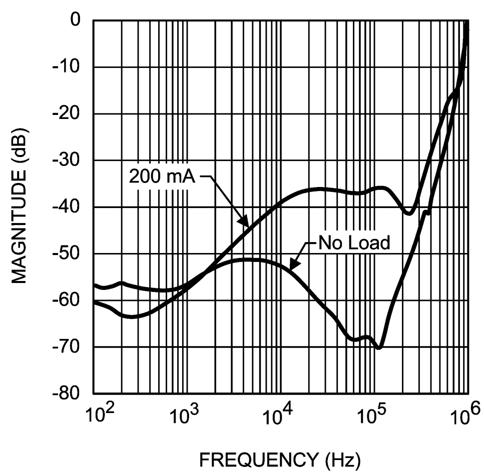
LDO1 PSRR



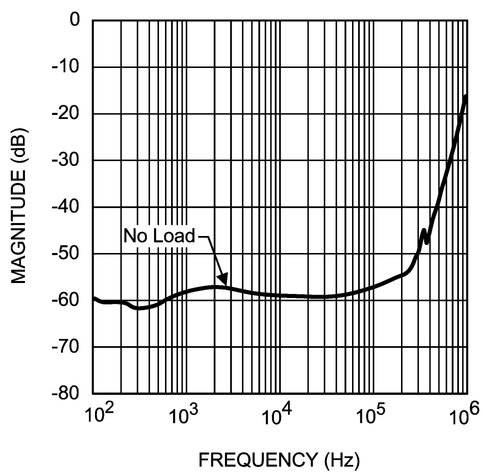
20154557

LDO2 PSRR



20154558

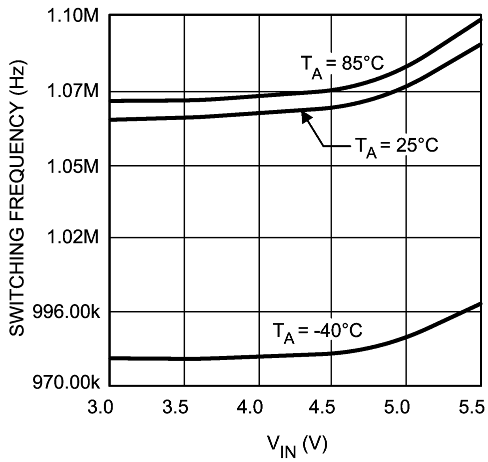
LDO3 PSRR



20154559

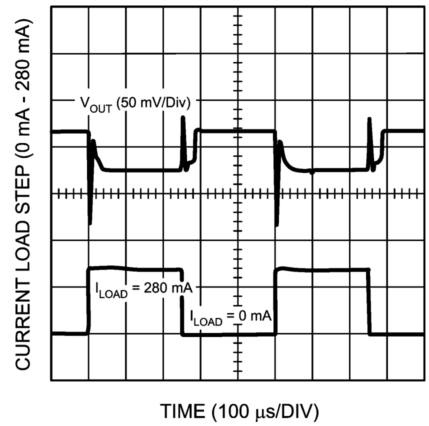
Typical Performance Characteristics Unless otherwise stated: V_{IN}=3.6V (Continued)

Switching Frequency vs. V_{IN}



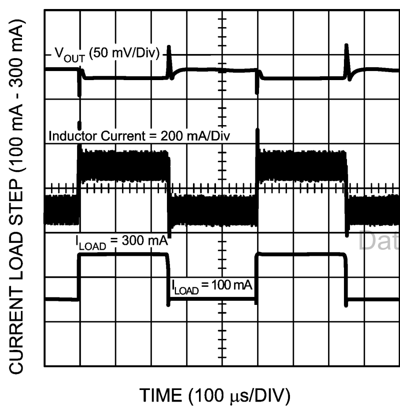
20154510

Load Transient Response
Switcher, Automatic PWM/PFM Transition



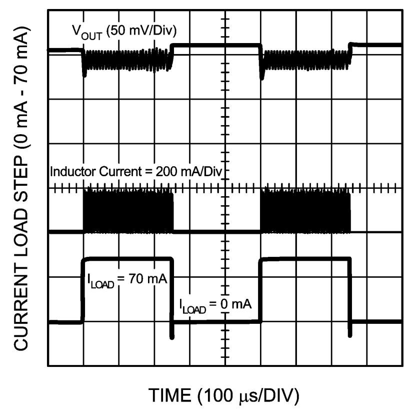
20154513

Load Trainsiet Response
Switcher, PWM only



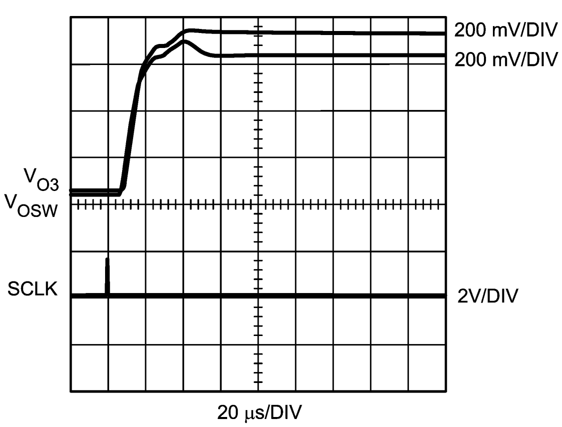
20154514

Load Transient Response
Switcher, PFM only



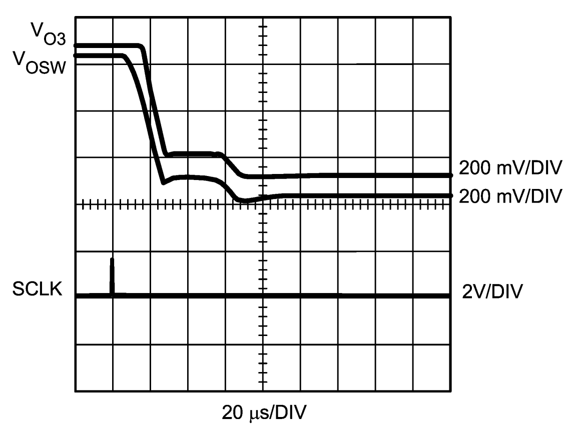
20154515

V_{OUT} Transient Response
Min to Max Transient



20154516

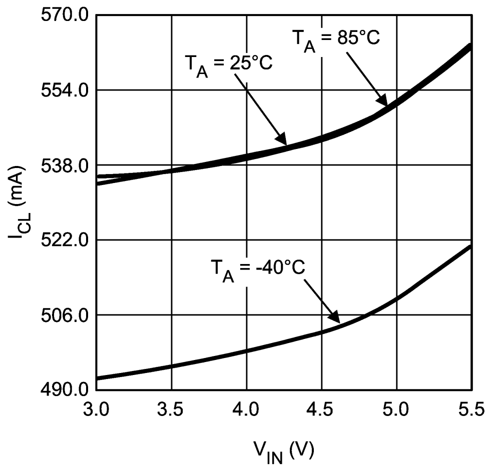
V_{OUT} Transient Response
Max to Min Transient



20154517

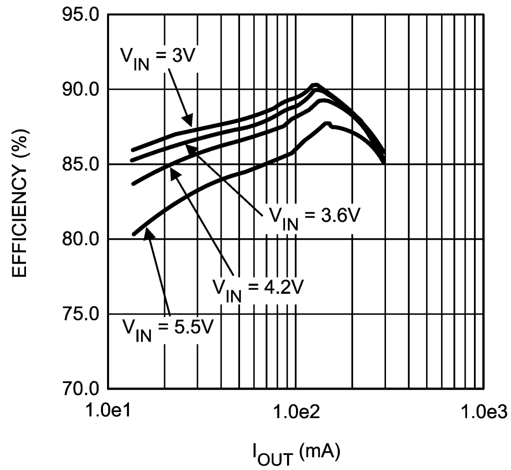
Typical Performance Characteristics Unless otherwise stated: V_{IN}=3.6V (Continued)

Switch Current Limit vs. V_{IN}



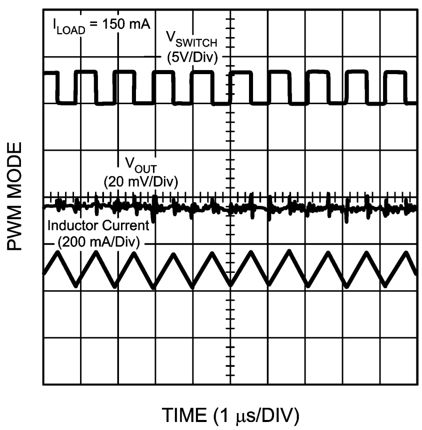
20154518

Efficiency vs. Load (Switcher)



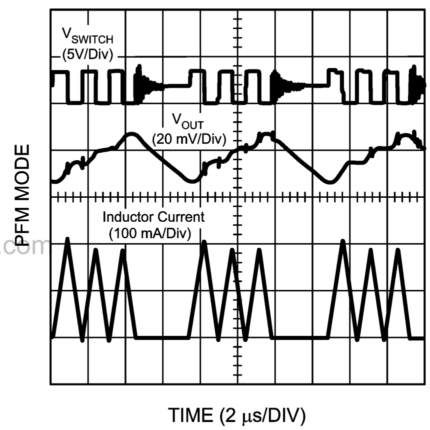
20154519

Switching Waveforms PWM



20154520

Switching Waveforms PFM



20154521

LP5550 PWI Register Map

The PWI standard supports sixteen 8-bit registers on the PWI slave. The table below summarizes these registers and shows default register bit values after reset. The following sub-sections provide additional detail on the use of each individual register.

Summary

Register Address	Register Name	Register Usage	Type	Reset Default Value							
				7	6	5	4	3	2	1	0
0x0	R0	Core voltage	R/W	0	1	1	1	1	1	1	1
0x1	R1	Unused	R/W	-	-	-	-	-	-	-	-
0x2	R2	Memory retention voltage	R/W	0	1	1	0	0	-	-	-
0x3	R3	Status register	R/O	0	0	0	0	1	1	1	1
0x4	R4	PWI version number	R/O	0	0	0	0	0	0	0	1
0x5	R5	Unused	R/W	-	-	-	-	-	-	-	-
0x6	R6	Unused	R/W	-	-	-	-	-	-	-	-
0x7	R7	LDO2 voltage	R/W	0	1	1	1	1	-	-	-
0x8	R8	LDO1 voltage	R/W	0	0	1	0	1	-	-	-
0x9	R9	PFM/PWM force	R/W	0	0	-	-	-	-	-	-

LP5550 PWI Register Map (Continued)

Summary (Continued)

Register Address	Register Name	Register Usage	Type	Reset Default Value							
				7	6	5	4	3	2	1	0
0xA	R10	Unused	R/W	-	-	-	-	-	-	-	-
0xB	R11	Unused	R/W	-	-	-	-	-	-	-	-
0xC	R12	Unused	R/W	-	-	-	-	-	-	-	-
0xD	R13	Unused	R/W	-	-	-	-	-	-	-	-
0xE	R14	Unused	R/W	-	-	-	-	-	-	-	-
0xF	R15	Reserved	R/W	-	-	-	-	-	-	-	-

R0 - Core Voltage Register

Address 0x0

Type R/W

Reset Default 8h'7F

Bit	Field Name	Description or Comment	
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.	
6:0	Voltage	Core voltage value. Default value is in **bold**.	
		Voltage Data Code [7:0]	Voltage Value (V)
		7h'00	0.6
		7h'xx	Linear scaling
		7h'7f	**1.2** (default)

R1 - Unused Register

Address 0x1

Type R/W

Reset Default 8h'00

Bit	Field Name	Description or Comment
7:0	Unused	Write transactions to this register are ignored. Read transactions will return a "No Response Frame." A no response frame contains all zeros (see PWI 1.0 specification).

R2 – VO3 Voltage Register (Memory Retention Voltage)

Address 0x2

Type R/W

Reset Default 8h'60

Bit	Field Name	Description or Comment
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.

R2 – VO3 Voltage Register (Memory Retention Voltage) (Continued)

Bit	Field Name	Description or Comment	
6:3	Voltage	Fixed voltage value. A code of all ones indicates maximum voltage while a code of all zero indicates minimum voltage. Default value is in **bold**.	
		Voltage Data Code [6:3]	Voltage Value (volts)
		4h'0	0.6
		4h'1	0.65
		4h'2	0.7
		4h'3	0.75
		4h'4	0.8
		4h'5	0.85
		4h'6	0.9
		4h'7	0.95
		4h'8	1
		4h'9	1.05
		4h'A	1.1
		4h'B	1.15
		4h'C	**1.20** (default)
		4h'D	1.25
		4h'E	1.3
		4h'F	1.35
2:0	Unused	These bits are fixed to '0'. Reading these bits will result in a '000'. Any data written into these bits using the Register Write command is ignored.	

R3 - Status Register

Address 0x3

Type Read Only

Reset Default 8h'0F

Bit	Field Name	Description or Comment
7	Reserved	Reserved, read returns 0
6	Reserved	Reserved, read returns 0
5	User Bit	Unused, read returns 0
4	User Bit	Unused, read returns 0
3	Fixed OK	Unused, read returns 1
2	IO OK	Unused, read returns 1
1	Memory OK	Unused, read returns 1
0	Core OK	Unused, read returns 1

R4 - PWI Version Number Register

Address 0x4

Type Read Only

Reset Default 8h'01

Bit	Field Name	Description or Comment
7:0	Version	Read transaction will return 8h'01 indicating PWI 1.0 specification. Write transactions to this register are ignored.

R5-R6 - Unused Registers

Address 0x5, 0x6

Type R/W

Reset Default 8h'00

Bit	Field Name	Description or Comment
7:00	Unused	Write transactions to this register are ignored. Read transactions will return a "No Response Frame." A no response frame contains all zeros (see PWI 1.0 specification).

R7 – VO2 Voltage Register (I/O Voltage)

Address 0x7

Type R/W

Reset Default 8h'78

Bit	Field Name	Description or Comment	
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.	
6:3	Voltage	Fixed voltage value. A code of all ones indicates maximum voltage while a code of all zero indicates minimum voltage. Default value is in bold.	
		Voltage Data Code [6:3]	Voltage Value (volts)
		4h'0	1.5
		4h'1	1.5
		4h'2	1.5
		4h'3	1.5
		4h'4	1.6
		4h'5	1.7
		4h'6	1.8
		4h'7	1.9
		4h'8	2
		4h'9	2.1
		4h'A	2.2
		4h'B	2.3
		4h'C	2.5
		4h'D	2.8
		4h'E	3
		4h'F	**3.3** (default)
2:0	Unused	These bits are fixed to '0'. Reading these bits will result in a '000'. Any data written into these bits using the Register Write command is ignored.	

R8 – VO1 Voltage Register (PLL/Fixed Voltage)

Address 0x8

Type R/W

Reset Default 8h'28

Bit	Field Name	Description or Comment	
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.	

R8 – VO1 Voltage Register (PLL/Fixed Voltage) (Continued)

Bit	Field Name	Description or Comment	
6:3	Voltage	Fixed voltage value. A code of all ones indicates maximum voltage while a code of all zero indicates minimum voltage. Default value is in bold.	
		Voltage Data Code [6:3]	Voltage Value (volts)
		4h'0	0.7
		4h'1	0.8
		4h'2	0.9
		4h'3	1
		4h'4	1.1
		4h'5	**1.2** (default)
		4h'6	1.3
		4h'7	1.4
		4h'8	1.5
		4h'9	1.6
		4h'A	1.7
		4h'B	1.8
		4h'C	1.9
		4h'D	2
		4h'E	2.1
		4h'F	2.2
2:0	Unused	These bits are fixed to '0'. Reading these bits will result in a 3b'000. Any data written into these bits using the Register Write command is ignored.	

R9– PFM/PWM Force Register

Address 0x9

Type R/W

Reset Default 8h'00

Bit	Field Name	Description or Comment		
7:6	PFM/PWM Force		User Register	
			PFM Force (bit 7)	PWM Force (bit 6)
		Automatic Transition	0	0
		Automatic Transition	1	1
		Forced PFM Mode	1	0
		Forced PWM Mode	0	1
5:0	Unused	These bits are fixed to '0'. Reading these bits will result in a '000000'. Any data written into these bits using the Register Write command is ignored.		

R10-R14 – Unused Registers

Address 0xA, 0xB, 0xC, 0xD, 0xE

Type R/W

Reset Default 8h'00

Bit	Field Name	Description or Comment
7:0	Unused	Write transactions to this register are ignored. Read transactions will return a "No Response Frame." A no response frame contains all zeros (see PWI 1.0 specification) frame.

R15 – Manufacturer Register

Reset Default 8h'00

Adress 0xF

Type R/W

Bit	Field Name	Description or Comment
7:0	Reserved	Do not write to this register

Operation Description

DEVICE INFORMATION

The LP5550 is a PowerWise Interface (PWI) compliant power management unit (PMU) for application or baseband processors in mobile phones or other portable equipment. It operates cooperatively with processors using National Semiconductor's Advanced Power Controller (APC) to provide Adaptive or Dynamic Voltage Scaling (AVS, DVS) which drastically improves processor efficiencies compared to conventional power delivery methods. The LP5550 consists of a high efficiency switching DC/DC buck converter to supply the AVS or DVS voltage domain, three LDOs for supplying the logic, PLL, and memory, and PWI registers and logic.

OPERATION STATE DIAGRAM

The LP5550 has four operating states: Start-up, Active, Sleep and Standby.

The Start-up state is the default state after reset. All regulators are off and PWROK output is '0'. The device will power up when the external enable-input is pulled high. After the power-up sequence LP5550 enters the Active state.

In the Active state all regulators are on and PWROK-output is '1'. Immediately after Start-up the output voltages are at their default levels. LP5550 can be turned off by supplying the Shutdown command over PWI, or by setting ENABLE and/or RESETN to '0'. The LP5550 can be switched to the Sleep state by issuing the Sleep command.

In the Sleep state the core voltage regulator is off, but the PWROK output is still '1'. The memory voltage regulator (VO3) provides the programmed memory retention voltage. LDO1 and LDO2 are on. The LP5550 can be activated from the Sleep state by giving the Wake-up command. This resumes the last programmed Active state configuration. The device can also be switched off by giving the Shutdown command, or by setting ENABLE and/or RESETN to '0'

In the Shutdown-state all output voltages are '0', and PWROK-signal is '0' as well. The LP5550 can exit the Shutdown-state if either ENABLE or RESETN is '0'. In either case the device moves to the Start-up state. See the ENABLE

Figure 6 shows the LP5550 state diagram. The figure assumes that supply voltage to the regulator IC is in the valid range.

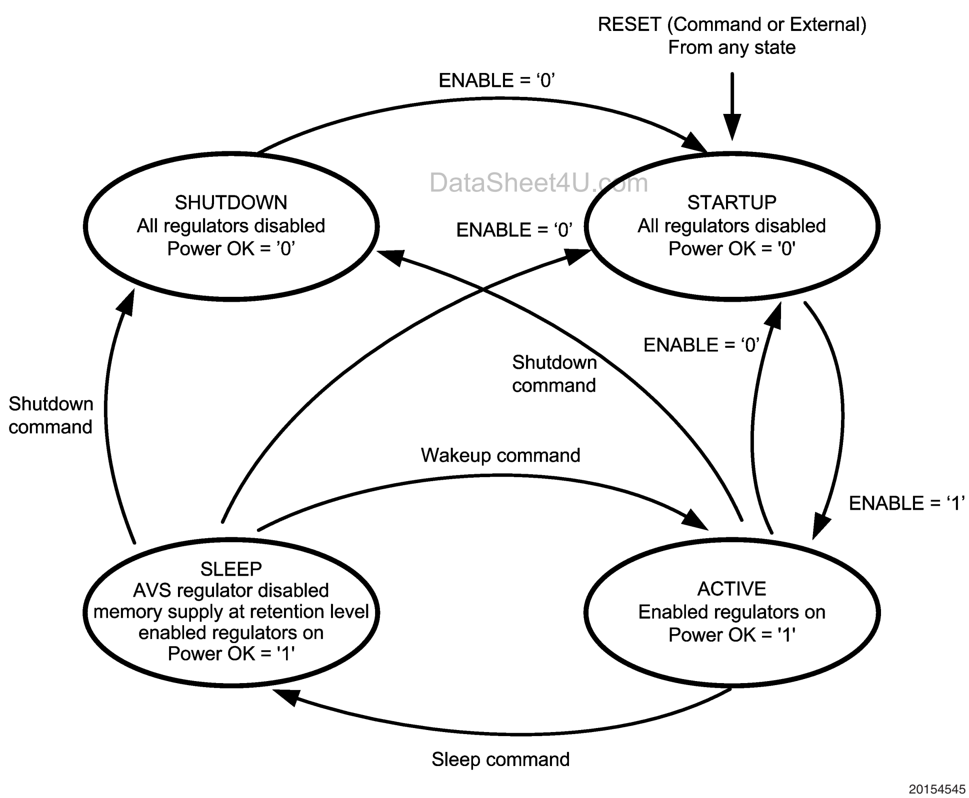


FIGURE 6. LP5550 State Diagram

Operation Description (Continued)

VOLTAGE SCALING

The LP5550 is designed to be used in a voltage scaling system to lower the power dissipation of baseband or application processors in mobile phones or other portable equipment. By scaling supply voltage with the clock frequency of a processor, dramatic power savings can be achieved. Two types of voltage scaling are supported, dynamic voltage scaling (DVS) and adaptive voltage scaling (AVS). DVS systems switch between pre-characterized voltages which are paired to clock frequencies used for frequency scaling in the processor. AVS systems track the processor performance and optimize the supply voltage to the required performance. AVS is a closed loop system that provides process and temperature compensation such that for any given processor, temperature, or clock frequency, the minimum supply voltage is delivered.

DIGITALLY CONTROLLED VOLTAGE SCALING

The LP5550 delivers fast, controlled voltage scaling transients with the help of a digital state machine. The state machine automatically optimizes the control loop in the LP5550 switching regulator to provide large signal transients with minimal over- and undershoot. This is an important characteristic for voltage scaling systems that rely on minimal over- and undershoot to set voltages as low as possible and save energy.

LARGE SIGNAL TRANSIENT RESPONSE

The switching converter in the LP5550 is designed to work in a voltage scaling system. This requires that the converter has a well controlled large signal transient response. Specifically, the under- and over-shoots have to be minimal or zero while maintaining settling times less than 100 usec. Typical response plots are shown in the Typical Performance section.

PowerWise (TM) INTERFACE

To support DVS and AVS, the LP5550 is programmable via the low power, 2 wire PowerWise Interface (PWI). This serial interface controls the various voltages and states of all the regulators in the LP5550. In particular, the switching regulator voltage can be controlled between 0.6V and 1.2V in 128 steps (linear scaling). This high resolution voltage control affords accurate temperature and process compensation in AVS. The LDO voltages can also be set, however they are not intended to be dynamic in operation. The LP5550 supports the full command set as described in PWI 1.0 specification:

- Core Voltage Adjust
- Reset
- Sleep
- Shutdown
- Wakeup
- Register Read
- Register Write
- Authenticate
- Synchronize

PWM/PFM OPERATION

The switching converter in the LP5550 has two modes of operation: pulse width modulation (PWM) and pulse frequency modulation (PFM). In PWM the converter switches at 1MHz. Each period can be split into two cycles. During the first cycle, the high-side switch is on and the low-side switch is off, therefore the inductor current is rising. In the second cycle, the high-side switch is off and the low-side switch is on causing the inductor current to decrease. The output ripple voltage is lowest in PWM mode *Figure 7*. As the load current decreases, the converter efficiency becomes worse due to the increased percentage of overhead current needed to operate in PWM mode. The LP5550 can operate in PFM mode to increase efficiency at low loads.

By default, the part will automatically transition into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

A. The inductor valley current goes below 0 A

B. The peak PMOS switch current drops below the I_{MODE} level:

$$I_{MODE} < 26\text{ mA} + \frac{V_{IN}}{50\Omega}\text{ (typ)}$$

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between 0.8% and 1.6% (typ) above the nominal PWM output voltage. If the output voltage is below the 'high' PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage exceeds the 'high' PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The peak current in PFM mode is:

$$I_{PFM} = 117\text{ mA} + \frac{V_{IN}}{64\Omega}\text{ (typ)}$$

Operation Description (Continued)

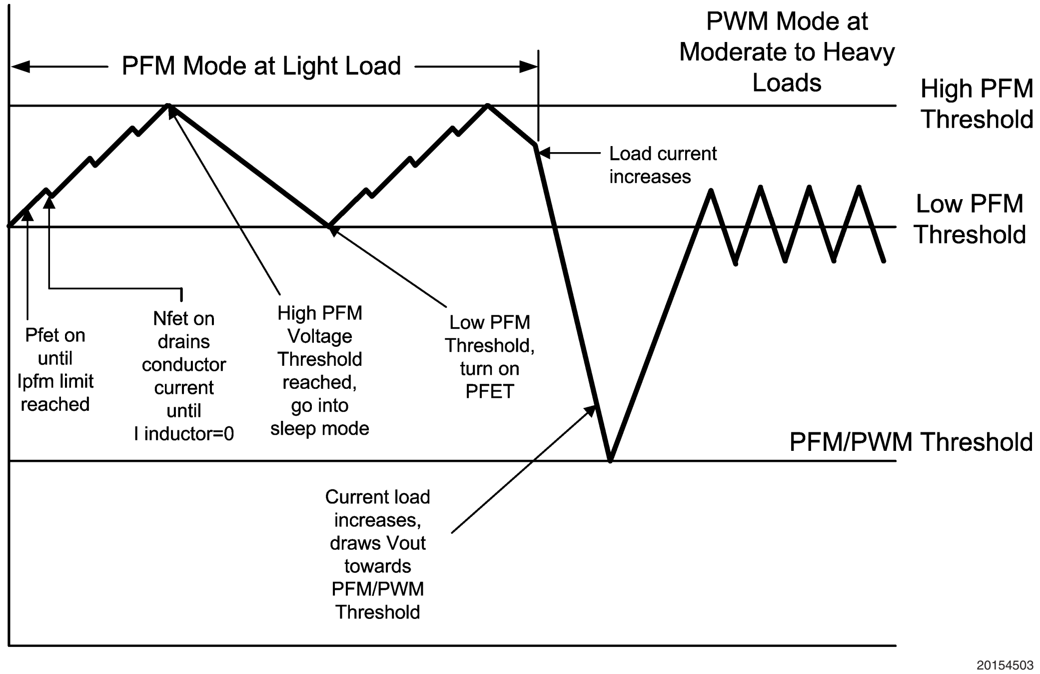


FIGURE 7. Operation in PFM Mode and Transfer to PWM Mode

Application Information

PWM/PFM FORCE REGISTER (R9)

By default, the LP5550 automatically transitions between PFM and PWM to optimize efficiency. The PWM/PFM force register (R9) provides the option to override the automatic transition and force PFM or PWM operation (see R9 – PWM/PFM Force Register declaration). Note that if the operating mode of the regulator is forced to be PFM then the switch current limit is reduced to 100 mA (50 mA average load current).

EN/RESETN

The LP5550 can be shutdown via the ENABLE or RESETN pins, or by issuing a shutdown command from PWI. To disable the LP5550 via hardware (as opposed to the PWI shutdown command), pull the ENABLE and/or the RESETN pin(s) low. To enable the LP5550, both the ENABLE and the RESETN pins must be high. Once enabled, the LP5550 engages the power-up sequence and all voltages return to their default values.

When using PWI to issue a shutdown command, the PWI will be disabled along with the regulators in the LP5550. To re-enable the part, either the ENABLE, RESETN, or both pins must be toggled (high – low – high). The part will then enter the power-up sequence and all voltages will return to their default values. *Figure 8* summarizes the ENABLE/ RESETN control.

The ENABLE and RESETN pins provide flexibility for system control. In larger systems such as a mobile phone, it can be advantageous to enable/disable a subsystem independently. For example, the LP5550 may be powering the applications processor in a mobile phone. The system controller can power down the applications processor via the ENABLE pin, but leave on other subsystems. When the phone is turned off or in a fault condition, the system controller can have a global reset command that is connected to all the subsystems (RESETN for the LP5550). However, if this type of control is not needed, the ENABLE and RESETN pins can be tied together and used as a single enable/disable pin.

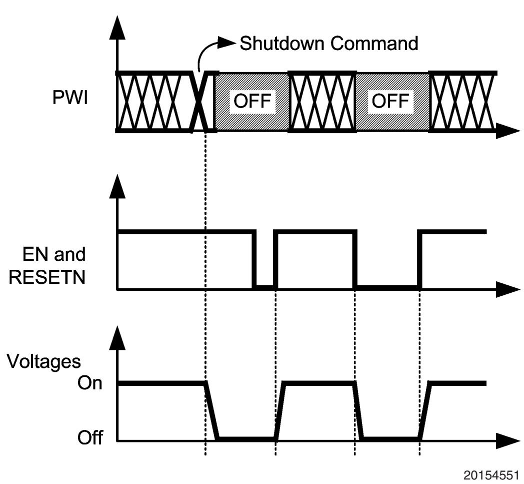


FIGURE 8. ENABLE and RESETN operation

INDUCTOR

A 10uH or 4.7uH inductor should be used with the LP5550. The inductor should be rated to handle the peak load current plus the ripple current:

$$I_{L(MAX)} = I_{LOAD(MAX)} + \Delta i_{L(MAX)}$$

$$= I_{LOAD(MAX)} + \frac{D \times (V_{IN(MAX)} - V_{OUT})}{2 \times L \times f_S}$$

$$= I_{LOAD(MAX)} + \frac{D \times (V_{IN(MAX)} - V_{OUT})}{20} \text{ (A)}, \left\{ \begin{array}{l} f_S = 1 \text{ MHz}, \\ L = 10\ \mu H \end{array} \right.$$

$$= I_{LOAD(MAX)} + \frac{D \times (V_{IN(MAX)} - V_{OUT})}{9.4} \text{ (A)}, \left\{ \begin{array}{l} f_S = 1 \text{ MHz}, \\ L = 4.7\ \mu H \end{array} \right.$$

CURRENT LIMIT

The switching converter in the LP5550 detects the peak inductor current and limits it for protection (see Electrical Characteristics table and/or Typical Performance section). To determine the average current limit from the peak current limit, the inductor size, input and output voltage, and switching frequency must be known. The LP5550 is designed to work with a 4.7uH or 10uH inductor, so:

$$I_{CL\_AVG} = I_{CL\_PK} - \Delta i_L$$

$$= I_{CL\_PK} - \frac{D \times (V_{IN} - V_{OUT})}{2 \times L \times f_S}$$

$$\approx 0.4 - \frac{D \times (V_{IN} - V_{OUT})}{20}, \left\{ \begin{array}{l} f_S = 1 \text{ MHz}, \\ L = 10\ \mu H \end{array} \right.$$

$$\approx 0.4 - \frac{D \times (V_{IN} - V_{OUT})}{9.4}, \left\{ \begin{array}{l} f_S = 1 \text{ MHz}, \\ L = 4.7\ \mu H \end{array} \right.$$

INPUT CAPACITOR

The input capacitor to the switching converter supplies the AC switching current drawn from the switching action of the internal power FETs. The input current of a buck converter is discontinuous, so the ripple current supplied by the input capacitor is large. The input capacitor must be rated to handle this current:

$$I_{RMS\_CIN} = I_{OUT} \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \text{ (A)}$$

The power dissipated in the input capacitor is given by:

$$P_{D\_CIN} = I^2_{RMS\_CIN} \times R_{ESR\_CIN} \text{ (W)}$$

The input capacitor must be rated to handle both the RMS current and the dissipated power. A 10 μF ceramic capacitor is recommended for the LP5550.

Application Information (Continued)

OUTPUT CAPACITOR

The switching converter in the LP5550 is designed to be used with a 10uF ceramic output capacitor. The dielectric should be X5R, X7R, or comparable material to maintain proper tolerances. The output capacitor of the switching converter absorbs the AC ripple current from the inductor and provides the initial response to a load transient. The ripple voltage at the output of the converter is the product of the ripple current flowing through the output capacitor and the impedance of the capacitor. The impedance of the capacitor can be dominated by capacitive, resistive, or inductive elements within the capacitor, depending on the frequency of the ripple current. Ceramic capacitors are predominately used in portable systems and have very low ESR and remain capacitive up to high frequencies.

The switcher peak - to - peak output voltage ripple in steady state can be calculated as:

$$V_{PP} = I_{LPP} \left(R_{ESR} + \frac{1}{F_S \times 8 \times C_{OUT}}\right)$$

LDO INFORMATION

The LDOs included in the LP5550 provide static supply voltages for various functions in the processor. Use the following sections to determine loading and external components.

LDO LOADING CAPABILITY

The LDOs in the LP5550 can regulate to a variety of output voltages, depending on the need of the processor. These voltages can be programmed through the PWI. Table 1 summarizes the parameters of the LP5550 LDOs.

TABLE 1. LDO Parameters

	PWI Register	Output voltage range	Recommended Maximum Output Current	Dropout Voltage (typical)	Typical Load
LDO1	R8	0.6 V – 2.2 V	100 mA	200 mV	PLL
LDO2	R7	1.5 V – 3.3 V	250 mA	150 mV	I/O
LDO3	R2	V_{OSW} + 0.05 V[1] 0.7 V – 1.35 V[2]	50 mA	200 mV	Memory/Memory retention

1. LDO3 tracks the switching converter output voltage (V_{OSW}) plus a 50 mV offset when the LP5550 is in active state.
2. LDO3 regulates at the set memory retention voltage when the LP5550 is in shutdown state.

LDO OUTPUT CAPACITOR

The output capacitor sets a low frequency pole and a high frequency zero in the control loop of an LDO. The capacitance and the equivalent series resistance (ESR) of the capacitor must be within a specified range to meet stability requirements. The LDOs in the LP5550 are designed to be used with ceramic output capacitors. The dielectric should be X5R, X7R, or comparable material to maintain proper tolerances. Use the following table to choose a suitable output capacitor:

TABLE 2. Output Capacitor Selection Guide

	Output Capacitance Range (Recommended Typical Value)	ESR range
LDO1	1 µF – 20 µF (2.2 µF)	5 mohm – 500 mohm
LDO2	2 µF – 20 µF (4.7 µF)	5 mohm – 500 mohm
LDO3	0.7 µF – 2.2 µF (1.0 µF)	5 mohm– 500 mohm

Application Information (Continued)

BOARD LAYOUT CONSIDERATIONS

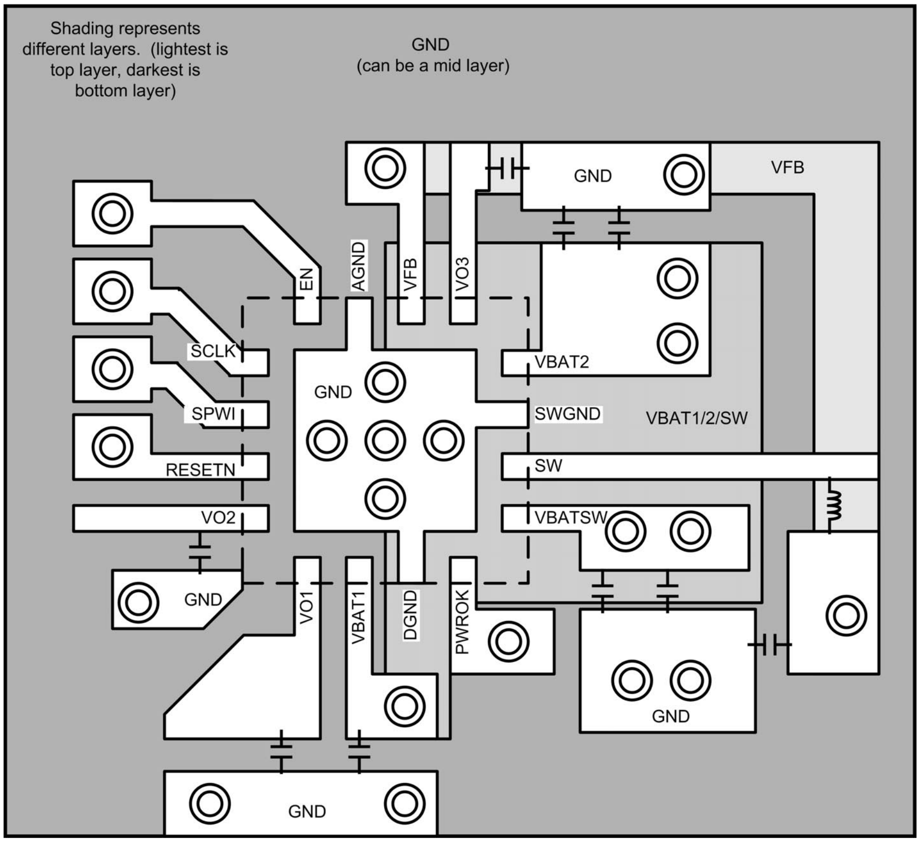
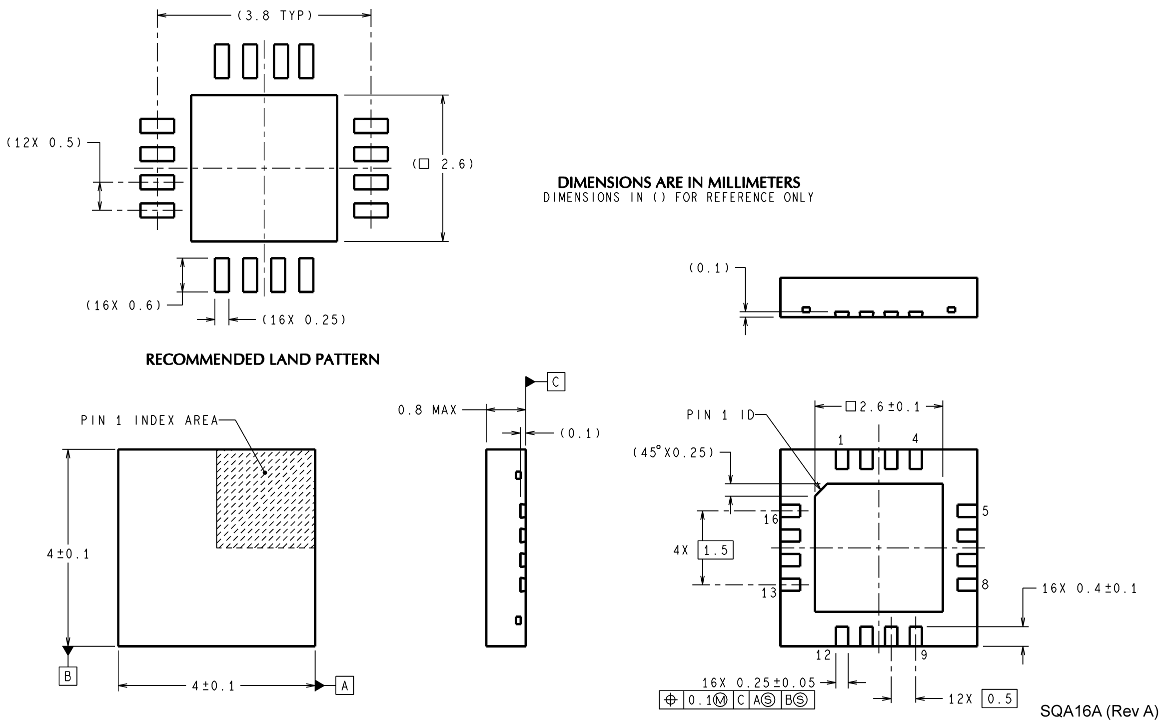


FIGURE 9. Board Layout Design Recommendations for the LP5550

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead LLP Package
NS Package Number SQA16A

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