Document Title

32K X 8 BIT HIGH SPEED CMOS SRAM

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	November 9, 2001	Preliminary

Preliminary — *32K X 8 BIT HIGH SPEED CMOS SRAM*

Features

- Single +3.3V power supply
- Access times: 12/15 ns (max.)
- Current: Operating: 120mA (max.)
  Standby: 5mA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL compatible
- Common I/O using three-state output
- Data retention voltage: 2V (min.)
- Available in 28-pin SOJ package

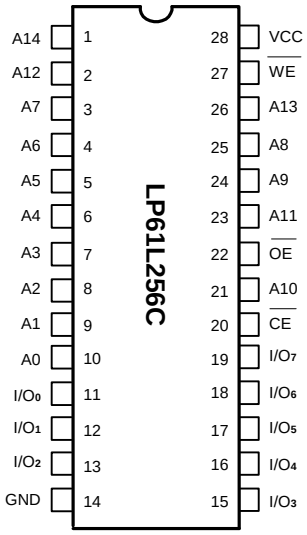
General Description

The LP61L256C is a high-speed, low-power 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates on a single 3.3V power supply. It is built using high performance CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

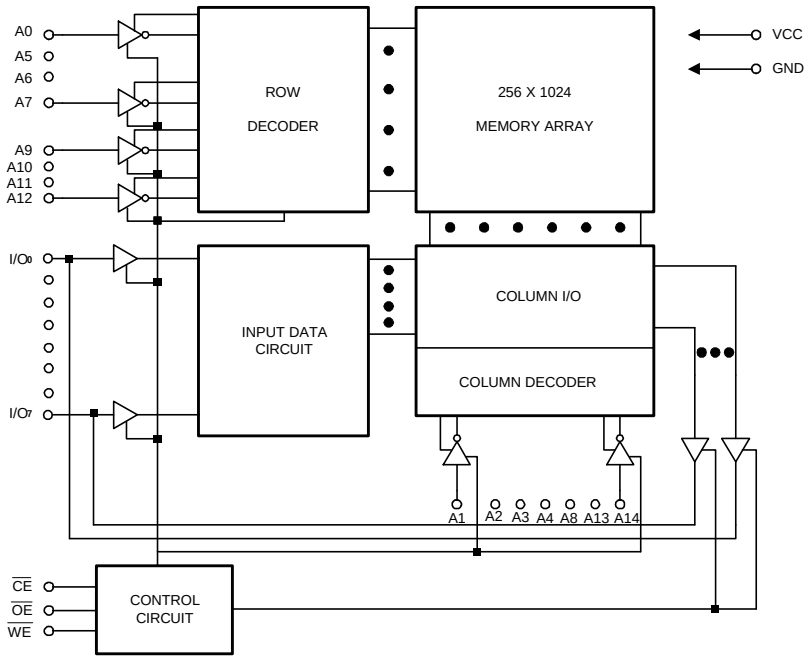
Minimum standby power is drawn by this device when $\overline{CE}$ is at a high level, independent of the other input levels.
Data retention is guaranteed at a power supply voltage as low as 2V.

Pin Configurations

■ **SOJ**



Block Diagram



Pin Descriptions - SOJ

Pin No.	Symbol	Description
1 - 10, 21, 23 - 26	A0 - A14	Address Inputs
11 - 13, 15 - 19	I/O_0 - I/O_7	Data Inputs/Outputs
14	GND	Ground
28	VCC	Power Supply
20	$\overline{CE}$	Chip Enable
22	$\overline{OE}$	Output Enable
27	$\overline{WE}$	Write Enable

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	3.0	3.3	3.6	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	VCC + 0.3	V
V_{IL}	Input Low (1) Voltage	-0.5	0	+0.8	V
C_L	Output Load	-	-	30	pF

Absolute Maximum Ratings*

VCC to GND . . . . . -0.5V to +4.6V
IN, IN/OUT Volt to GND . . . . . -0.5V to VCC +0.5V
Operating Temperature, Topr . . . . . 0°C to +70°C
Storage Temperature, Tstg . . . . . -55°C to +125°C
Temperature Under Bias, Tbias . . . . . -10°C to +85°C
Power Dissipation, P_T 1.0W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to + 70°C, VCC = 3.3V ± 10%, GND = 0V)

Symbol	Parameter	LP61L256C-12/15		Unit	Conditions
		Min.	Max.		
$\lvert I_{LI} \rvert$	Input Leakage	-	2	µA	V_{IN} = GND to VCC
$\lvert I_{LO} \rvert$	Output Leakage	-	2	µA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to VCC
I_{CC1} (2)	Dynamic Operating Current	-	120	mA	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0 mA Min. Cycle, Duty = 100%
I_{SB}	Standby Power Supply Current	-	30	mA	$\overline{CE}$ = V_{IH}
I_{SB1}		-	5	mA	$\overline{CE}$ ≥ VCC - 0.2V V_{IN} ≥ VCC -0.2V or V_{IN} ≤ 0.2V
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = -4 mA

Notes: 1. V_{IL} = -3.0V for pulses less than 20 ns.
2. I_{CC1} is dependent on output loading, cycle rates, and Read/Write patterns.

Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	High Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	High Z	I_{CC1}
Read	L	L	H	D_{OUT}	I_{CC1}
Write	L	X	L	D_{IN}	I_{CC1}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance		10	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		10	pF	$V_{I/O}$ = 0V

* These parameters are sampled and not 100% tested.

AC Characteristics (T_A = 0°C to +70°C, VCC = 3.3V ± 10%)

Symbol	Parameter	LP61L256C-12		LP61L256C-15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	12	-	15	-	ns
t_{AA}	Address Access Time	-	12	-	15	ns
t_{ACE}	Chip Enable Access Time	-	12	-	15	ns
t_{OE}	Output Enable to Output Valid	-	6	-	8	ns
t_{CLZ}	Chip Enable to Output in Low Z	3	-	3	-	ns
t_{OLZ}	Output Enable to Output in Low Z	0	-	0	-	ns
t_{CHZ}	Chip Disable Output in High Z	0	6	-	8	ns
t_{OHZ}	Output Disable to Output in High Z	0	6	0	8	ns
t_{OH}	Output Hold from Address Change	3	-	3	-	ns

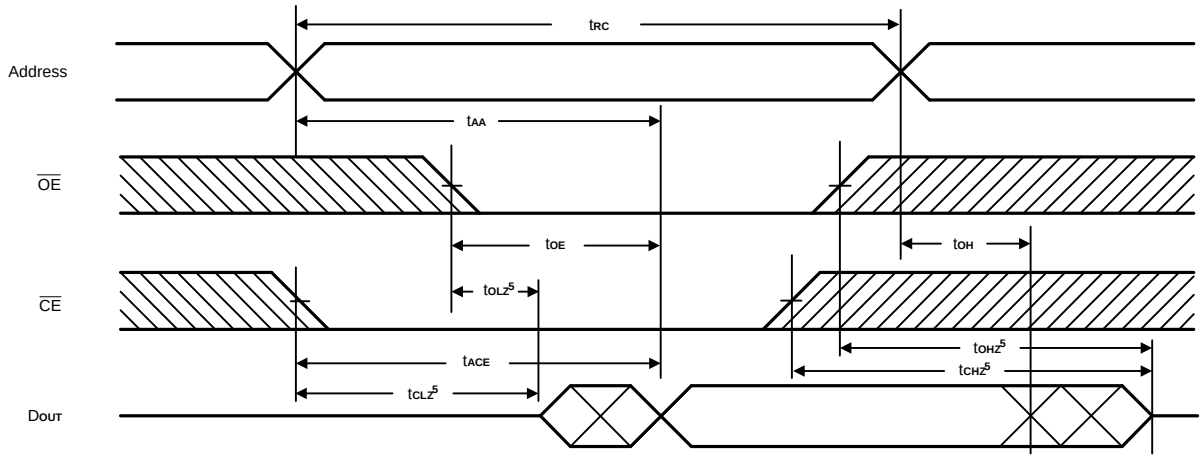
AC Characteristics (continued)

Symbol	Parameter	LP61L256C-12		LP61L256C-15		Unit
		Min.	Max.	Min.	Max	
Write Cycle						
t_{WC}	Write Cycle Time	12	-	15	-	ns
t_{CW}	Chip Enable to End of Write	10	-	12	-	ns
t_{AS}	Address Setup Time of Write	0	-	0	-	ns
t_{AW}	Address Valid to End of Write	10	-	12	-	ns
t_{WP}	Write Pulse Width	10	-	12	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	ns
t_{WHZ}	Write to Output in High Z	0	6	0	8	ns
t_{DW}	Data to Write Time Overlap	6	-	7	-	ns
t_{DH}	Data Hold from Write Time	0	-	0	-	ns
t_{OW}	Output Active from End of Write	3	-	3	-	ns

Notes: t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levles.

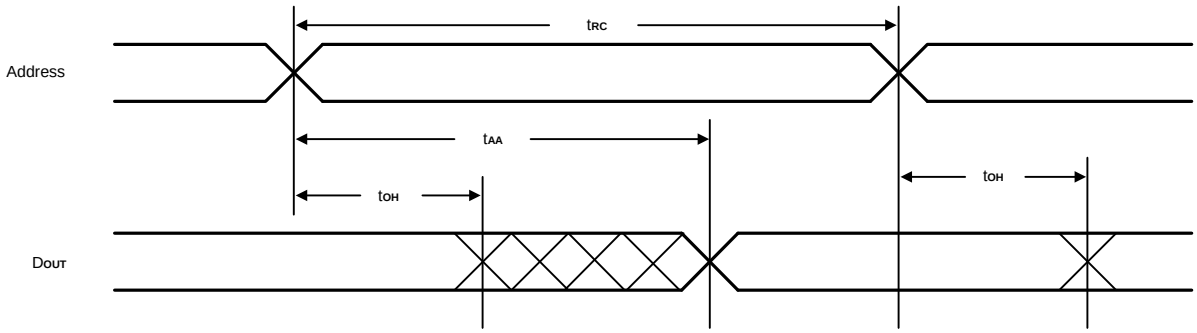
Timing Waveforms

Read Cycle 1[(1)]

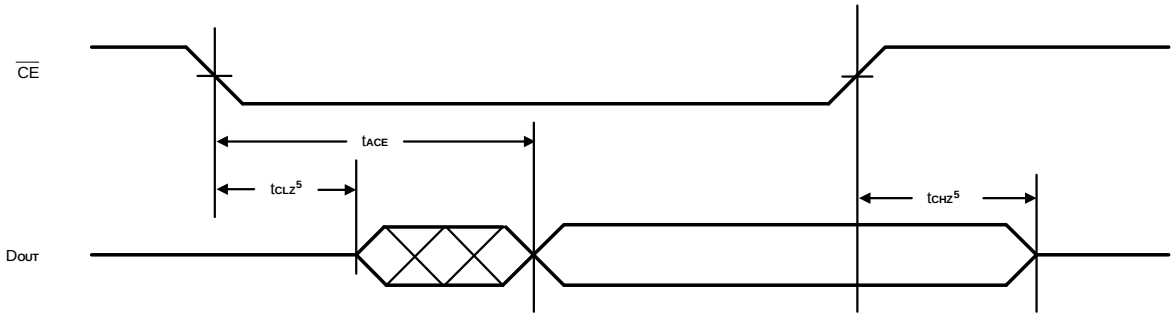


Timing Waveforms (continued)

Read Cycle 2[1, 2, 4]



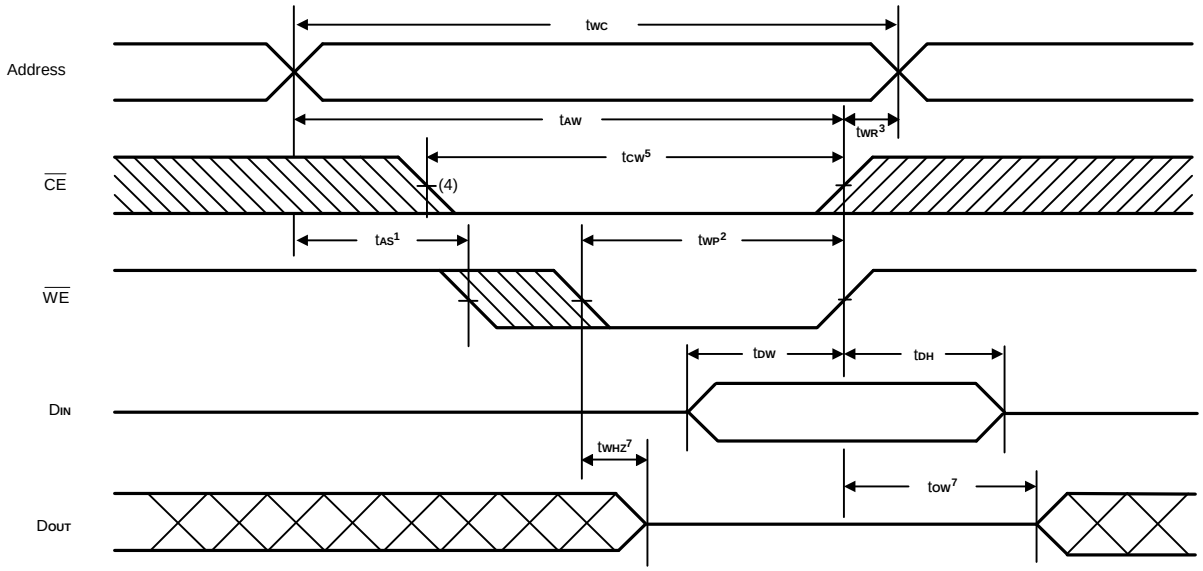
Read Cycle 3[1, 3, 4,]



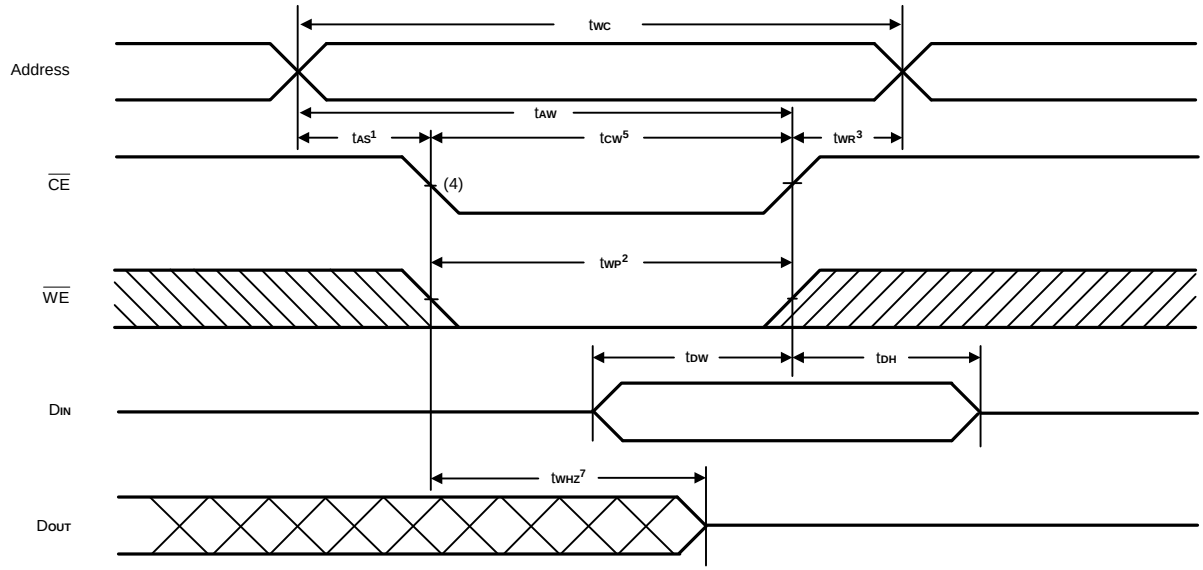
Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

Timing Waveforms (continued)

Write Cycle 1[6]
(Write Enable Controlled)



Write Cycle 2
(Chip Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}) of a low $\overline{CE}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earliest of $\overline{CE}$ or $\overline{WE}$ going high to the end of the Write cycle
4. If the $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. t_{CW} is measured from the later of $\overline{CE}$ going low to the end of Write.
6. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})
7. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Time	2 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2

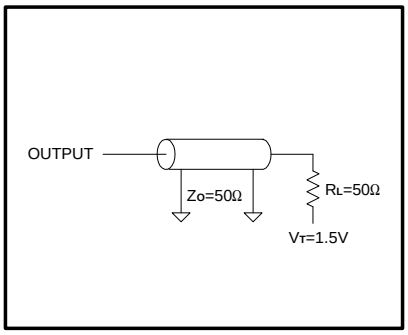


Figure 1. Output Load

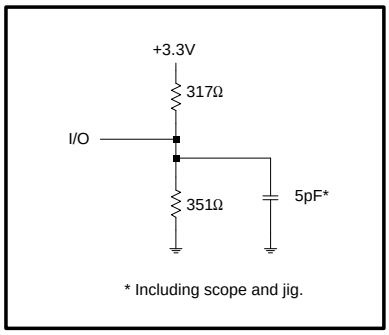


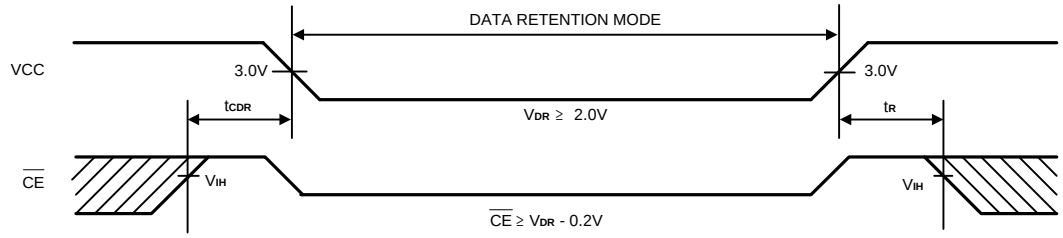
Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}

Data Retention Characteristics (T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{DR}	VCC for Data Retention	2	3.6	V	$\overline{CE} \geq$ VCC - 0.2V
I_{CCDR}	Data Retention Current	-	2	mA	VCC = 2.0V $\overline{CE} \geq$ VCC - 0.2V $V_{IN} \geq$ VCC - 0.2V or $V_{IN} \leq$ 0.2V
t_{CDR}	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
t_R	Operation Recovery Time	t_{RC}*	-	ns	

t_{RC} = Read Cycle Time

Low VCC Data Retention Waveform



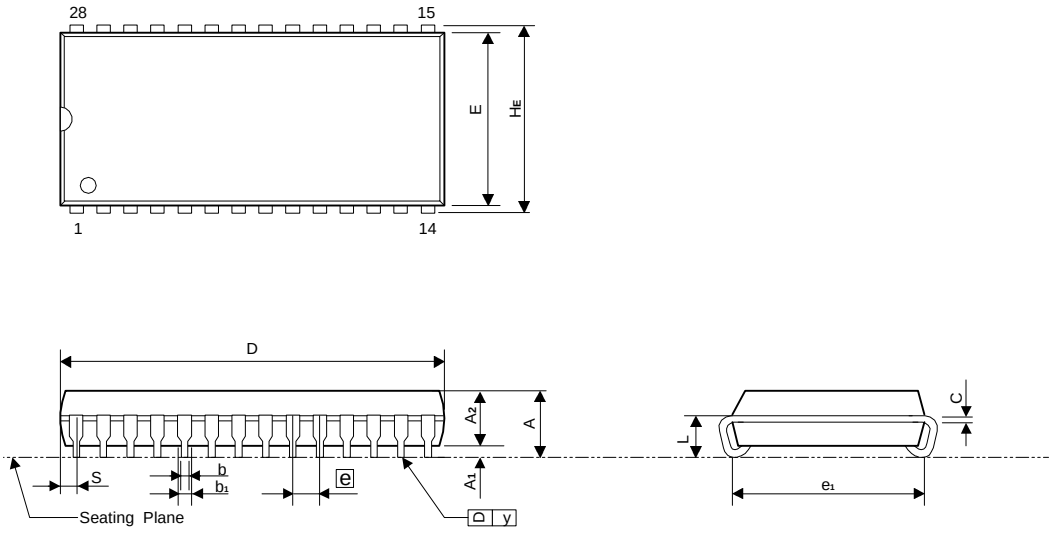
Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
LP61L256CS-12	12	120	5	28L SOJ
LP61L256CS-15	15	120	5	28L SOJ

Package Information

SOJ 28L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.140	-	-	3.56
A_1	0.027	-	-	0.69	-	-
A_2	0.095	0.100	0.105	2.41	2.54	2.67
b_1	0.028 TYP			0.71 TYP		
b	0.018 TYP			0.46 TYP		
C	0.010 TYP			0.25 TYP		
D	-	0.710	0.730	-	18.03	18.54
E	0.295	0.300	0.305	7.49	7.62	7.75
e	0.050 BSC			1.27 BSC		
e_1	0.255	0.265	0.275	6.48	6.73	6.99
H_E	0.329	0.337	0.345	8.36	8.56	8.76
L	0.077	0.087	0.097	1.96	2.21	2.46
S	-	-	0.045	-	-	1.14
y	-	-	0.004	-	-	0.10

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.