High Efficiency 1.4A/30VBoost DC/DC Convertor

General Description

The LP6320A is a 1.2MHz PWM boost switching regulator designed for constant-voltage boost applications. The LP6230A can drive a string of up to 30V. The LP6230A implements a constant frequency 1.2MHz PWM control scheme. The high frequency PWM operation also saves board space by reducing external component sizes. The LP6230A features automatic shifting to pulse frequency modulation mode at light loads.Highly integration and internal compensation network minimizes as 6 external component counts. Optimized operation frequency can meet the requirement of small LC filters value and low operation current with high efficiency.

The LP6230A includes under-voltage lockout, current limiting, and thermal overload protection to prevent damage in the event of an output overload. The LP6230A is available in a small 8-pin MSOP8 package.

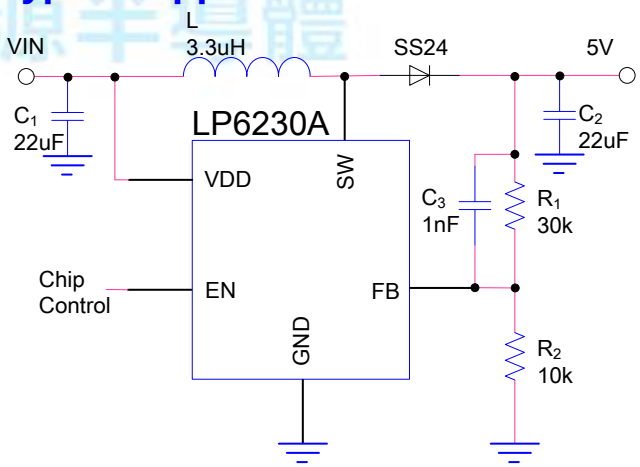
Features

- Up to 92% efficiency
- Shut-down current:<1uA
- Output voltageUp to 30V
- Internal Compensation
- 1.2MHz fixed frequency switching
- High switch on current: 1.4A
- Available in MSOP8Package

Applications

- Battery products
- Host Products
- Panel

Typical Application Circuit



Ordering Information

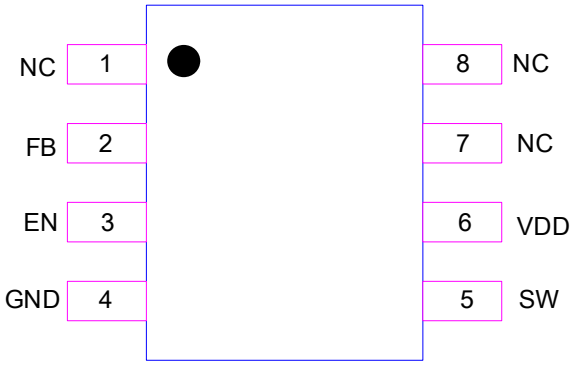
LP6230A □ □ □

- F: Pb-Free
- Package Type
  - MS: MSOP-8

Marking Information

Device	Marking	Package	Shipping
LP6230AMSF	LPS LP6230 YWX	MSOP-8	3K/REEL

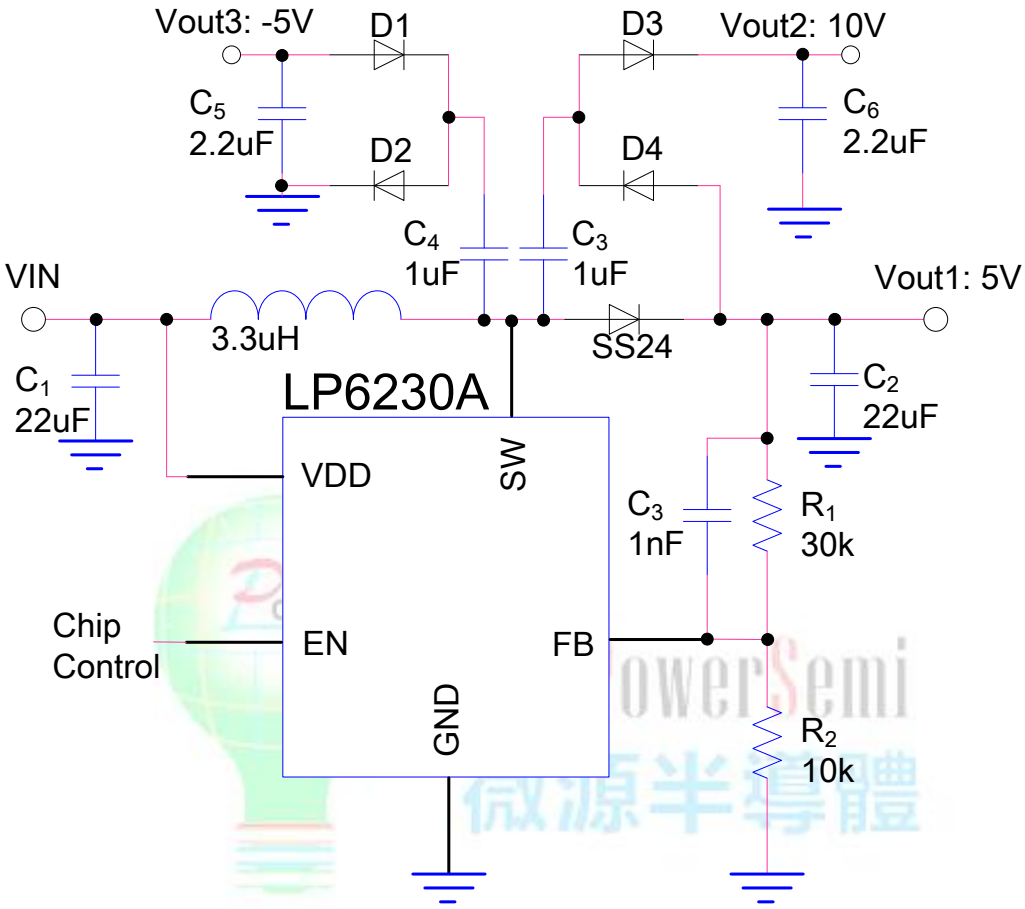
Pin Configurations



Functional Pin Description

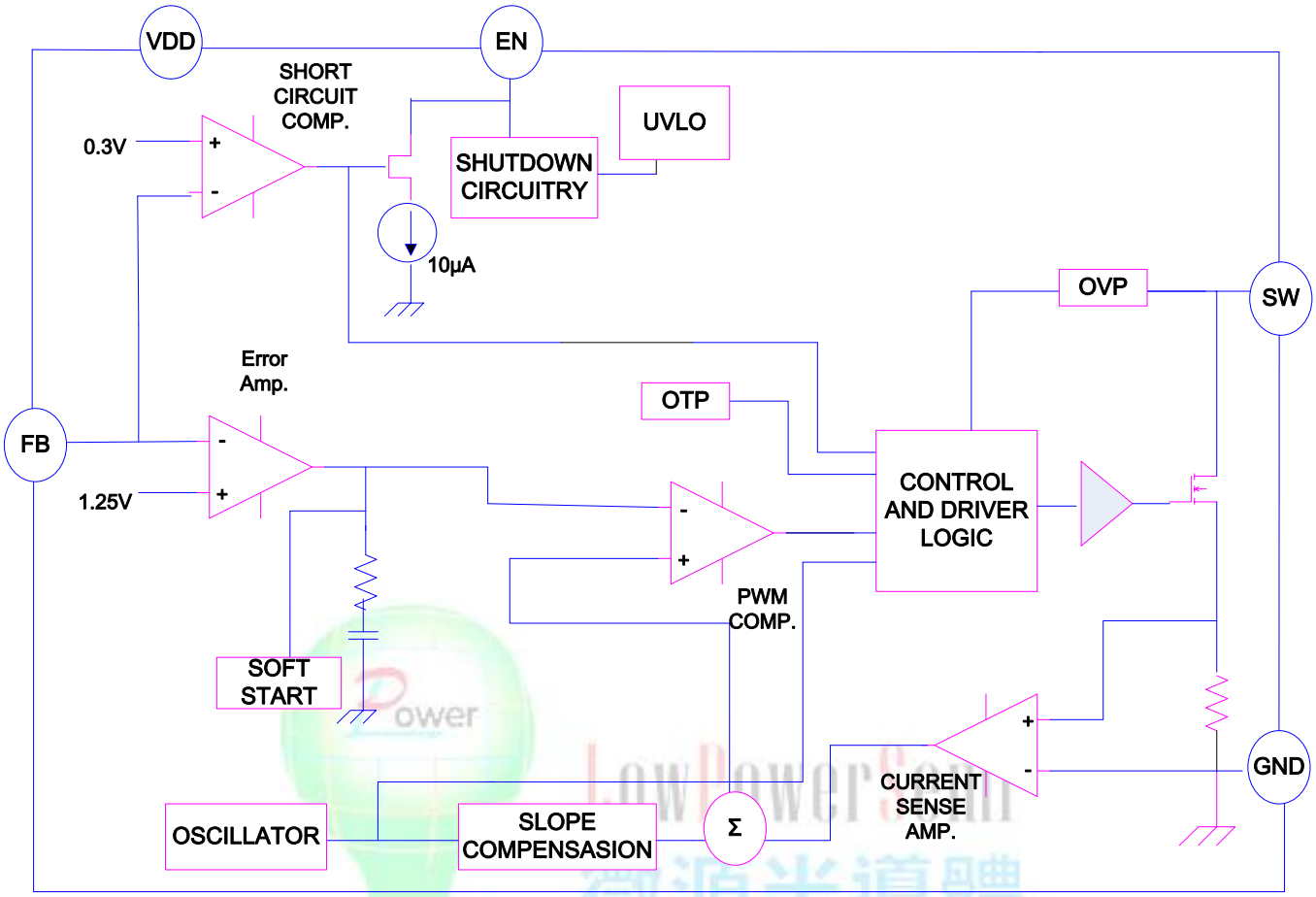
PIN	PIN Name	Description
1,7,8	NC	No Connection.
2	FB	Regulation Feedback Input. Connect to an external resistive voltage divider from the output to FB to set the output voltage.
3	EN	Regulator On/off Control Input. A logic high input(VEN>1.4V) turns on the regulator. A logic low input(VEN<0.4V) puts the LP6230A into low current shutdown mode.
4	GND	Ground.
5	SW	Switching pin.
6	VDD	Power Supply pin.

Application Circuit



LP6230A Application Circuit of LCD Bias

Function Block Diagram



Absolute Maximum Ratings Note 1

- ✧ Input to GND ---------- -03V to 6V
- ✧ SW Pin to GND ---------- 36V
- ✧ Other Pin to GND (V_{FB},V_{EN}) ---------- 6V
- ✧ Operation Junction Temperature Range ---------- 150℃
- ✧ Operation Ambient Temperature Range ---------- -40℃ to 85℃
- ✧ Lead Temperature (Soldering, 10 sec.) ---------- 260℃

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Maximum Power Dissipation (MSOP8,PD,T_A=25℃) ---------- 900mW
- ✧ Thermal Resistance (θ_{JA}, ---------- 165℃/W

Electrical Characteristics

(Vin=3.3V,Vout=5V,Cin=10uF,Cout=22uF,L1=4.7uH)

Parameter	Conditions	LP6230A			Units
		Min	Typ	Max	
Supply Voltage		2.7		5.5	V
Output Voltage Range		2.7		30	V
Supply Current(Shutdown)	VEN=VOUT=0V,VSW=5V		0.1	1	uA
Supply Current			430	550	uA
Feedback Voltage		1.22	1.25	1.28	V
Feedback Input Current	VFB=1.25V		50		nA
Switching Frequency			1200		KHz
Maximum Duty Cycle		93			%
EN Input Low Voltage				0.4	V
EN Input High Voltage		1.4			V
Low-side Current Limit			1.4		A
High-side On Resistance	Vout=3.3V		0.4		Ω
Mosfet voltage			30		V

Operation Information

The LP6230A uses a fixed frequency, peak current mode boost regulator architecture to regulate voltage at the feedback pin. At the start of each oscillator cycle the MOSFET is turned on through the control circuitry. To prevent sub-harmonic oscillations at duty cycles greater than 50 percent, a stabilizing ramp is added to the output of the current sense amplifier and the result is fed into the negative input of the PWM comparator. When this voltage equals The output voltage of the error amplifier the power MOSFET is turned off. The voltage at the output of the error amplifier is an amplified version of the difference between the 1.25V bandgap reference voltage and the feedback voltage. In this way the peak current level keeps the output in regulation. If the feedback voltage starts to drop, the output of the error amplifier increases. These results in more current to flow through the power MOSFET, thus increasing the power delivered to the output. TheLP6230A has internal soft start to limit the amount of input current at startup and to also limit the amount of overshoot on the output.

Setting the Output Voltage

Set the output voltage by selecting the resistive voltage divider ratio. The voltage divider drops the output voltage to the 1.25V feedback voltage. Use a 100K resistor for R2 of the voltage divider. Determine the high-side resistor R1 by the equation:

$$Vout=(R1/R2+1)\times VFB$$

$$Vout=(R1/R2+1)\times 1.25V$$

Diode Selection

To achieve high efficiency, Schottky diode is good choice for low forward drop voltage and fast switching time. The output diode rating should be able to handle the maximum output voltage, average power dissipation and the pulsating diode peak current.

Input Capacitor Selection

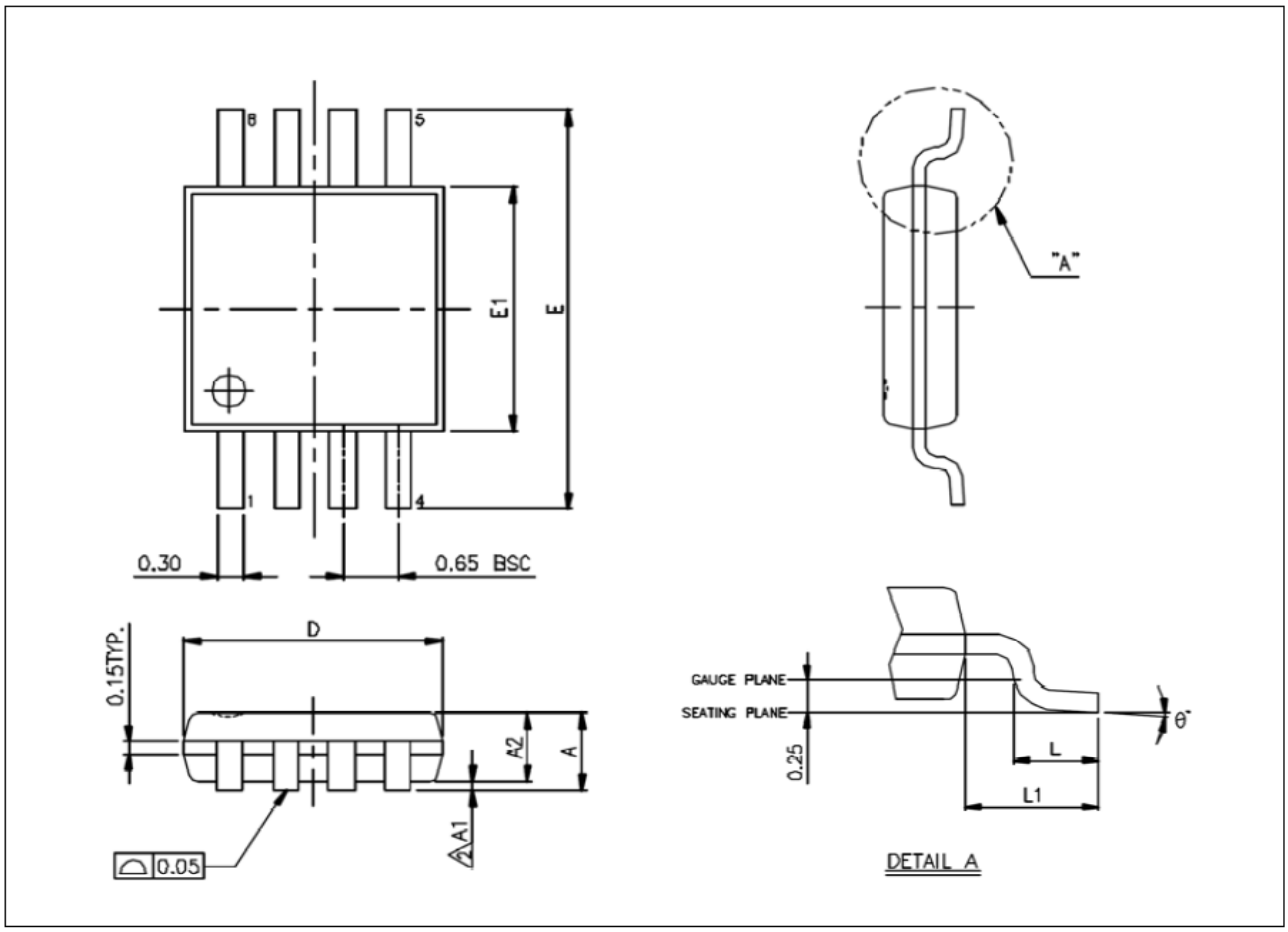
For better input bypassing, low-ESR ceramic capacitors are recommended for performance. A 10μF input capacitor is sufficient for most applications. For a lower output power requirement application, this value can be decreased.

Layout Guideline

For high frequency switching power supplies, the PCB layout is important step in system application design. In order to let IC achieve good regulation, high efficiency and stability, it is strongly recommended the power components should be placed as close as possible. The set races should be wide and short. The feedback pin and then works of feedback and compensation should keep away from the power loops, and be shielded with a ground trace or plane to prevent noise coupling.Input and Output capacitors should be placed close to the IC and connected to ground plane to reduce noise coupling.

Packaging Information

MSOP-8L



Unit: mm

Symbols	Min. (mm)	Max. (mm)
A		1.100
A1	0.000	0.150
A2	0.750	0.950
D	3.000 BSC	
E	4.900 BSC	
E1	3.000 BSC	
L	0.400	0.800
L1	0.950 REF	
θ°	0°	8°

Note:

1. Package dimensions are in compliance with JEDEC outline: MO-187 AA.
2. Dimension “D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E1” does not include inter-lead flash or protrusions.