

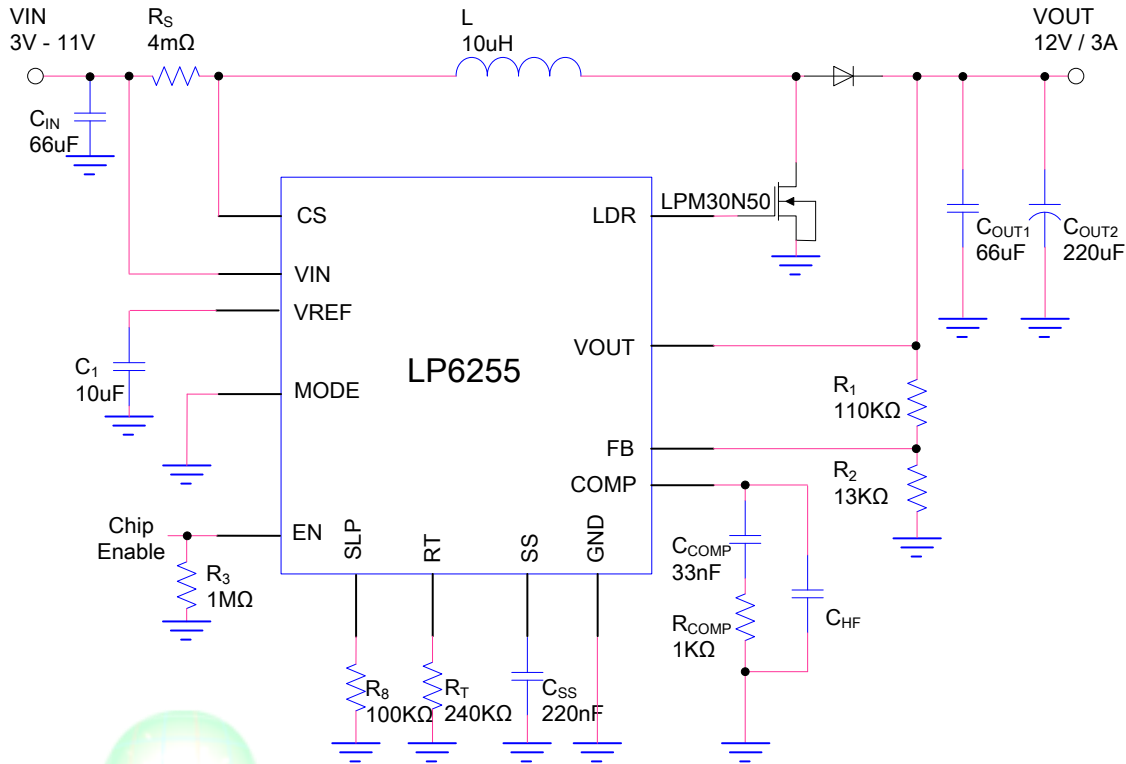


Functional Pin Description

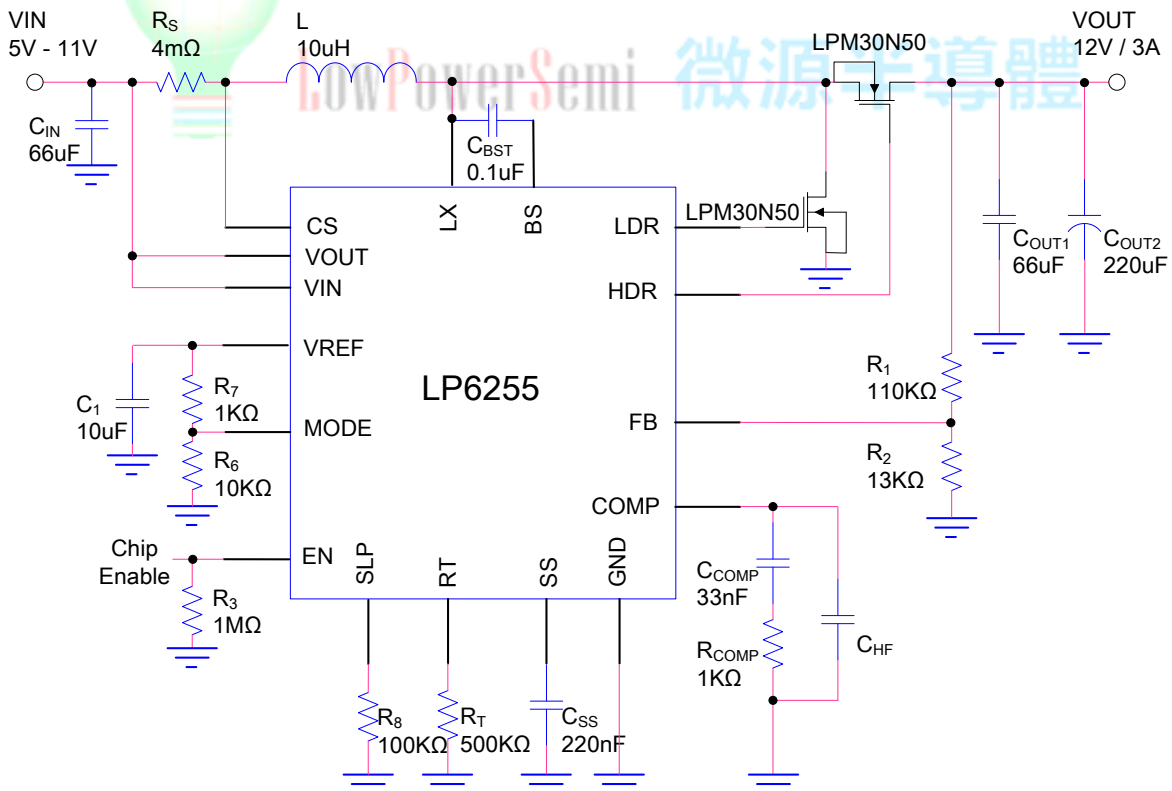
Pin	Name	Description
1	COMP	Compensation pin. The loop compensation network should be connected between this pin and the GND pin.
2	FB	Feedback input. Connect to an external resistive voltage divider from the output to FB to set the output voltage. The pin is 1.31V. $V_{OUT}=1.31 \times (R_1/R_2+1)V$.
3	SLP	Slope compensation is programmed by an external resistor between SLP and the GND.
7,18	NC	No Connector. There should not connect ground or VIN to it. Leaving it float is OK.
4,13	VREF	Internal bias supply. Decouple with a 10uF ceramic capacitor as close to the pin as possible.
6	EN	Chip enable pin. If the EN pin is below 1V, the regulator is in the shutdown mode with all functions disabled. If the EN pin voltage is above 2.2V, the startup sequence begins. EN exceeds 2.2 V and flows through the external EN resistors to provide hysteresis. The EN pin should not be left floating.
8	MODE	Switching mode selection pin. When MODE pin voltage is greater than 1.4 V, diode emulation mode threshold, forced PWM mode is enabled, allowing current to flow in either direction through the high-side N-channel MOSFET switch. If the MODE pin is below 0.1V or grounded, the controller still operates in diode emulation mode, but the skip cycle comparator will not be triggered in normal operation, this enables pulse skipping operation at light load.
9	RT	The internal oscillator frequency is programmed by an external resistor between RT and the GND. The internal oscillator can be synchronized to an external clock by applying a positive pulse signal into this pin.
10	SS	Soft start pin. Connect a capacitor to this pin. The capacitor is charged with a constant current.
5,11	GND	Power Ground pin.
12	LDR	Pin for driving external N-Channel MOS which cooperates with external NMOS.
14	VOUT	This pin needs connection to output node.
15	LX	Connect inductor between LX and VIN. Make these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot.
16	HDR	Pin for driving external N-Channel MOS which work as switch tube.
17	BST	Bootstrap pin to power the MOS driver. Connect a capacitor between this pin and LX pin.
19	CS	Connect to negative-side of current sense resistor as voltage detective pin cooperating with VIN pin.
20	VIN	Voltage supply pin.



Typical Application Circuit



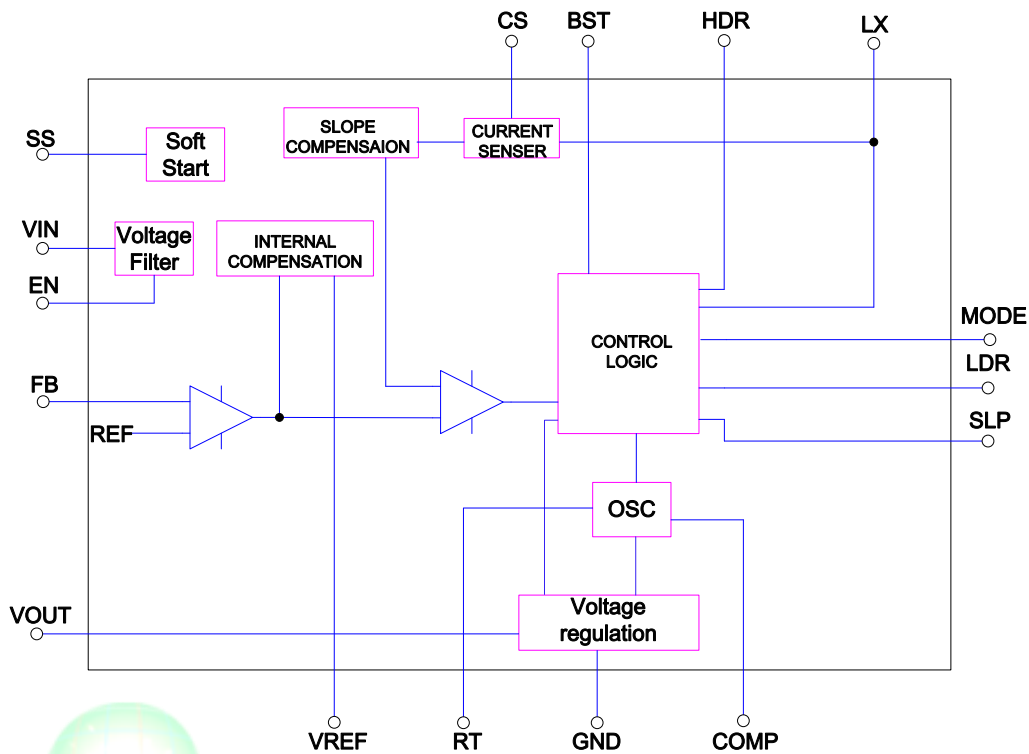
Application in asynchronous mode



Application in synchronous mode @ VIN>5V



Function Block Diagram



Absolute Maximum Ratings ^{Note 1}

- ✧ Input, CS to GND ----- -0.3V to 33V
- ✧ HDR, BST to GND ----- -0.3V to 40V
- ✧ LX to GND ----- -0.3V to 35V
- ✧ OUT to GND ----- -0.3V to 33V
- ✧ Other Pin to GND ----- -0.3V to 6V
- ✧ Maximum Junction Temperature ----- 150°C
- ✧ Operating Ambient Temperature Range ----- -40°C to 85°C
- ✧ Maximum Soldering Temperature (at leads, 10 sec) ----- 260°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Maximum Power Dissipation (TQFN-20, PD, T_A=25°C) ----- 1.2W
- ✧ Thermal Resistance (TQFN-20, J_A) ----- 95°C/W

ESD Susceptibility

- ✧ HBM(Human Body Mode) ----- 2KV
- ✧ MM(Machine Mode) ----- 200V



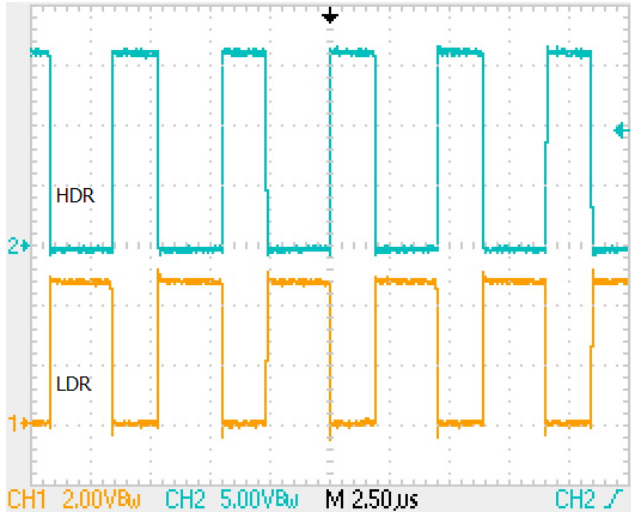
Electrical Characteristics

($V_{IN}=5V$, $V_{OUT}=12V$, $L=10\mu H$, $R_1=123K$, $R_2=15K$, $R_T=400K$, $R_{SLP}=51K$)

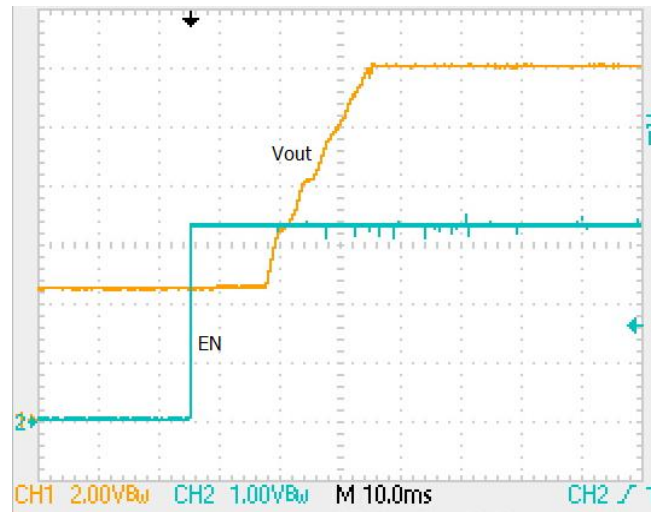
Parameter	Condition	Min	Typ	Max	Units
Supply Voltage		2.5		30	V
Output Voltage Range		2.8		30	V
VREF Voltage		4.5	5	5.2	V
Supply Current(Shutdown)	$V_{EN}=0V$		10	30	μA
Supply Current	$V_{FB}=1V$			2.5	mA
Voltage for Input Current Limit(V_{CS})	Cycle-by-cycle current limit threshold		100		mV
Feedback Voltage			1.31		V
Feedback Input Current	$V_{FB}=1.3V$			100	nA
Switching Frequency	$R_T=400K\Omega$		250		KHz
Maximum Duty Cycle		80	90	95	%
LDR HIGH Voltage	$V_{IN}=5V$, $V_{OUT}=12V$		5		V
HDR HIGH Voltage	$V_{IN}=5V$, $V_{OUT}=12V$		17		V
EN Input Low Voltage				1	V
EN Input High Voltage		2.5		6	V
EN Input Bias Current	$V_{EN}=5V$, $I_{OUT}=0A$		100		μA



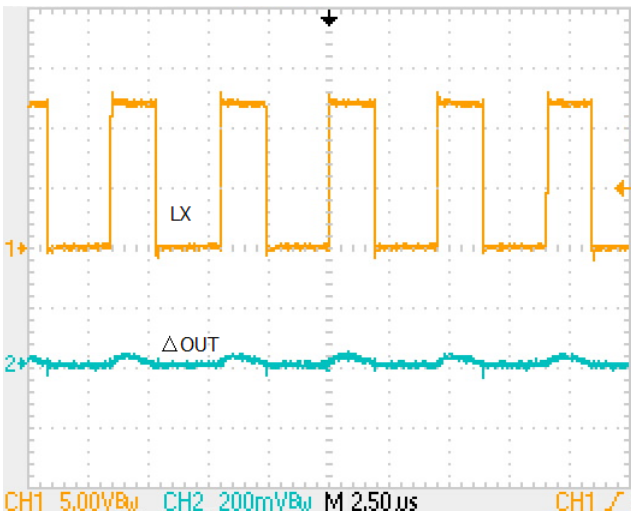
Typical Operating Characteristics



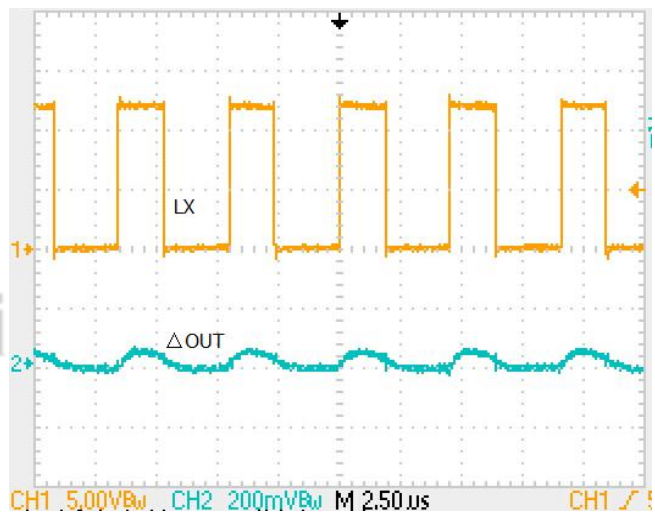
HDR&LDR($R_T=200K\Omega$)



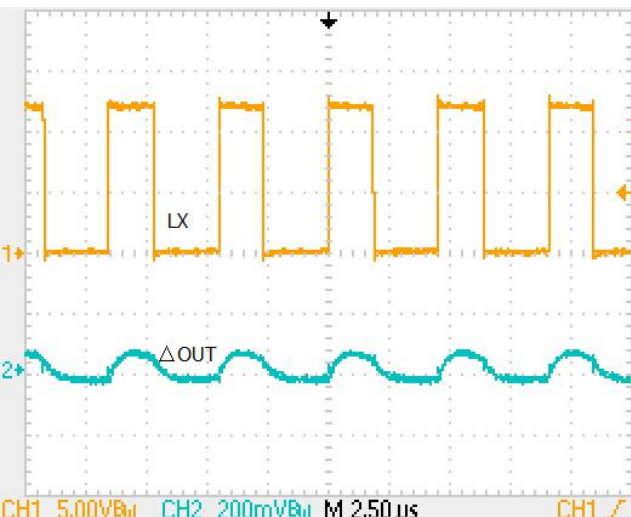
Power On From EN($C_{SS}=0.1\mu F$)



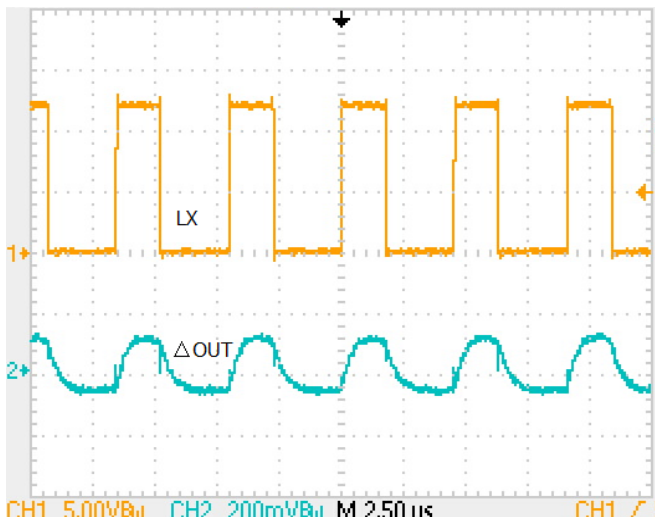
$V_{IN}=3.3V, V_{OUT}=12V, I_{OUT}=100mA$



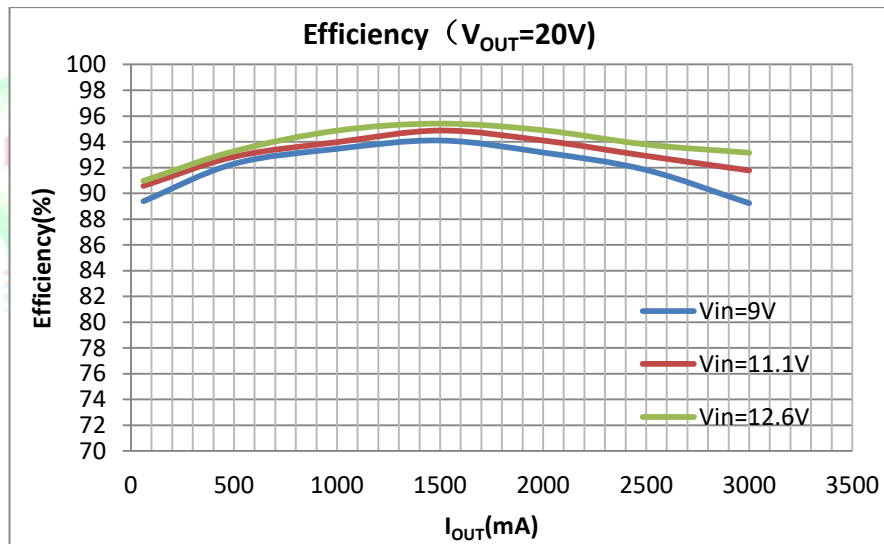
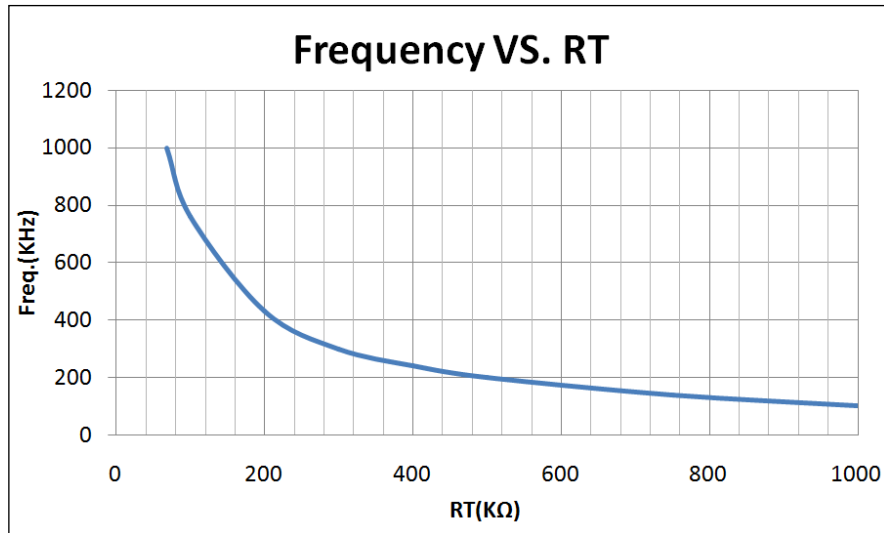
$V_{IN}=3.3V, V_{OUT}=12V, I_{OUT}=500mA$



$V_{IN}=3.3V, V_{OUT}=12V, I_{OUT}=1A$



$V_{IN}=3.3V, V_{OUT}=12V, I_{OUT}=2A$





Application Information

The LP6255 wide input range synchronous boost controller features all of the functions necessary to implement a highly efficient synchronous boost regulator. The regulator control method is based upon peak current mode control. Peak current mode control provides inherent line feed-forward and ease of loop compensation. This highly integrated controller provides strong high-side and low-side N-channel MOSFET drivers. The switching frequency is user programmable up to 1MHz, by a single resistor connected to ground. The LP6255 contains an internal high voltage regulator that provides typical 5V the controller and N-channel MOSFET drivers. The input of the VIN regulator can be connected to a voltage source as high as 30V.

The control mode of high-side synchronous switch can be configured as either forced PWM (FPWM) or diode emulation mode. Fault protection features include cycle-by-cycle current limiting, hiccup mode over load protection, hiccup mode short circuit protection, thermal shutdown. Hiccup mode short circuit protection minimizes power dissipation during prolonged output short condition. The device is available in 20-pin QFN package featuring an exposed pad to aid in thermal dissipation.

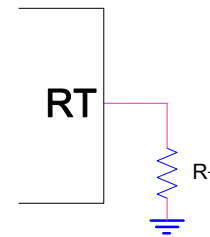
Setting the Output Voltage

Set the output voltage by selecting the resistive voltage divider ratio. The voltage divider drops the output voltage to the 1.31V feedback voltage. Use a 10K resistor for R_2 of the voltage divider. Determine the high-side resistor R_1 by the equation:

$$V_{OUT} = (R_1 / R_2 + 1) \times V_{FB}$$

Oscillator and Clock Synchronization

The LP6255 switching frequency is programmable by a single external resistor connected between the RT pin and the GND pin. The resistor should be located very close to the device and connected directly to the RT and GND pin. To set a desired switching frequency (f_{LX}), the resistor value can be programmed as below.



PWM Comparator

The PWM comparator compares the sum of sensed inductor current and slope compensation ramp to the voltage at the COMP pin through a 1.2V internal COMP to PWM voltage drop and terminates the present cycle when the sum of sensed inductor current and slope compensation ramp is greater than V_{COMP} .

HDR and LDR Drivers

The LP6255 contains two strong N-channel MOSFET gate drivers and a high-side level shifter to drive the external N-channel MOSFET switches. The high-side gate driver works in conjunction with an external bootstrap diode DBST, and bootstrap capacitor CBST. During the on-time of the low-side N-channel MOSFET driver, the LX pin voltage is approximately 0V and the CBST is charged from VIN through the DBST. A 0.1μF or larger ceramic capacitor, connected with short traces between the BST and LX pin, is recommended.



The LDR and HDR outputs are controlled with an adaptive dead-time methodology which ensures that both outputs are never enabled at the same time. When the controller commands LDR to be enabled, the adaptive dead-time logic first disables HDR and waits for HDR-LX voltage to drop. LDR is then enabled after a small delay (HDR Fall to LDR Rise Delay). Similarly, the HDR turn-on is delayed until the LDR voltage has discharged. HDR is then enabled after a small delay (LDR Fall to HDR Rise Delay). This technique ensures adequate dead-time for any size N-channel MOSFET or parallel MOSFET configurations especially when V_{IN} is supplied by a higher external voltage source. Use caution when adding series gate resistors, as this may decrease the effective dead-time.

Care should be exercised in selecting the N-channel MOSFET devices threshold voltage. During startup at low input voltages, the low-side N-channel MOSFET's gate plateau voltage should be sufficiently low to completely enhance the N-channel MOSFET device. If the low-side MOSFET drive voltage is lower than the low-side MOSFET gate plateau voltage during startup, the regulator may not start properly and it may operate at the maximum duty cycle in a high power dissipation state.

Cycle-by-Cycle Current Limit

The LP6255 features a peak cycle-by-cycle current limit function. If the V_{IN} to CS voltage exceeds the 100mV cycle-by-cycle current limit threshold, the current limit comparator immediately terminates the LDR output. For the case where the inductor current overshoots the desired limit, such as inductor saturation, the current limit comparator blocks LDR pulses until the current has decayed below the current limit threshold. Peak inductor current in current limit can be calculated as follows:

$$I_{PEAK} = \frac{100mV}{R_S}$$

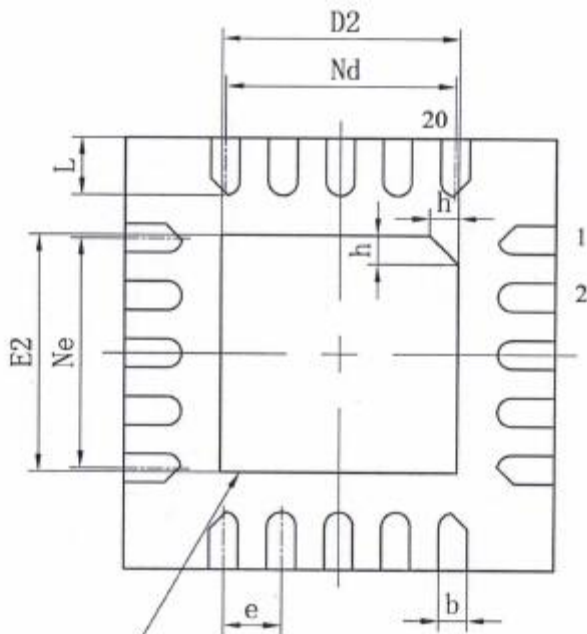
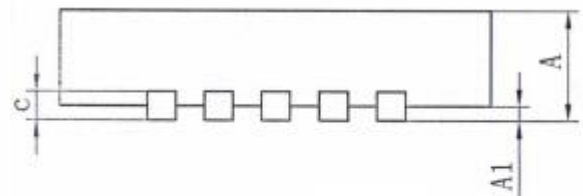
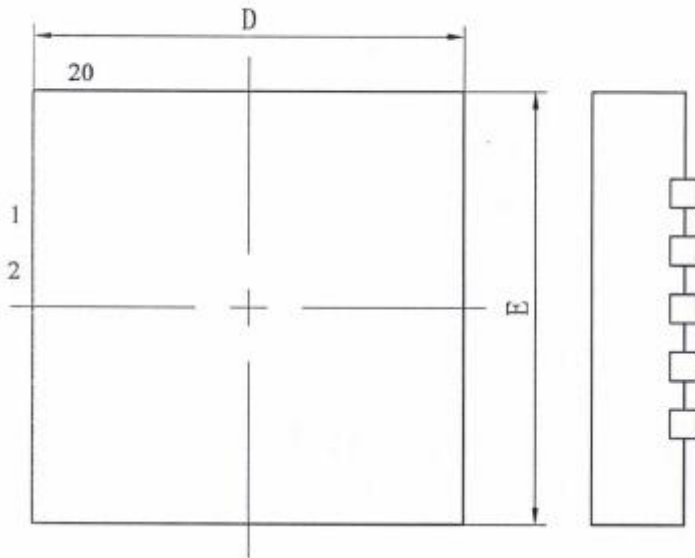
Thermal Protection

Internal thermal shutdown circuitry is provided to protect the controller in the event the maximum junction temperature is exceeded. When activated, typically at 150°C, the controller is forced into a low-power shutdown mode, disabling the output drivers, disconnection switch and the V_{IN} regulator. This feature is designed to prevent overheating and destroying the device.



Packaging Information

QFN-20



EXPOSED THERMAL
PAD ZONE

BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30