Buck 2A, 4-Channel Power Management IC

General Description

The LP6304B is a 2A buck converter of 4-CH power management IC for applications powered by one Li-Ion battery or a DC 5V adapter. It integrates four synchronous buck converters and can provide high efficiency output at light load and heavy load operation. The internal compensation architecture simplifies the application circuit design. Besides, the independent enable control makes the designer have the greatest flexibility to optimize timing for power sequencing purposes.

The LP6304B is available in a 24 pin TQFN 4x4 package.

Order Information

LP6304B □ □ □

- F: Pb/Halogen-Free
- Package Type
  - QV: TQFN 4×4

Applications

- ✧ Smart Phone
- ✧ IP Camera
- ✧ OTT
- ✧ Digital Camera

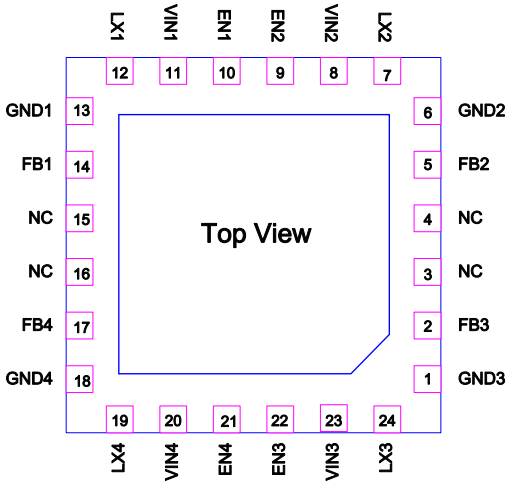
Features

- ◆ 2.2V to 5.5V Input Voltage Range
- ◆ Four Buck Converters
- ◆ Output Voltage Range: 0.6V to Vin
- ◆ Continuous Loading:
- ◆ 2A (Buck1), 2A (Buck2), 2A (Buck3), 2A (Buck4)
- ◆ Fixed 1.5MHz Switching Frequency
- ◆ 100% Duty Cycle Low Dropout Operation
- ◆ <1uA Shutdown Current
- ◆ Independent Enable Control
- ◆ Internal Compensation
- ◆ Cycle-by-Cycle Current Limit
- ◆ Short Circuit Protection
- ◆ Auto Recovery OTP Protection
- ◆ Available in 24-pin 4mm x 4mm QFN Package

Marking Information

Device	Marking	Package	Shipping
LP6304B	LPS LP6304B XXX	TQFN4X4	3K/REEL
Note: X is series number.			

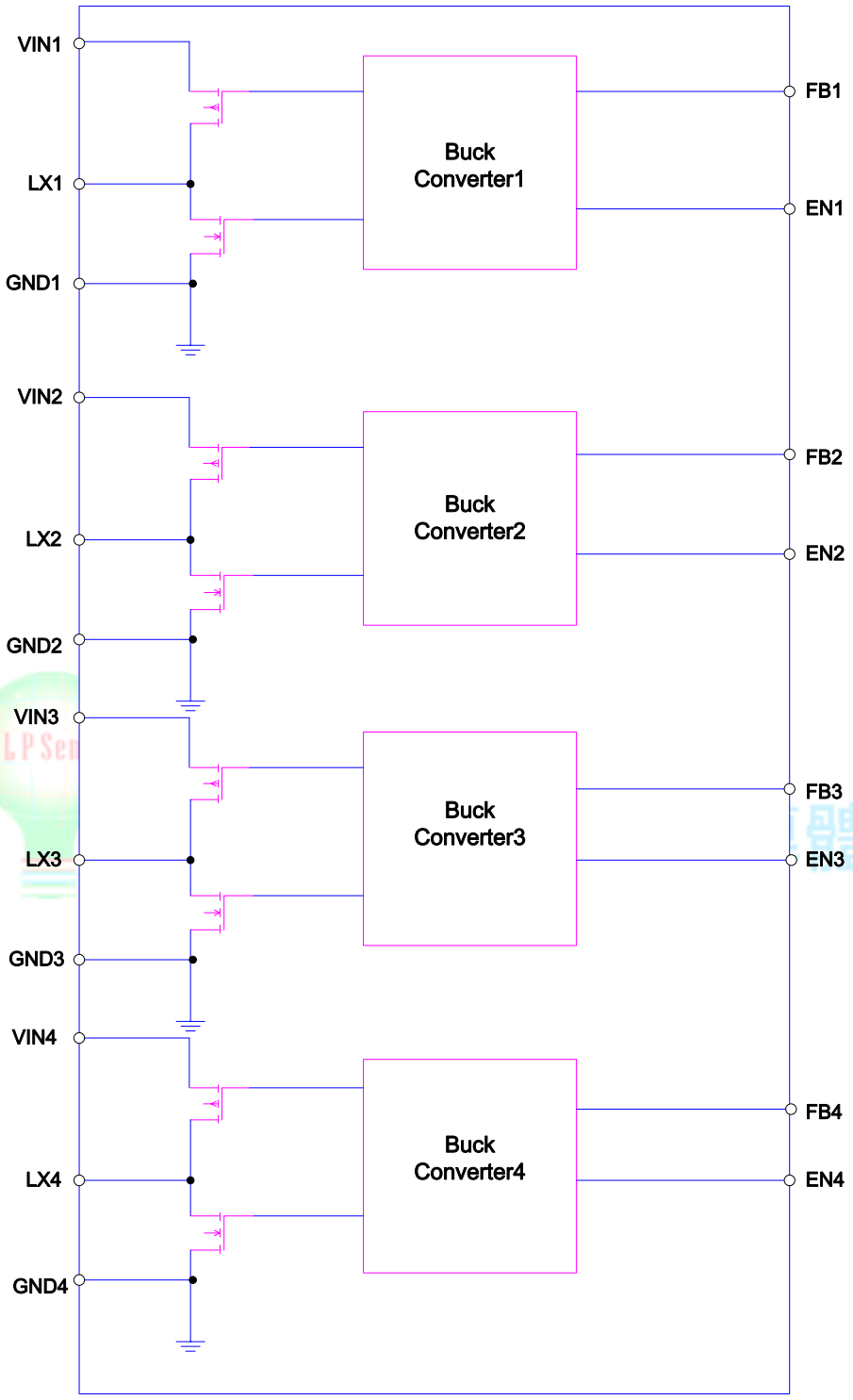
Functional Pin Description

Package Type	Pin Configurations
TQFN 4×4	

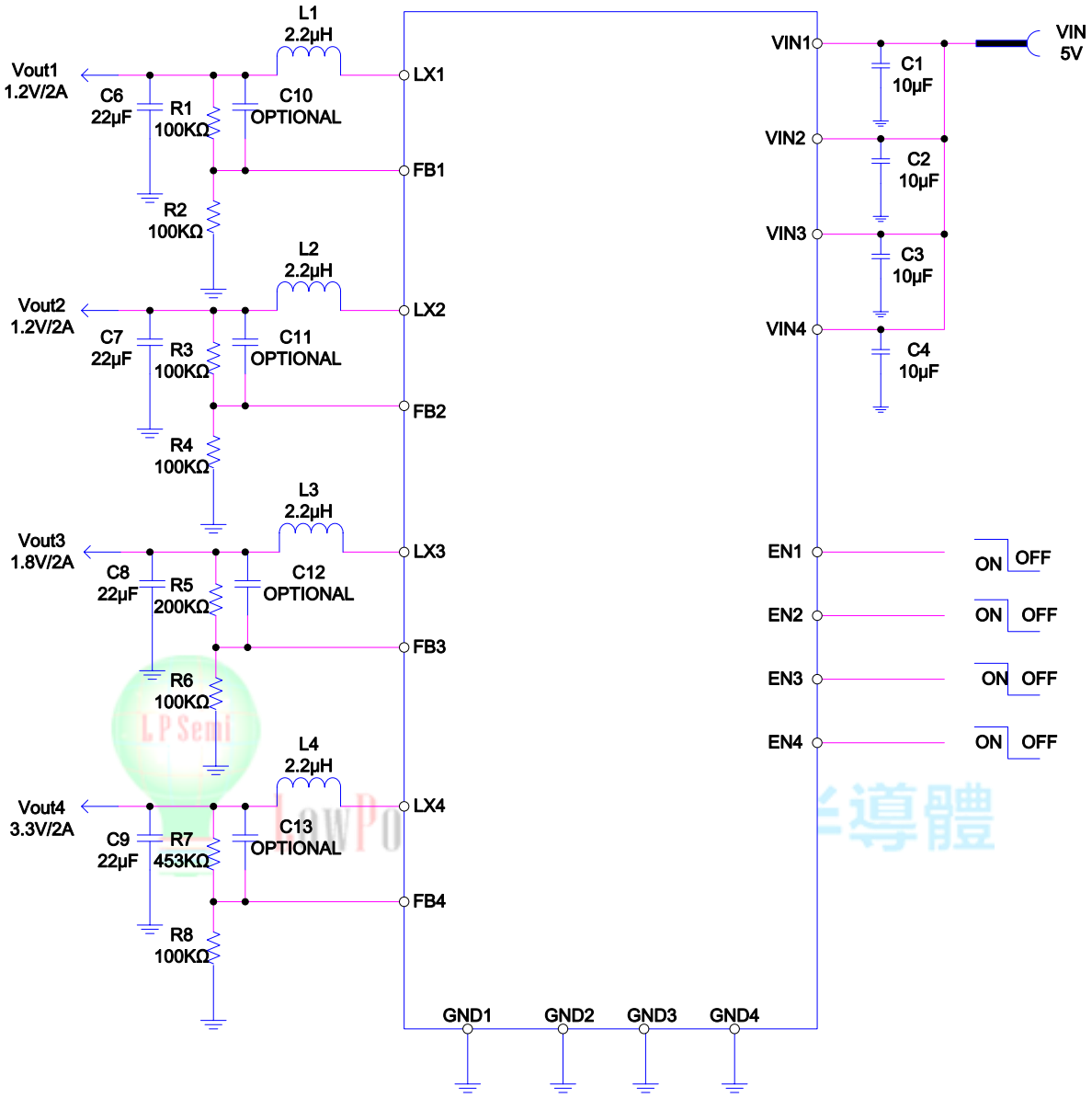
Pin Description

Pin	Name	Description
1	GND3	Power Common Ground.
2	FB3	CH3 Feedback Reference Voltage Pin.
3,4,15,16	NC	No Connecter.
5	FB2	CH2 Feedback Reference Voltage Pin.
6	GND2	Power Common Ground.
7	SW2	CH2 Switch Pin.
8	VIN2	CH2 Supply Input Power.
9	EN2	CH2 Chip Enable.
10	EN1	CH1 Chip Enable.
11	VIN1	CH1 Supply Input Power.
12	SW1	CH1 Switch Pin.
13	GND1	Power Common Ground.
14	FB1	CH1 Feedback Reference Voltage Pin.
17	FB4	CH4 Feedback Reference Voltage Pin.
18	GND4	Power Common Ground.
19	SW4	CH4 Switch Pin.
20	VIN4	CH4 Supply Input Power.
21	EN4	CH4 Chip Enable.
22	EN3	CH3 Chip Enable.
23	VIN3	CH3 Supply Input Power.
24	SW3	CH3 Switch Pin.

Function Diagram



Application Circuit



Absolute Maximum Ratings Note 1

- ✧ Input to GND(VIN) ---------- -0.3V to 6V
- ✧ Other Pin to GND ---------- -0.3V to 6V
- ✧ Maximum Junction Temperature ---------- 125°C
- ✧ Operating Junction Temperature Range (T_J) ---------- -40℃ to 85°C
- ✧ Storage Temperature Range (T_J) ---------- -65℃ to 150℃
- ✧ Maximum Soldering Temperature (at leads, 10 sec) ---------- 260°C

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Maximum Power Dissipation (P_D,T_A=25℃) ---------- 2.5W
- ✧ Thermal Resistance (θ_{JA}) ---------- 50℃/W

ESD Susceptibility

- ✧ HBM(Human Body Mode) ---------- 2KV
- ✧ MM(Machine Mode) ---------- 200V

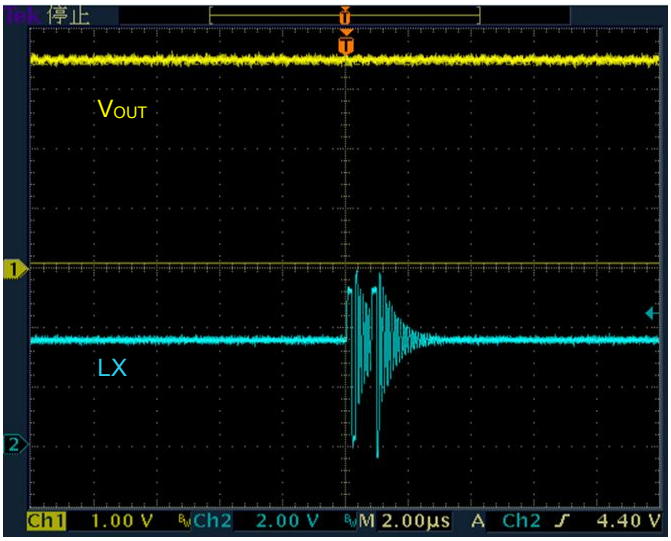
Electrical Characteristics

(V_{INX}=5V, T_A=25°C, unless otherwise noted)

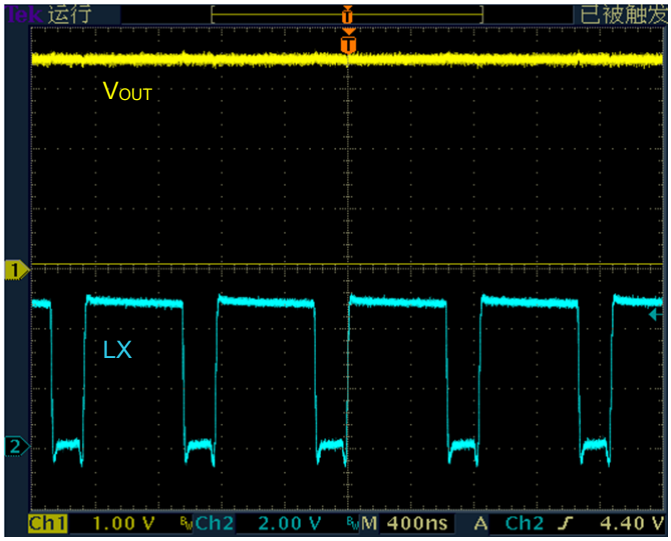
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Supply Voltage						
Input Voltage	V_{INX}		2.2		5.5	V
Control Circuit Input Voltage	V_{CC}		2.2		5.5	V
Buck Converter						
Shutdown Supply Current	I_{SD}	V_{EN} = 0V		0.1	1	μA
Quiescent Current	I_Q	V_{EN} = 2V, No Load			280	μA
UVLO Threshold	V_{UVLO}	V_{IN} Rising		2		V
UVLO Hysteresis	V_{UV-HYS}			0.1		V
Output Load Current	I_{LOAD}		2			A
Reference Voltage	V_{REF}		0.588	0.6	0.612	V
Switching Frequency	F_{SW}	I_{LOAD} = 100mA	1	1.5	2	MHz
PMOS Current Limit	I_{LIM-P}		3			A
PMOS On-Resistance Note	$R_{DS(ON)-P}$	I_{LOAD} = 100mA		100		mΩ
NMOS On-Resistance Note	$R_{DS(ON)-N}$	I_{LOAD} = 100mA		90		mΩ
Enable Pin Input Low Voltage	V_{EN-L}				0.4	V
Enable Pin Input High Voltage	V_{EN-H}		1.5			V
Enable Input Current	I_{EN}				2	uA
Output Voltage Soft Start	T_{SS}	(0%→90%)V_{OUT}		450		us
Over-Temperature Shutdown Threshold	T_{SD}			150		℃
Maximum Duty Cycle	D_{MAX}		100			%

Note: MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

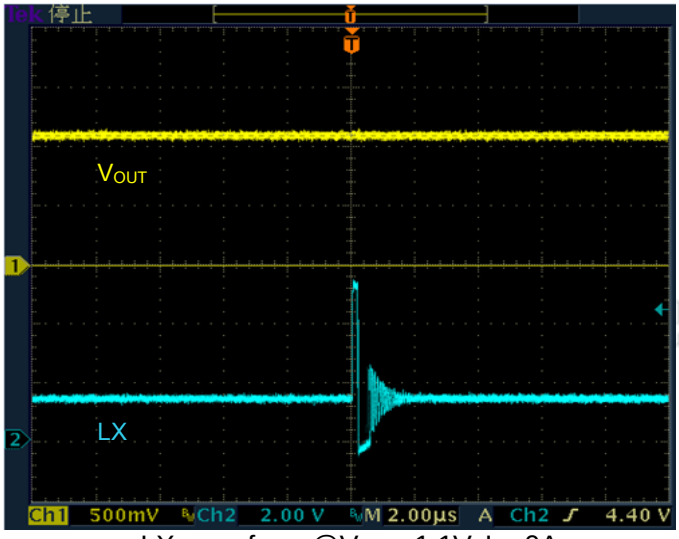
Typical Operating Characteristics



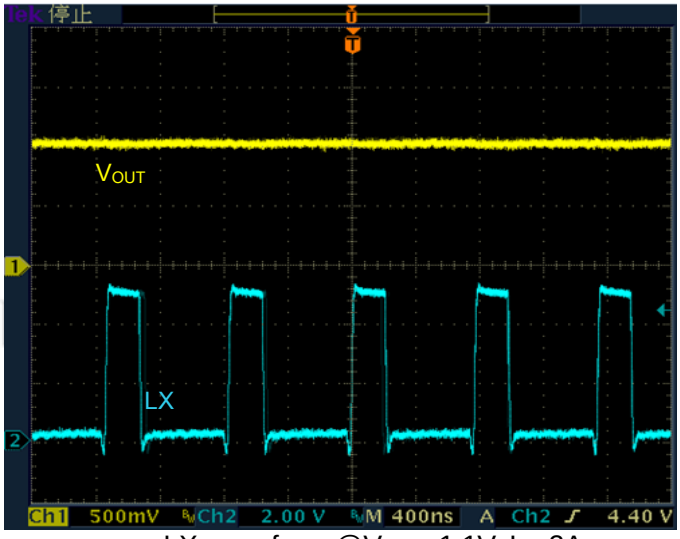
LX waveform @V_{OUT}=3.3V, Io=0A



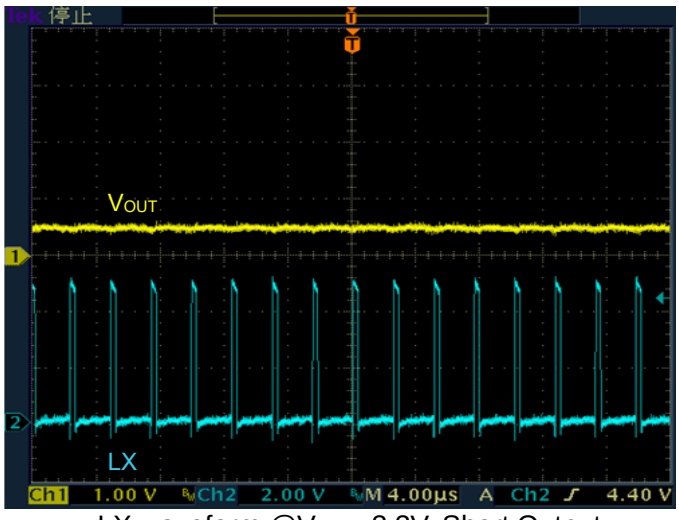
LX waveform @V_{OUT}=3.3V, Io=2A



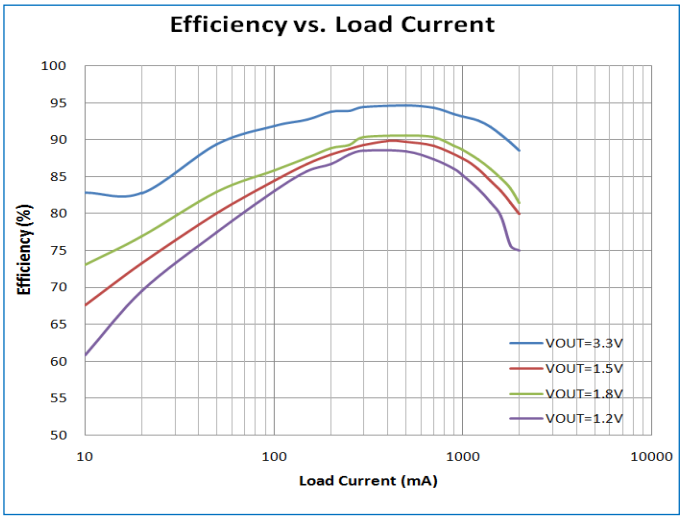
LX waveform @V_{OUT}=1.1V, Io=0A

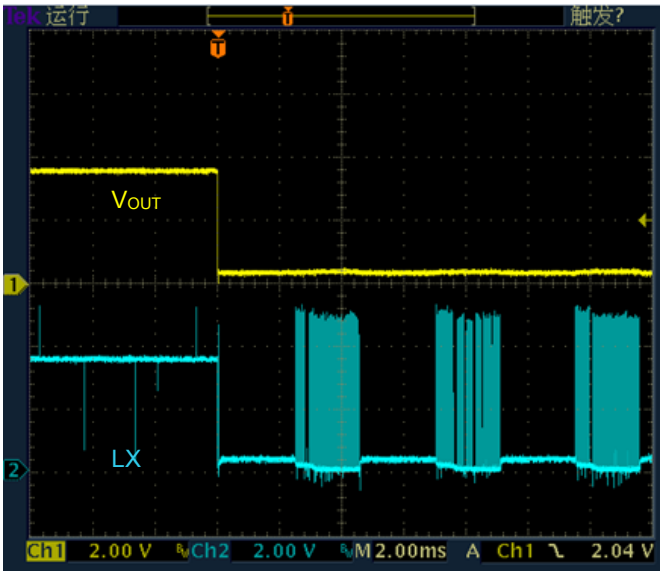


LX waveform @V_{OUT}=1.1V, Io=2A

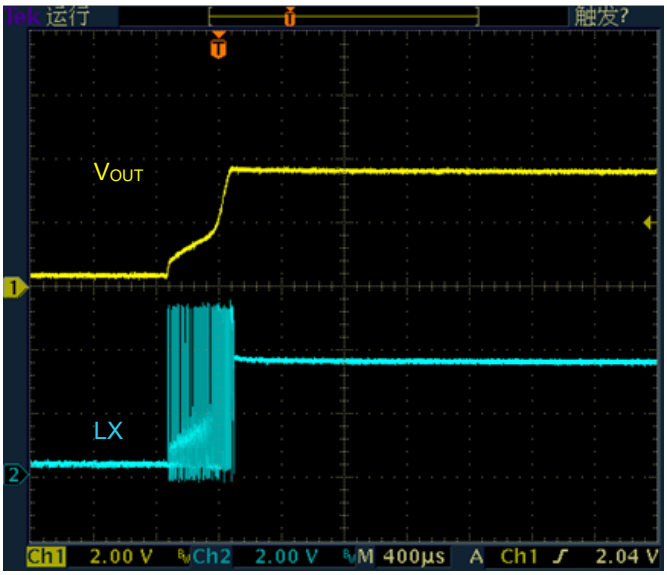


LX waveform @V_{OUT}=3.3V, Short Output

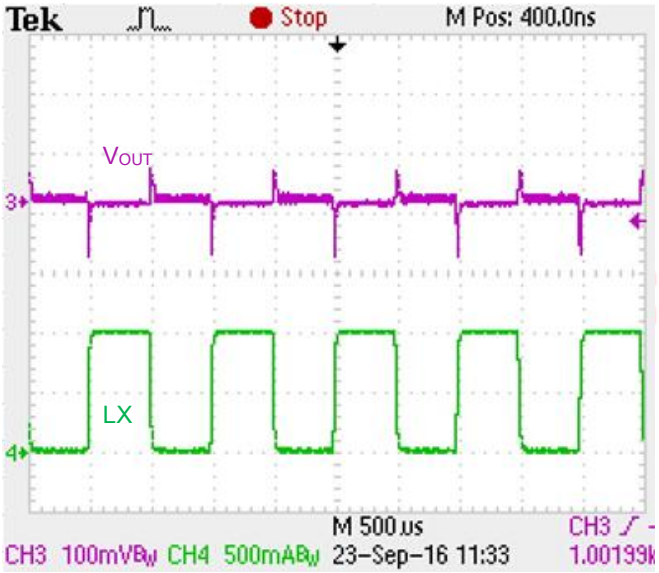




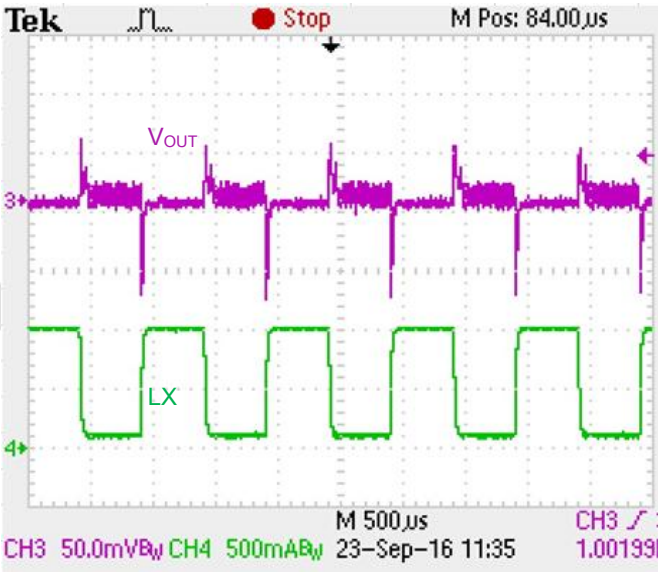
LX waveform @V_{OUT}=3.3V, No Load to Short Output



LX waveform @V_{OUT}=3.3V, Short Output to No Load



Output waveform @V_{OUT}=3.3V, Io=10mA to 1A



Output waveform @V_{OUT}=3.3V, Io=100mA to 1A

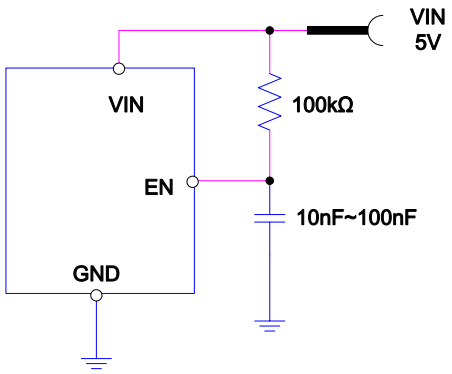
Functional Description

PFM/PWM Operation

Each of the buck regulators can be operated at PFM/PWM mode. If the output current is less than 170mA (V_{OUT}=1.2V), the regulators automatically enters the PFM mode. The output voltages and output ripples at PFM mode are higher than the output voltages and output ripples at PWM mode. But at very light load, the PFM mode operation provides higher efficiency than PWM mode operation.

Enable Control

The LP6304B is a high efficiency Power Management IC which is designed for IPC and OTT applications. It incorporates four 2A synchronous buck regulators and can be controlled by individual EN pins. The start-up time for each channel can be programmed by using the circuit shown as below:



Over Current Protection

The LP6304B internal four regulators have their own cycle-by-cycle current limit circuits. When the inductor peak current exceeds the current limit threshold, the output voltage starts to drop until FB pin voltage is below the threshold.

Thermal Shutdown

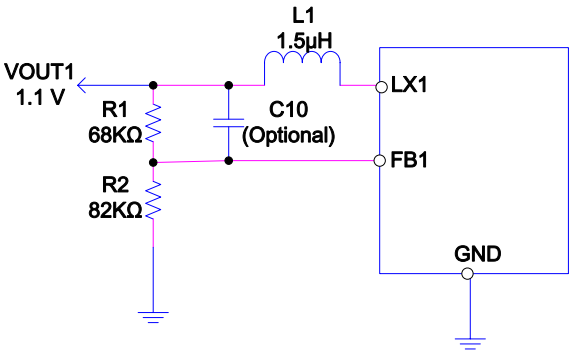
The LP6304B will automatically disabled if the die temperature is higher than the thermal shutdown threshold point. To avoid unstable operation, the hysteresis of thermal shutdown is about 20°C.

Application Information

Output Voltage Setting

Each of the regulators output voltage can be set via a resistor divider (ex. R1, R2). The output voltage is calculated by following equation:

$$V_{OUT1} = 0.6 \times \frac{R1}{R2} + 0.6\ V$$



The following table lists common output voltage and the corresponding R1, R2 resistance value for reference.

V_{OUT}	R1	R2	Tolerance
3.3V	510KΩ	110KΩ	1%
1.8V	200KΩ	100KΩ	1%
1.5V	150KΩ	100KΩ	1%
1.1V	68KΩ	82KΩ	1%

Output Inductor Selection

The output inductor selection mainly depends on the amount of ripple current through the inductor ΔI_L. Large ΔI_L will cause larger output voltage ripple and loss, but the user can use a smaller inductor to save cost and space. On the contrary, the larger inductance can get smaller ΔI_L and thus the smaller output voltage ripple and loss. But it will increase the space and the cost. The inductor value can be calculated as:

$$L = \frac{V_{PWR} - V_{OUT}}{\Delta I_L \times F_{SW}} \times \frac{V_{OUT}}{V_{PWR}}$$

For most applications, 1.0uH to 2.2uH inductors are suitable for LP6304B

Power Dissipation

The total output power dissipation of LP6304B should not to exceed the maximum 10W range. The total output power dissipation can be calculated as:

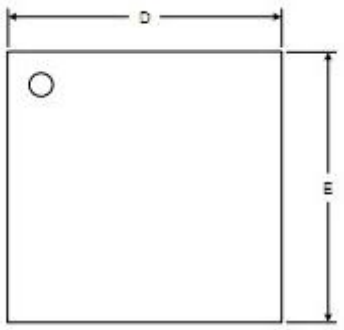
$$P_{D(total)} = V_{OUT1} \times I_{OUT1} + V_{OUT2} \times I_{OUT2} + V_{OUT3} \times I_{OUT3} + V_{OUT4} \times I_{OUT4}$$

PCB Layout

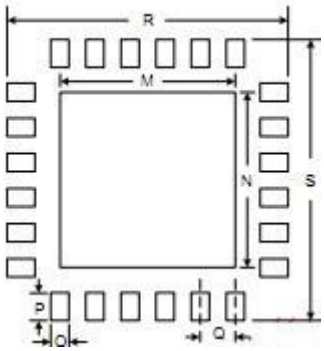
Layout is very critical for PMIC designs. For LP6304B PCB layout considerations, please refer to the following suggestions to get best performance.

- It is suggested to use 4-layer PCB layout and place LX plane and output plane on the top layer, place VIN plane in the inner layer.
- The top layer SMD input and output capacitors ground plane should be connected to the internal ground layer and bottom ground plane individually by using vias.
- The GND should be connected to inner ground layer directly by using via.
- High current path traces need to be widened.
- Place the input capacitors as close as possible to the VINx pin to reduce noise interference.
- Keep the feedback path (from V_{OUTX} to FBx) away from the noise node (ex. LXx). LXx is a high current noise node. Complete the layout by using short and wide traces.
- The top layer exposed pad ground plane should be connected to the internal ground layer and bottom ground plane by using a number of vias to improve thermal performance.
- Place the input capacitors as close as possible to the VINx pin to reduce noise interference.

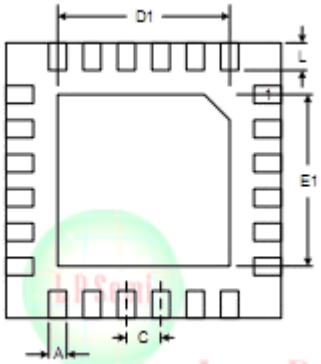
Packaging Information



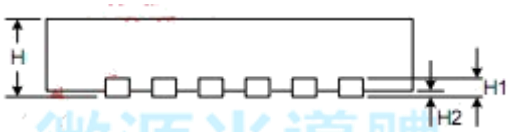
TOP VIEW



Recommended Layout Pattern



Bottom View



Side View

Symbol	Dimension		Dimension	
	Min.	Max.	Symbol	Typ.
A	0.18	0.30	M	2.60
C	0.45	0.55	N	2.60
D	3.95	4.05	O	0.30
E	3.95	4.05	P	0.80
D1	2.30	2.70	Q	0.50
E1	2.30	2.70	R	4.70
L	035	0.45	S	4.70
H	0.80	1.00		
H1	0.17	0.25		
H2	0.00	0.05		