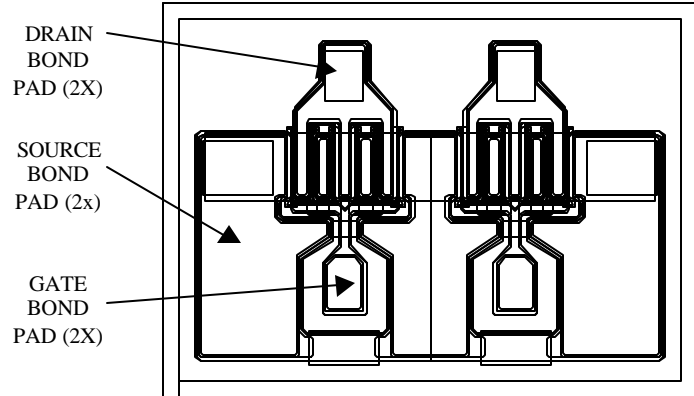


FEATURES

- ◆ 27 dBm Output Power at 1-dB Compression at 18 GHz
- ◆ 9.5 dB Power Gain at 18 GHz
- ◆ 55% Power-Added Efficiency



DIE SIZE: 14.6X19.7 mils (370x500 μm)
 DIE THICKNESS: 3.0 mils (75 μm)
 BONDING PADS: 1.9X2.4 mils (50x60 μm)

DESCRIPTION AND APPLICATIONS

The LP6872 is an Aluminum Gallium Arsenide / Indium Gallium Arsenide (AlGaAs/InGaAs) Pseudomorphic High Electron Mobility Transistor (PHEMT), utilizing an Electron-Beam direct-write 0.25 μm by 720 μm Schottky barrier gate. The recessed “mushroom” gate structure minimizes parasitic gate-source and gate resistances. The epitaxial structure and processing have been optimized for reliable high-power applications. The LP6872 also features Si_3N_4 passivation.

Typical applications include commercial wireless infrastructure amplifiers, such as SATCOM uplink transmitters, PCS/Cellular low-voltage high-efficiency output amplifiers, and medium-haul digital radio transmitters.

ELECTRICAL SPECIFICATIONS @ $T_{\text{Ambient}} = 25^\circ\text{C}$

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Saturated Drain-Source Current	I_{DSS}	$V_{\text{DS}} = 2 \text{ V}; V_{\text{GS}} = 0 \text{ V}$	180	245	260	mA
Power at 1-dB Compression	P-1dB	$V_{\text{DS}} = 8 \text{ V}; I_{\text{DS}} = 50\% I_{\text{DSS}}$	25	27		dBm
Power Gain at 1-dB Compression	G-1dB	$V_{\text{DS}} = 8 \text{ V}; I_{\text{DS}} = 50\% I_{\text{DSS}}$	8	9.5		dB
Power-Added Efficiency	PAE	$V_{\text{DS}} = 8 \text{ V}; I_{\text{DS}} = 50\% I_{\text{DSS}}$		55		%
Maximum Drain-Source Current	I_{MAX}	$V_{\text{DS}} = 2 \text{ V}; V_{\text{GS}} = 1 \text{ V}$		385		mA
Transconductance	G_{M}	$V_{\text{DS}} = 2 \text{ V}; V_{\text{GS}} = 0 \text{ V}$	175	220		mS
Gate-Source Leakage Current	I_{GSO}	$V_{\text{GS}} = -5 \text{ V}$		5	40	μA
Pinch-Off Voltage	V_{P}	$V_{\text{DS}} = 2 \text{ V}; I_{\text{DS}} = 4 \text{ mA}$	-0.25	-1.2	-2.0	V
Gate-Source Breakdown Voltage Magnitude	$ V_{\text{BDGS}} $	$I_{\text{GS}} = 4 \text{ mA}$	-10	-13		V
Gate-Drain Breakdown Voltage Magnitude	$ V_{\text{BDGD}} $	$I_{\text{GD}} = 4 \text{ mA}$	-10	-14		V
Thermal Resistivity	Θ_{JC}			70		$^\circ\text{C/W}$

frequency=18 GHz

- ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	V_{DS}	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		12	V
Gate-Source Voltage	V_{GS}	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		-4	V
Drain-Source Current	I_{DS}	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		$2xI_{DSS}$	mA
Gate Current	I_G	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		35	mA
RF Input Power	P_{IN}	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		300	mW
Channel Operating Temperature	T_{CH}	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		175	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	—	-65	175	$^{\circ}\text{C}$
Total Power Dissipation	P_{TOT}	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		1.76	W

Notes:

- Operating conditions that exceed the Absolute Maximum Ratings could result in permanent damage to the device.
- Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$, where
 P_{DC} : DC Bias Power
 P_{IN} : RF Input Power
 P_{OUT} : RF Output Power
- Absolute Maximum Power Dissipation to be de-rated as follows above 25 $^{\circ}\text{C}$:
 $P_{TOT} = 1.76\text{W} - (0.0117\text{W}/^{\circ}\text{C}) \times T_{HS}$
 where T_{HS} = heatsink or ambient temperature.

- HANDLING PRECAUTIONS**

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A (0-500 V). Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

- ASSEMBLY INSTRUCTIONS**

The recommended die attach is gold/tin eutectic solder under a nitrogen atmosphere. Stage temperature should be 280-290 $^{\circ}\text{C}$; maximum time at temperature is one minute. The recommended wire bond method is thermo-compression wedge bonding with 0.7 or 1.0 mil (0.018 or 0.025 mm) gold wire. Stage temperature should be 250-260 $^{\circ}\text{C}$.

- APPLICATIONS NOTES & DESIGN DATA**

Applications Notes are available from your local Filtronic Sales Representative or directly from the factory. Complete design data, including S-parameters, noise data, and large-signal models are available on the Filtronic web site.

All information and specifications are subject to change without notice.