Advanced 1A Lithium-Ion Linear Battery Charger

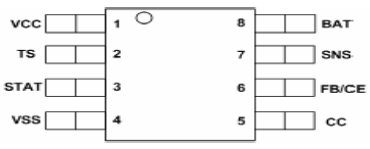
General Description

The LP8501 is a single Lithium-Ion (Li-Ion) linear charge management controller for use in cost sensitive and portable applications. It combines high accuracy constant-current and constant-voltage regulation, cell preconditioning, tempera ture monitoring, automatic charge termination, charge-status indication, in a space-saving MSOP-8 package.

The LP8501 applies a constant current up to 1A to the battery and the charge current can be programmed externally with a sense-resistor.

The LP8501 automatically terminates the charge cycle when the charge current drops to the charge termination threshold (ITERM) after the charge-regulation voltage is reached. When the input supply is removed, the LP8501 automatically enters a low-power sleep mode, dropping the battery drain current to less than 1μA. A battery charge state output pin is provided to indicate Programmable Charge Current up to 1A 4.5V-7V Input Voltage Range Ideal for Single Cell (4.1V or 4.2V) Li-Ion or Li-Pol Batteries. Preset Charge Voltage with ±1% Accuracy Constant-Current/ Constant Voltage Operation Preconditioning of Low Voltage Cells Optional Cell-Temperature Monitoring Before and During Charge Charge Status Indication Automatic Battery Recharge Charge Termination by Minimum Current Automatic Low-Power Sleep Mode When Input Power is Removed Available in MSOP-8 Package RoHS Compliant and 100% Lead (Pb)-Free battery charge status through a display LED.

Pin Configurations



Features

- Ideal for Single Cell (4.1V or 4.2V) Li-Ion or Li-Pol Batteries
- 4.5V-7V Input Voltage Range
- Programmable Charge Current up to 1A
- Precharge Constant-Current/Constant Voltage mode
- Automatic Low-Power Sleep Mode
- Automatic Battery Recharge Charge Termination by Minimum Current
- Optional Cell-Temperature Monitoring Before and During Charge
- Charge status through a display LED
- Automatic Low-Power Sleep Mode When Input Power is Removed

Applications

- Portable Media Players/MP3 players
- Cellular and Smart mobile phone
- PDA
- DSC

Ordering Information

LP8501 - □ □ □ □ □

F:PB-Free

Package
MS:MSOP-8

Output Type
41: 4.1V
42: 4.2V

Marking Information

RoHS compliant and compatible with the current require ments of IPC/JEDEC J-STD-020.

Suitable for use in SnPb or Pb-free soldering processes.

Typical Application Circuit

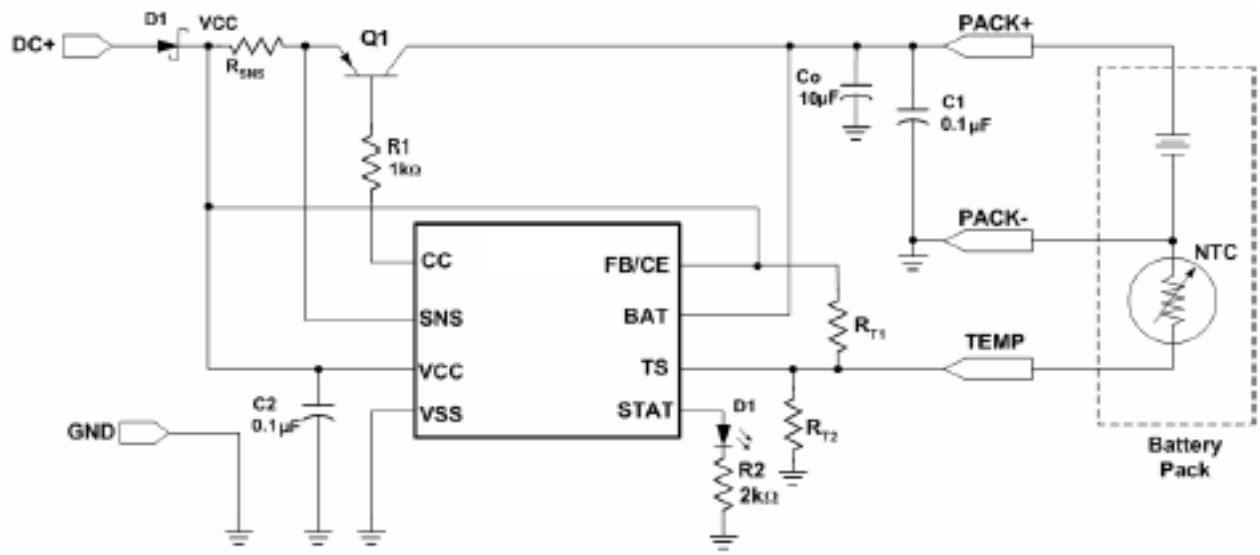


Figure1. Linear Charger Using PNP Transistor

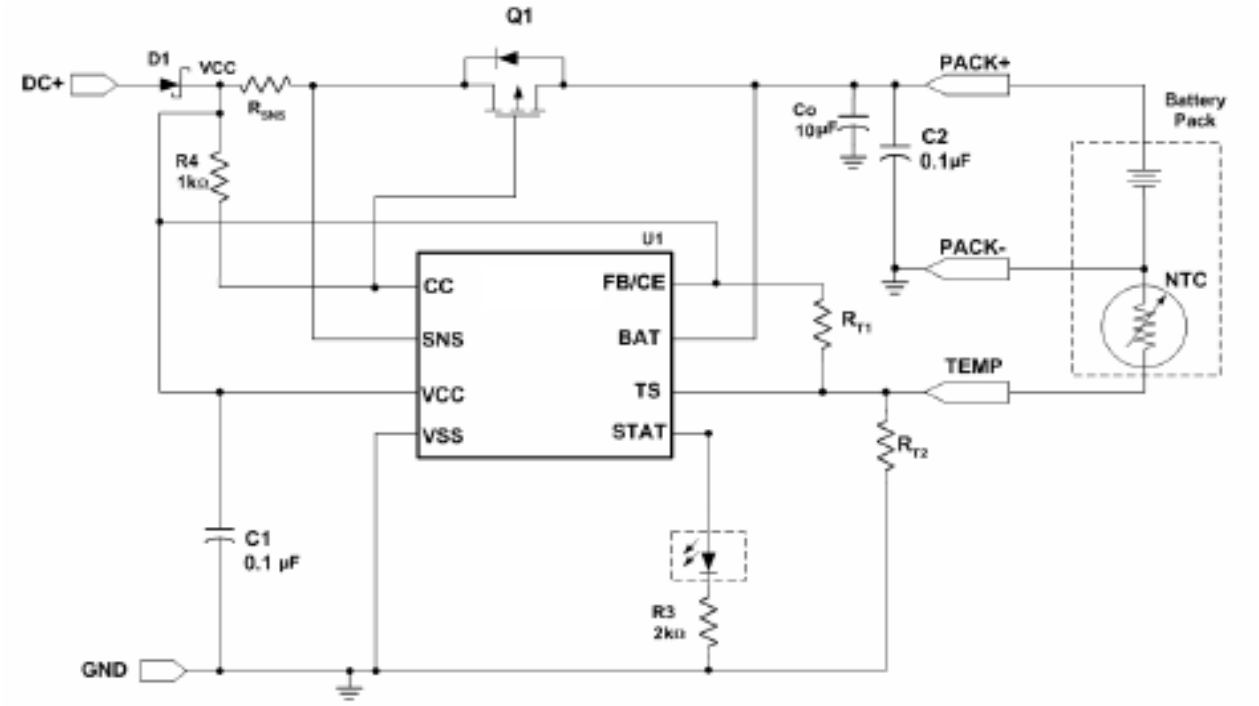


Figure2. Linear Charger Using P-Channel MOSFET

Functional Pin Description

PIN	MSOP-8	I/O	DESCRIPTION
VCC	1	I	Supply Voltage Input
TS	2	I	Temperature Sense Input
STAT	3	O	Charge Status Output
VSS	4		Ground
CC	5	O	Charge Control Output
FB/CE	6	I	External Feedback input or Charge Enable Function. Input from controller or finely adjust the battery regulated voltage with external voltage divider
SNS	7	I	Current Sense Input
BAT	8	I	Battery Voltage Input

Function Block Diagram

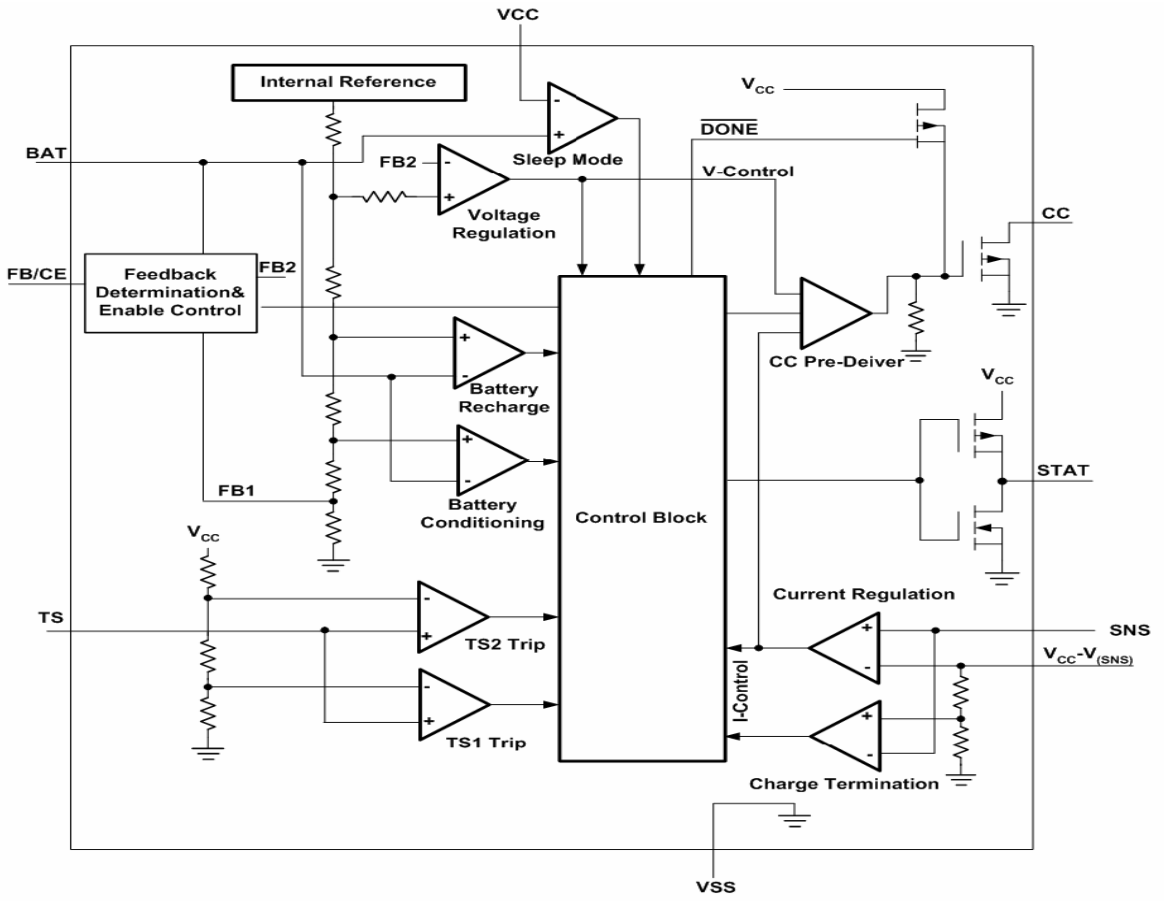
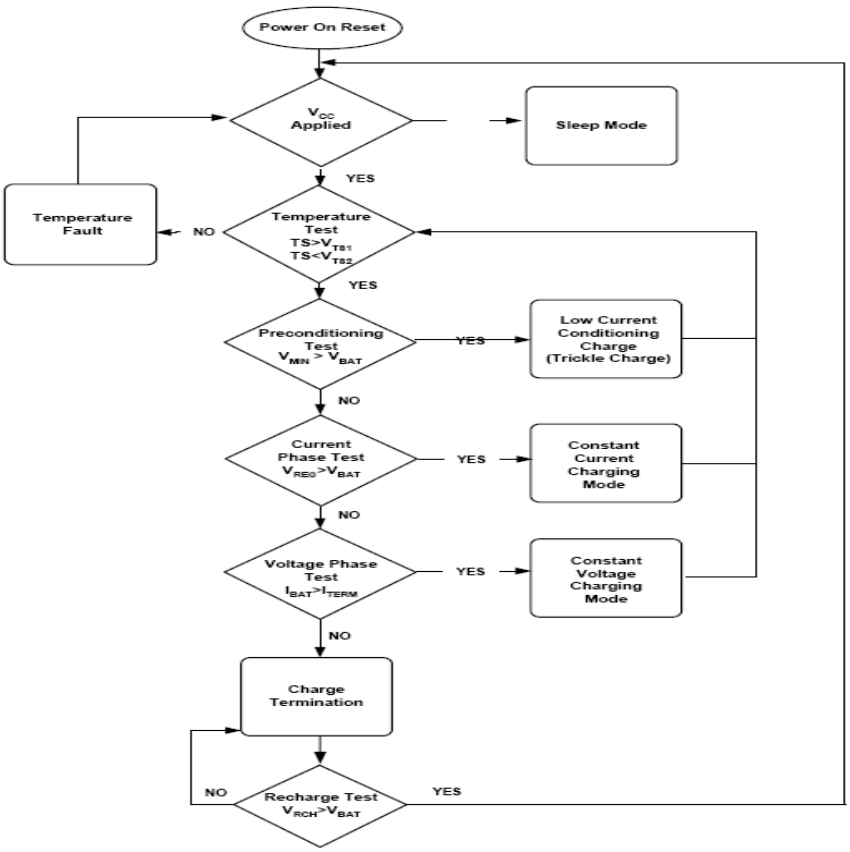


Figure3. Block Diagram

Operation Flow Chart



Absolute Maximum Ratings

- Supply voltage, (Vcc with respect to GND) ---------- -0.3 to +7V
- Input voltage, SNS, BAT, TS, PI (all with respect to GND)---------- -0.3V to V_{CC} +0.3V
- Sink current (STAT pin) not to exceed P_D ---------- 20mA
- Source current (STAT pin) not to exceed P_D ---------- 10mA
- Output current (CC pin) not to exceed P_D ---------- 40mA
- Maximum Junction Temperature, T_J ---------- 150°C
- Storage temperature range, Tstg ---------- -65°C to 150°C
- Lead temperature (soldering, 10s) ---------- 300°C
- Package Thermal Resistance, θ_{JA}- MSOP8 ---------- 80°C/W

Electrical Characteristics

Symbol	Parameter	Conditions	LP8501			Unit
			Min.	Typ.	Max.	
$I_{(VCC)}$	VCC current	VCC=5V VCC(min), Excluding external loads		0.6	1	mA
$I_{(VCCS)}$	VCC Sleep current	V(BAT) ≥ V(min), V(BAT)-VCC ≥ 0.8V		2	6	μA
$I_{IB(BAT)}$	Input bias current on BAT pin	V(BAT)=V(REG)			1	μA
$I_{IB(SNS)}$	Input bias current on SNS pin	V(SNS)=5V			1	μA
$I_{IB(TS)}$	Input bias current on TS pin	V(TS)=5V			1	μA
$I_{IB(PI)}$	Input bias current on PI pin	V(PI)=5V			1	μA
Battery Voltage Regulation						
$V_{O(REG)}$	Output voltage	LP8501-41	4.059	4.10	4.141	V
		LP8501-42	4.158	4.20	4.242	
$V_{(SNS)}$	Current regulation threshold	Voltage at pin SNS, relative to VCC	198	220	242	mV
Charge Termination Detection						
$I_{(TERM)}$	Charge termination current detect threshold	Voltage at pin SNS, relative to VCC 0°C ≤ TA ≤ 50°C	-25	-15	-5	mV
Temperature Comparator						
$V_{(TS1)}$	Lower temperature threshold	TS pin voltage	29	30	31	%VCC
$V_{(TS2)}$	Upper temperature threshold		58	60	62	
Precharge Comparator						
$V_{(min)}$	Precharge threshold	LP8501-4.1MSF	2.94	3	3.06	
		LP8501-4.2MSF	3.04	3.1	3.16	V
Precharge Current Regulation						
$I_{(PRECHG)}$	Precharge current regulation	Voltage at pin SNS, relative to VCC 0°C ≤ TA ≤ 50°C		15		mV
		Voltage at pin SNS, relative to VCC 0°C ≤ TA ≤ 50°C , VCC=5V	5	15	25	mV

VRCH comparator(Battery Recharge Threshold)						
VRCH	Recharge threshold	LP8501-4.1 and LP8501-4.2	VO(REG)-98mV	VO(REG)-100mV	VO(REG)-102mV	V
Stat Pin						
VOH(STAT)	Output(high)voltage	IOH=5mA			0.5	V
VOL(STAT)	Output(low)voltage	IOL=10mA	VCC-0.5			
CC Pin						
IO(CC)	Sink current	Not to exceed power rating specification(PD)	5		40	mA
VOL(CC)	Output low voltage	IO(CC)=5mA(sink)			1.5	V

Applications Information

When power is applied, the LP8501 starts a charge-cycle if a battery is already present or when a battery is inserted. Charge qualification is based on battery temperature and voltage.

The LP8501 suspends charge if the battery temperature is outside the V(TS1) to V(TS2) range and suspends charge until the battery temperature is within the allowed range. The LP8501 also checks the battery voltage. If the battery voltage is below the precharge threshold V(min), the LP8501 uses precharge to condition the battery. The conditioning charge rate I(PRECHG) is set at approximately 10% of the regulation current. The conditioning current also minimizes heat dissipation in the external pass-element during the initial stage of charge. See Figure5 for a typical charge-profile.

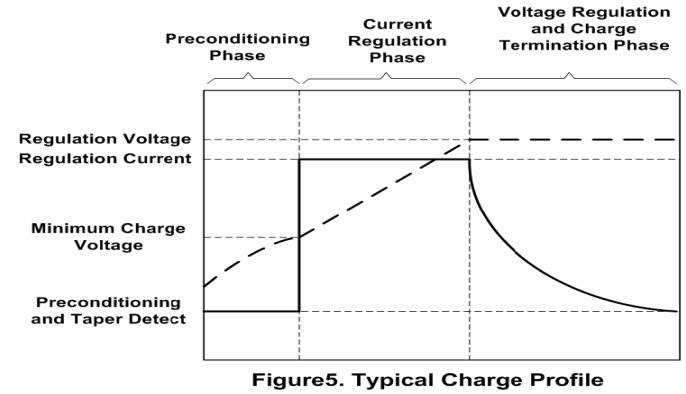


Figure5. Typical Charge Profile

Current Regulation Phase

The LP8501 regulates current while the battery-pack voltage is less than the regulation voltage, VO(REG). The LP8501 monitors charge current at the SNS input by the voltage drop across a sense-resistor, RSNS, in series with the battery pack. In current sensing configuration (Figure6), RSNS is between the VCC and SNS pins, charge-current feedback, applied through pin SNS, maintains a voltage of V(SNS) across the current sense resistor. The following formula calculates the value of the sense resistor:

$$R_{SNS} = \frac{V_{(SNS)}}{I_{O(REG)}}$$

Where IO(REG) is the desired charging current.
Example: For 0.55A, RSNS: 0.22V/0.55A: 0.4Ω
For 1.0A, RSNS: 0.22V/1.0A: 0.22Ω

For PTC Thermistors

$$R_{T1} = \frac{5 \times R_{TH} \times R_{TC}}{3 \times (R_{TH} - R_{TC})} \quad \text{----------} (5)$$

$$R_{T2} = \frac{5 \times R_{TH} \times R_{TC}}{[(2 \times (R_{TH}) - (7 \times R_{TC})]} \quad \text{----------} (6)$$

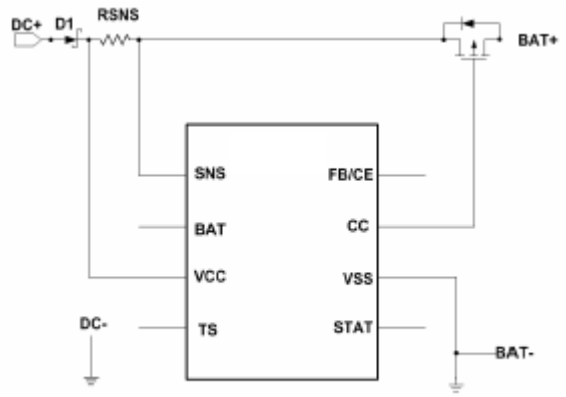


Figure6. Current Sensing Circuit

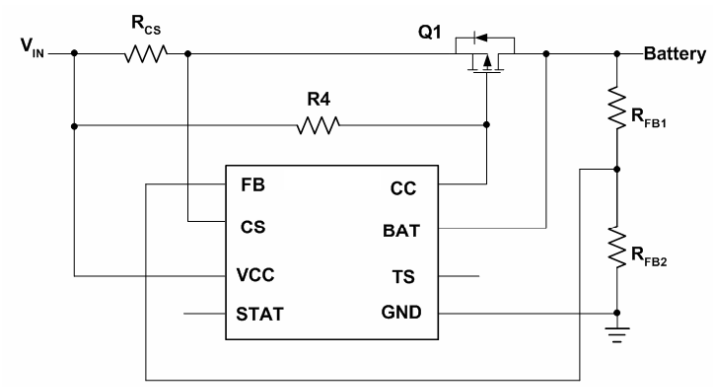


Figure8. For FB pin Function

Voltage Regulation Phase

The voltage regulation feedback is through the BAT pin. This input is tied directly to the positive side of the battery pack. The LP8501 monitors the battery-pack voltage between the BAT and VSS pins. The LP8501 is offered in two fixed-voltage versions:4.1V, 4.2V.

FB/CE Pin Function

This pin has two functions, one is to enable/disable the charge function, and the other is to finely adjust battery regulation voltage. Connect this pin to VDD to enable LP8501, and connect to ground to disable it (Figure7). If this pin is connected to a voltage divider as shown in Figure8, it can be a 2.15V reference voltage to adjust the output regulation voltage as desired.

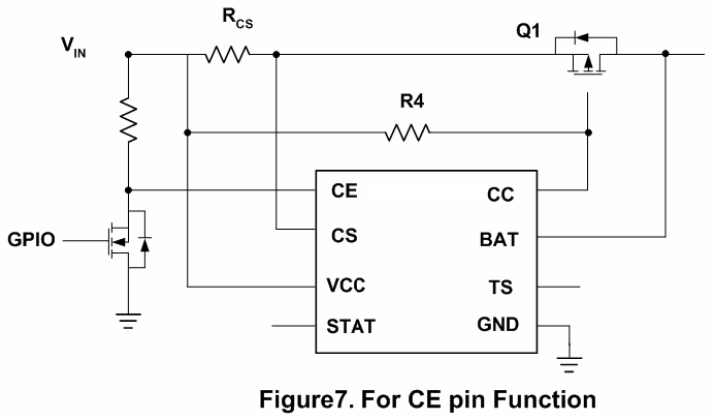


Figure7. For CE pin Function

$$V_{O(REG)} = 2.15 \times (1 + \frac{R_{FB1}}{R_{FB2}})V$$

Charge Termination and Recharge

The LP8501 monitors the charging current during the voltage-regulation phase. The LP8501 declares a done condition and terminates charge when the current drops to the charge termination threshold, I(TERM). A new charge cycle begins when the battery voltage falls below the (RCH) threshold.

Battery Temperature Monitoring

The LP8501 continuously monitors temperature by measuring the voltage between the TS and VSS pins. A negative-or a positive-temperature coefficient thermistor (NTC, PTC) and an external voltage divider typically develop this voltage (See Figure9). The LP8501 compares this voltage against its internal V(TS1) and V(TS2) thresholds to determine if charging is allowed. (See Figure10). The temperature sensing circuit is immune to any fluctuation in VCC, since both the external voltage divider and the internal thresholds (V(TS1) and V(TS2)) are referenced to VCC.

The resistor values of R(T1) and R(T2) are calculated by the following equations:

For NTC Thermistors

$$R_{T1} = \frac{5 \times R_{TH} \times R_{TC}}{3 \times (R_{TC} - R_{TH})} \quad \text{---------- (3)}$$

$$R_{T2} = \frac{5 \times R_{TH} \times R_{TC}}{[(2 \times (R_{TC}) - (7 \times R_{TH})]} \quad \text{---------- (4)}$$

Where R(TC) is the cold temperature resistance and R(TH) is the hot temperature resistance of thermistor, as specified by the thermistor manufacturer.

VRT1 or RT2 can be omitted if only one temperature (hot or cold) setting is required. Applying a voltage between the (TS1) and V(TS2) thresholds to pin TS disables the temperature-sensing feature.

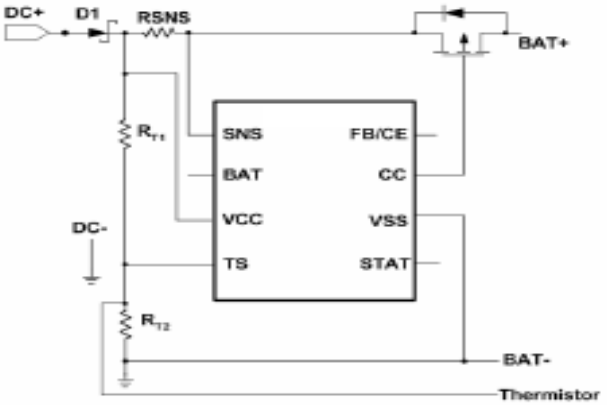
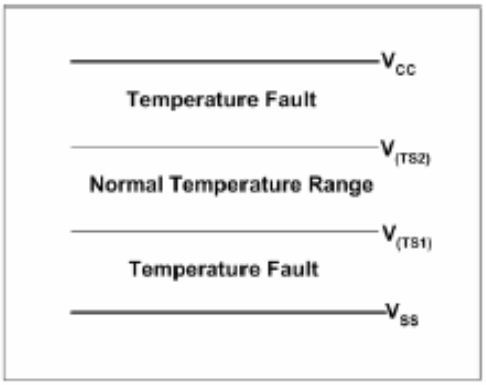


Figure9. Temperature Sensing Circuits



Charge Inhibit Function

The TS pin can be used as charge-inhibit input. The user can inhibit charge by connecting the TS pin to VCC or VSS (or any level outside the V(TS1) to V(TS2) thresholds). Applying a voltage between the V(TS1) and V(TS2) thresholds to pin TS returns the charger to normal operation.

Charge Status Indication

The LP8501 reports the status of the charger on the 3-state STAT pin. The following table summarized the operation of the
STAT pin.

Condition	STAT pin
Battery conditioning and charging	High
Charge complete(done)	Low
Temperature fault or sleep mode	Hi-Z

The STAT pin can be used to drive a single LED (Figure1), dual-chip LEDs (Figure2) or for interface to a host or system processor (Figure11). When interfacing the LP8501 to a processor, the user can use an output port, to recognize the high-Z state of the STAT pin. In this configuration, the user needs to read the input pin, toggle the output port and read the STAT pin again. In a high-Z condition, the input port always matches the signal level on the output port.

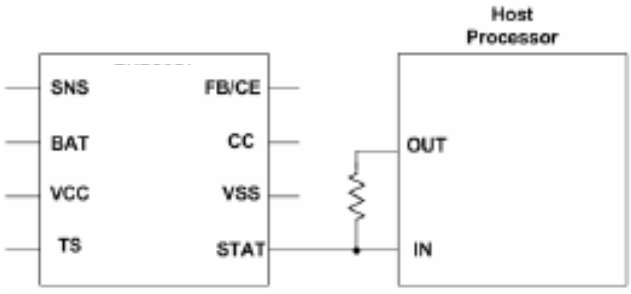


Figure10. Interfacing the LP8501 to a host processor

Low-Power Sleep Mode

When the input supply is disconnected, the charger automatically enters power-saving sleep mode. Only consuming an ultra-low 1μA in sleep mode, the LP8501 minimizes battery drain when it is not charging.

Selecting Input Capacitor

In most applications, all that is needed is high-frequency decoupling capacitor. A 0.1μF ceramic, placed in proximity to VCC and VSS pins, works well. The LP8501 works with both regulated and unregulated external dc supplies. If a non-regulated supply is chosen, the supply unit should have enough capacitance to hold up the supply voltage to the minimum required input voltage at maximum load. If not, more capacitance must be added to the input of the charger.

Selecting Output Capacitor

The LP8501 does not require any output capacitor for loop stability. In order to maintain good AC stability in the Constant Voltage mode, a minimum capacitance of 10μF is recommenced to bypass the VBAT pin to VSS. This capacitance provides compensation when there is no battery load. In addition, the battery and interconnections appear inductive at high frequencies. These elements are in the control feedback loop d＞uring Constant Voltage mode. Therefore, the bypass capacitance may be necessary to compensate for the inductive nature of the battery pack.

Virtually any good quality output filter capacitor can be used, independent of the capacitor's minimum ESR (Effective Series Resistance) value. The actual value of the capacitor and its associated ESR depends on the forward transconductance (gm) and capacitance of the external pass transistor. A 10μF tantalum or aluminum electrolytic capacitor at the output is usually sufficient to ensure stability for up to a 1A output current.

Selecting An External Pass-Device (PMOS or PNP)

The LP8501 is designed to work with both P-channel MOSFET or PNP transistor. The device should be chosen to handle the required power dissipation, given the circuit parameters, PCB layout and heat sink configuration. The following examples illustrate the design process for PMOS device:

P-Channel MOSFET

Selection steps for a P-channel MOSFET: We will use the following conditions: VI=5V (with 10% supply tolerance); I(REG)=1A, 4.2-V single-cell Li-Ion. VI is the input voltage to the charger and I(REG) is the desired charge current. (See Figure2)

1.Determine the maximum power dissipation, PD , in the transistor. The worst case power dissipation happens when the cell voltage, V(constant), is at its lowest (typically 3.1V at the beginning of current regulation phase) and VI is at its maximum. Where VD is the forward voltage drop across the reverse-blocking diode (if one is used), and VCS is the voltage drop across the current sense resistor.

PD=(VI(MAX)－VD－VCS－VBAT)×IREG --------- (7)

PD=(5.5－0.4－0.2－3.1)×1A

PD=1.8W

2.Determine the package size needed in order to keep the junction temperature below the manufacturer's recommended value, T_{JMAX}. Calculate the total theta, θ(°C/W), needed.

$$\theta_{JA} = \frac{(T_{max(J)} - T_{A(max)})}{P_D} \quad \text{----------(8)}$$

$$\theta_{JA} = \frac{(150 - 40)}{1.8} \qquad \theta_{JA} = 61°C/W$$

It is recommended to choose a package with a lower θ_{JA} than the number calculated above.

3.Select a drain-source voltage, V(DS), rating greater than the maximum input voltage. A 12V device will be adequate in this example.

4.Select a device that has at least 50% higher drain current (ID) rating than the desired charge current (REG).

5.Verify that the available drive is large enough to supply the desired charge current.

V (GS)=(VD+V(CS)+VOL(CC))－VI(min) ---------- (9)

V(GS)=(0.4+0.2+1) －4.5

V(GS)=-2.9

Where V(GS) is the gate-to-source voltage, VD is the forward voltage drop across the reverse-blocking diode (if one is used), and VCS is the voltage drop across the current sense resistor, and VOL(CC) is the

CC pin output low voltage specification for the LP8501.

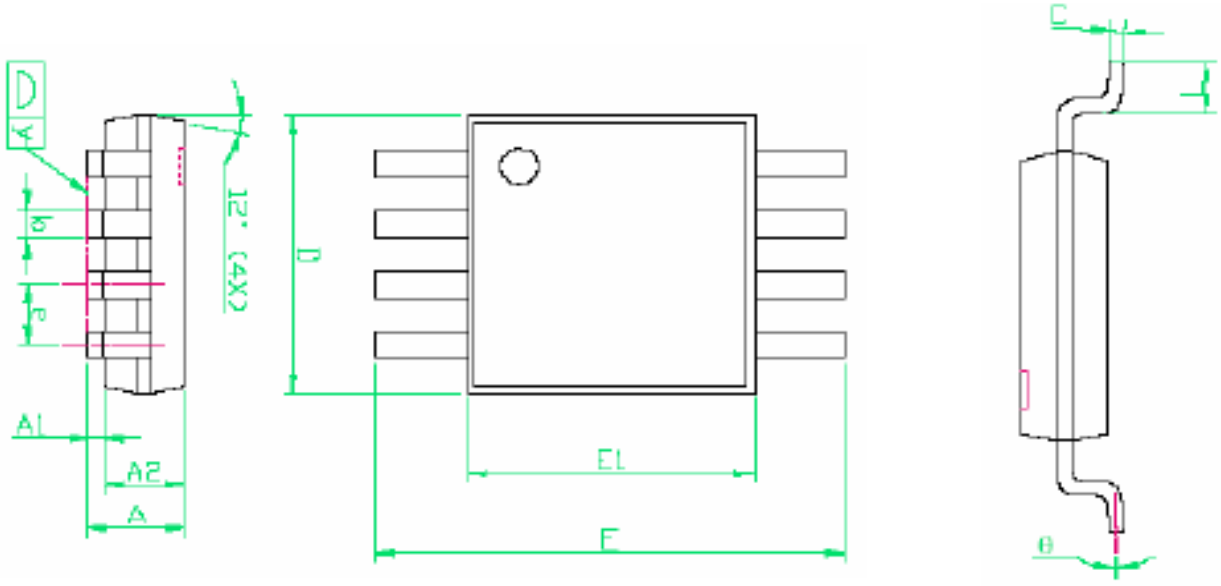
Select a MOSFET with gate threshold voltage, V(GSth), rating less than the calculated V(GS).

Reverse Blocking Protection

The optional reverse-blocking protection diode, depicted in Figure1&2 provides protection from a faulted or shorted input, or from a reversed-polarity input source. Without the protection diode, a faulted of shorted input would discharge the battery pack through the body diode of the external pass transistor.

If a reverse-protection diode is incorporated in the design, it should be chosen to handle the fast charge current continuously at the maximum ambient temperature. In addition, the reverse-leakage current of the diode should be kept as small as possible.

8-Pin MSOP



NOTE

1. Package body sizes exclude mold flash and gate burrs
2. Dimension L is measured in gage plane
3. Tolerance 0.10mm unless otherwise specified
4. Controlling dimension is millimeter. Converted inch dimensions are not necessarily exact.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.81	0.95	1.10	0.032	0.0375	0.043
A1	0.05	0.09	0.15	0.002	0.004	0.006
A2	0.76	0.86	0.97	0.030	0.034	0.038
b	0.28	0.30	0.38	0.011	0.012	0.015
C	0.13	0.15	0.23	0.005	0.006	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.70	4.90	5.10	0.185	0.193	0.201
E1	2.90	3.00	3.10	0.114	0.118	0.122
e	------	0.65	-----	------	0.026	------
L	0.40	0.53	0.66	0.016	0.021	0.026
y	------	------	0.10	------	------	0.004
θ	0	------	6	0	------	6