National Semiconductor

September 23, 2011

LP8545

High-Efficiency LED Backlight Driver for Notebooks

General Description

The LP8545 is a white LED driver with integrated boost converter. It has six adjustable current sinks which can be controlled by PWM input or with I^{2}C-compatible serial interface.

The boost converter has adaptive output voltage control based on the LED driver voltages. This feature minimizes the power consumption by adjusting the voltage to lowest sufficient level in all conditions.

LED outputs have 8-bit current resolution and up to 13-bit PWM resolution with additional 1-3 bit dithering to achieve smooth and precise brightness control. Proprietary Phase Shift PWM control is used for LED outputs to reduce peak current from the boost converter, thus making the boost capacitors smaller. The Phase Shifting scheme also eliminates audible noise.

Internal EEPROM is used for storing the configuration data. This makes it possible to have minimum external component count and make the solution very small.

LP8545 has safety features which make it possible to detect LED outputs with open or short fault. As well low input voltage and boost over-current conditions are monitored and chip is turned off in case of these events. Thermal de-rating function prevents overheating of the device by reducing backlight brightness when set temperature has been reached.

LP8545 is available in National's LLP 24-pin package.

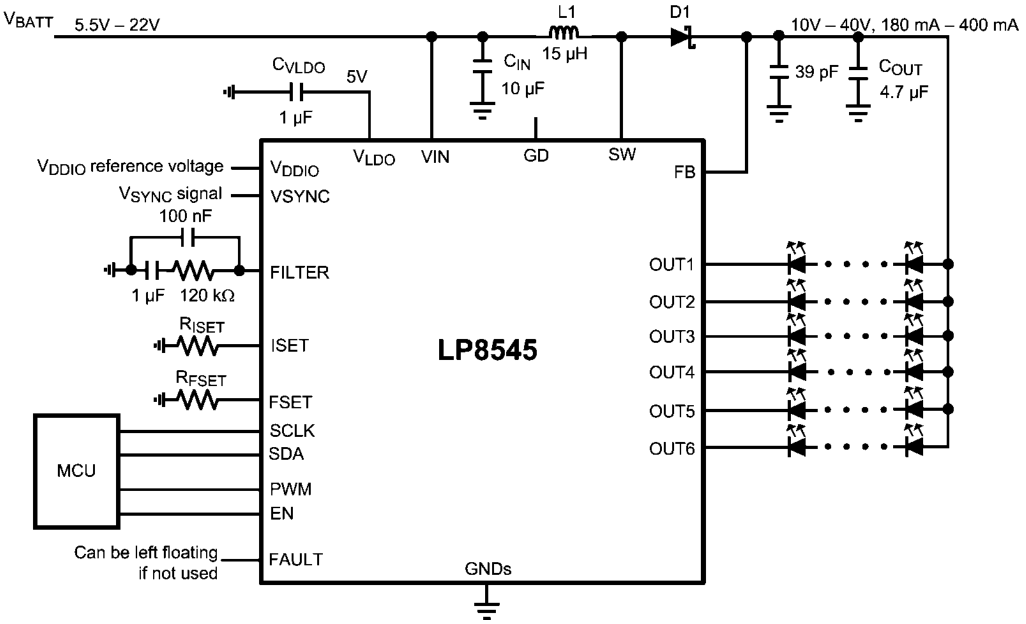
Features

- High-voltage DC/DC boost converter with integrated FET with four switching frequency options: 156/312/625/1250 kHz
- Configurable for use with external FET for applications needing higher output voltage
- 2.7V – 22V input voltage range to support 1x…5x cell Li-Ion batteries
- Programmable PWM resolution
  - 8 to 13 true bit (steady state)
  - Additional 1 to 3 bits using dithering during brightness changes
- I^{2}C and PWM brightness control
- PWM output frequency and LED current set through resistors
- Optional synchronization to display V_{SYNC} signal
- 6 LED outputs with LED fault (short/open) detection
- Low input voltage, over-temperature, over-current detection and shutdown
- Minimum number of external components
- LLP 24-pin package, 4 x 4 x 0.8 mm

Applications

- Notebook and Netbook LCD Display LED Backlight
- LED Lighting

Typical Application (1)



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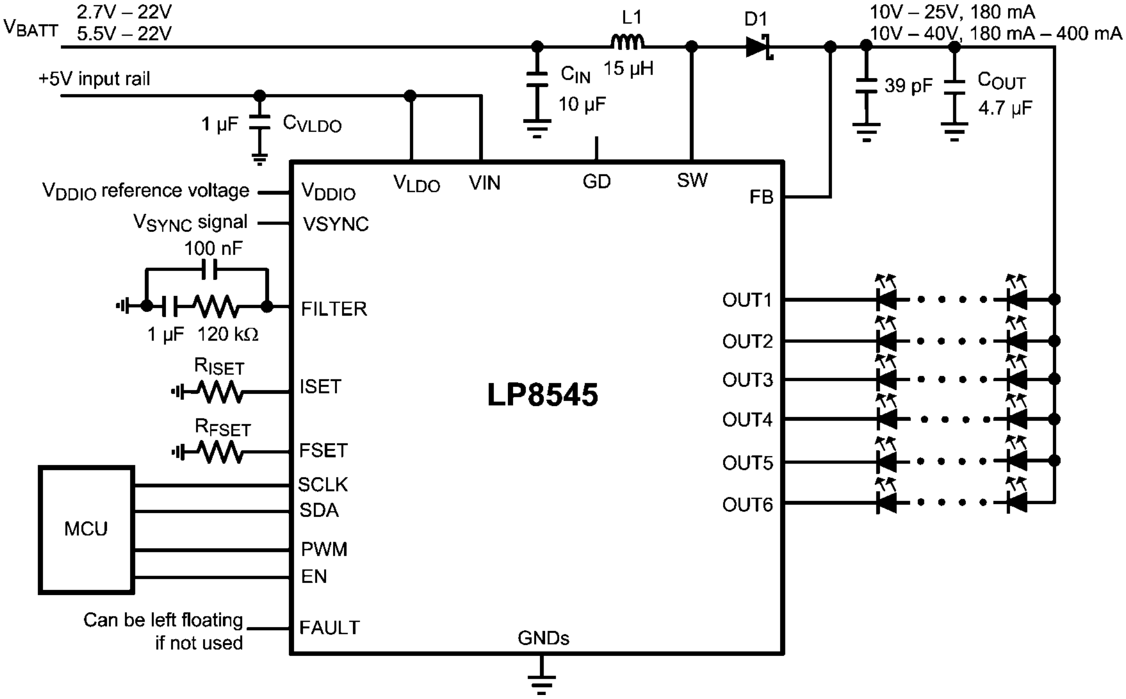
Typical Application for Low Input Voltage (2)



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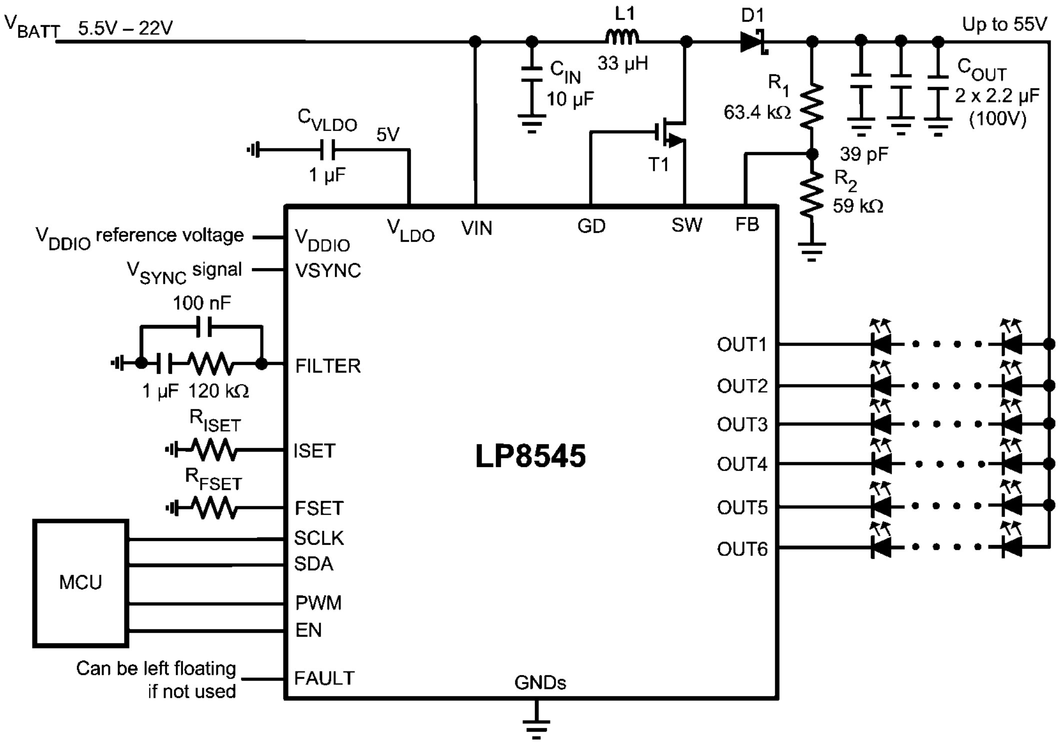
Note: Separate 5V rail to V_{LDO} can be also used to improve efficiency for applications with higher battery voltage. No power sequencing requirements between V_{IN}/V_{LDO} and V_{BATT}.

Typical Application for High Output Voltage (3)



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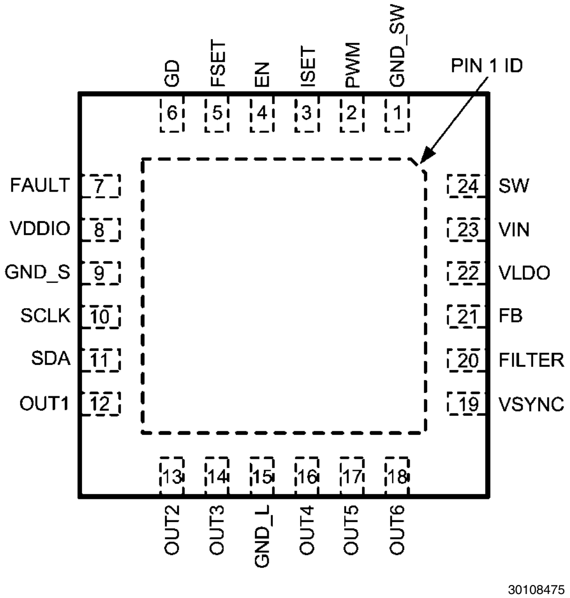
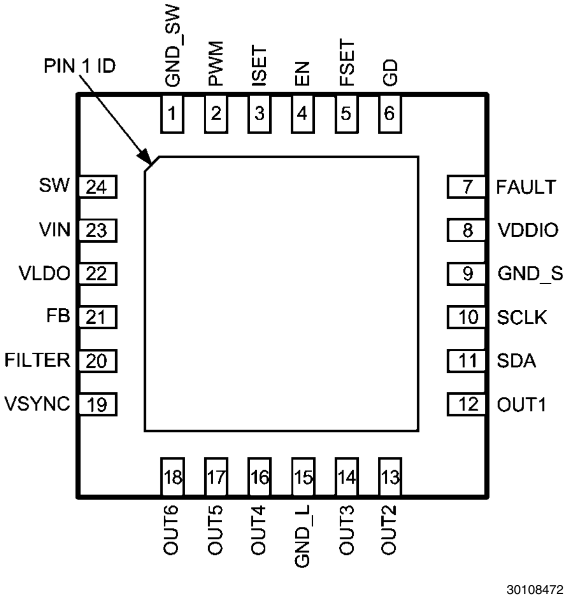
Connection Diagrams and Package Mark Information

24–pin Leadless Leadframe Package (LLP)
4.0 x 4.0 x 0.8mm, 0.5 mm pitch
NS Package Number SQA24A

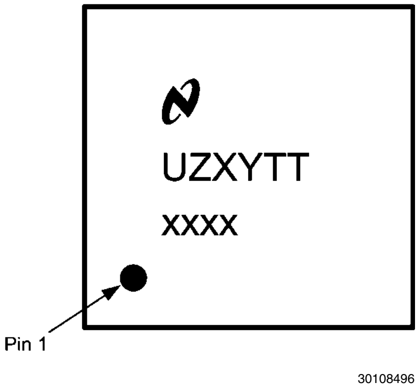


Top View



Bottom View

Package Mark



Package Mark - Top View

U = Fab
Z = Assembly
XY = 2–Digit Date Code
TT = Die Traceability
xxxx = Product Identification

Ordering Information

Order Number	Spec/flow	Package Marking	Supplied As
LP8545SQX	NOPB / HFLF	L8545SQ	4500 units, Tape-and-Reel

Pin Descriptions

Pin #	Name	Type	Description
1	GND_SW	G	Boost switch ground
2	PWM	A	PWM dimming input. This pin must be connected to GND if not used.
3	ISET	A	Set resistor for LED current. This pin can be left floating if not used.
4	EN	I	Enable input pin
5	FSET	A	PWM frequency set resistor. This pin can be left floating if not used.
6	GD	A	Gate driver for external FET. If not used, can be left floating.
7	FAULT	OD	Fault indication output. If not used, can be left floating.
8	VDDIO	P	Digital IO reference voltage (1.65V...5V) for I²C interface. If brightness is controlled with PWM input pin then this pin can be connected to GND.
9	GND_S	G	Signal ground
10	SCLK	I	Serial clock. This pin must be connected to GND if not used.
11	SDA	I/O	Serial data. This pin must be connected to GND if not used.
12	OUT1	A	Current sink output
13	OUT2	A	Current sink output
14	OUT3	A	Current sink output
15	GND_L	G	LED ground
16	OUT4	A	Current sink output
17	OUT5	A	Current sink output
18	OUT6	A	Current sink output
19	VSYNC	I	V_{SYNC} input. This pin must be connected to GND if not used.
20	FILTER	A	Low pass filter for PLL. This pin can be left floating if not used.
21	FB	A	Boost feedback input
22	VLDO	P	LDO output voltage. External 5V rail can be connected to this pin in low voltage application.
23	VIN	P	Input power supply up to 22V. If 2.7V ≤ VBATT < 5.5V (*Typical Application for Low Input Voltage (2)*) then external 5V rail must be used for VLDO and VIN.
24	SW	A	Boost switch. With external FET (typ. app. (3)) this pin acts as a current sense.

A: Analog Pin, G: Ground Pin, P: Power Pin, I: Input Pin, I/O: Input/Output Pin, O: Output Pin, OD: Open Drain Pin

Absolute Maximum Ratings (Note 1, Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN}	-0.3V to +24.0V
V_{LDO}	-0.3V to +6.0V
Voltage on Logic Pins (VSYNC, PWM, EN, SCLK, SDA)	-0.3V to +6.0V
Voltage on Logic Pin (FAULT)	-0.3V to VDDIO + 0.3V
Voltage on Analog Pins (FILTER, GD, VDDIO, ISET, FSET)	-0.3V to +6.0V
V (OUT1...OUT6, SW, FB)	-0.3V to +44.0V
Continuous Power Dissipation (Note 3)	Internally Limited
Junction Temperature ($T_{J\text{-}MAX}$)	125°C
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Soldering)	(Note 4)
ESD Rating	(Note 5)
Human Body Model:	2 kV
Machine Model:	200V
Charged Device Model:	1 kV

Operating Ratings (Note 1, Note 2)

Input Voltage Range (V_{IN}) typ. app. (1), (3)	5.5V to 22.0V
Input Voltage Range (V_{IN} + V_{LDO}) typ. app. (2)	4.5V to 5.5V
V_{DDIO}	1.65V to 5V
V(OUT1...OUT6, SW, FB)	0V to 40V
Junction Temperature (T_J) Range	-30°C to +125°C
Ambient Temperature (T_A) Range (Note 6)	-30°C to +85°C

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), SQA Package (Note 7)	35 to 50°C/W

Electrical Characteristics (Note 2, Note 8)

Limits in standard typeface are for T_A = 25°C. Limits in **boldface** type apply over the full operating ambient temperature range (-30°C ≤ T_A ≤ +85°C). Unless otherwise specified: V_{IN} = 12.0V, C_{VLDO} = 1 µF, L1 = 15 µH, C_{IN} = 10 µF, C_{OUT} = 10 µF. R_{ISET} = 16 kΩ (Note 9)

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{IN}	Standby Supply Current	Internal LDO disabled EN=L and PWM=L			**1**	µA
	Normal Mode Supply Current	LDO enabled, boost enabled, no current going through LED outputs, Internal FET used 5 MHz PLL Clock		4.0		mA
		10 MHz PLL Clock		4.8		
		20 MHz PLL Clock		6.0		
		40 MHz PLL Clock		8.4		
f_{OSC}	Internal Oscillator Frequency Accuracy		-4 **-7**		+4 **+7**	%
V_{LDO}	Internal LDO Voltage		**4.5**	5.0	**5.5**	V
I_{LDO}	Internal LDO External Loading				5.0	mA

Boost Converter Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
RDS_{ON}	Switch ON Resistance	I_{SW} = 0.5A		0.12		Ω
V_{MAX}	Boost Maximum Output Voltage			40		V
I_{LOAD}	Maximum Continuous Load Current, Internal FET	9.0V ≤ V_{BATT}, V_{OUT} = 35V		450		mA
		6.0V ≤ V_{BATT}, V_{OUT} = 35V		300		
		3.0V ≤ V_{BATT}, V_{OUT} = 25V		180		
I_{LOAD}	Maximum Continuous Load Current, External FET	9.0V ≤ V_{BATT}, V_{OUT} = 50V		320		mA
		6.0V ≤ V_{BATT}, V_{OUT} = 50V		190		

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}/V_{IN}	Conversion Ratio				10	
f_{SW}	Switching Frequency	BOOST_FREQ = 00		156		kHz
		BOOST_FREQ = 01		312		
		BOOST_FREQ = 10		625		
		BOOST_FREQ = 11		1250		
V_{OV}	Over-voltage Protection Voltage	$V_{BOOST} \geq 38V$		$V_{BOOST} + 1.6V$		V
		$V_{BOOST} < 38V$		$V_{BOOST} + 4V$		
t_{PULSE}	Switch Pulse Minimum Width	no load		50		ns
$t_{STARTUP}$	Startup Time	(Note 10)		6		ms
I_{MAX}	SW Pin Current Limit	BOOST_IMAX[1:0] = 00		0.9		A
		BOOST_IMAX[1:0] = 01		1.4		
		BOOST_IMAX[1:0] = 10		2.0		
		BOOST_IMAX[1:0] = 11		2.5		
V_{GD}	Gate Driver Pin Voltage	EN_EXT_FET = 1	0		VLDO	V

LED Driver Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{LEAKAGE}$	Leakage Current	Outputs OUT1...OUT6, V_{OUT} = 40V		0.1	1	µA
I_{MAX}	Maximum Source Current OUT1...OUT6	EN_I_RES = 0, CURRENT[7:0] = FFh		30		mA
		EN_I_RES = 1		50		
I_{OUT}	Output Current Accuracy (Note 11)	Output current set to 23 mA, EN_I_RES = 1	-3		+3	%
			-4		**+4**	
I_{MATCH}	Matching (Note 11)	Output current set to 23 mA, EN_I_RES = 1		0.5		%
PWM_{RES}	PWM Output Resolution (Note 14)	f_{LED} = 5 kHz, f_{PLL} = 5 MHz		10		bits
		f_{LED} = 10 kHz, f_{PLL} = 5 MHz		9		
		f_{LED} = 20 kHz, f_{PLL} = 5 MHz		8		
		f_{LED} = 5 kHz, f_{PLL} = 40 MHz		13		
		f_{LED} = 10 kHz, f_{PLL} = 40 MHz		12		
		f_{LED} = 20 kHz, f_{PLL} = 40 MHz		11		
f_{LED}	LED Switching Frequency (Note 14)	PWM_FREQ[4:0] = 00000b PLL clock 5 MHz		600		Hz
		PWM_FREQ[4:0] = 11111b PLL clock 5 MHz		19.2k		
V_{SAT}	Saturation Voltage (Note 12)	Output current set to 20 mA	**55**	120	**175**	mV
		Output current set to 30 mA	**80**	180	**270**	

PWM Interface Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PWM}	PWM Frequency Range		0.1		25	kHz
t_{MIN_ON}	Minimum Pulse ON time			1		µs
t_{MIN_OFF}	Minimum Pulse OFF time			1		
$t_{STARTUP}$	Turn on delay from standby to backlight on	PWM input active, EN pin rise from low to high		6		ms
T_{STBY}	Turn Off Delay	PWM input low time for turn off, slope disabled		50		ms
PWM_{RES}	PWM Input Resolution	f_{IN} < 9.0 kHz		10		bits
		f_{IN} < 4.5 kHz		11		
		f_{IN} < 2.2 kHz		12		
		f_{IN} < 1.1 kHz		13		

Under-Voltage Protection

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{UVLO}	V_{IN} UVLO Threshold Voltage	UVLO[1:0] = 00		Disabled		V
		UVLO[1:0] = 01, falling	2.55	2.70	2.94	
		UVLO[1:0] = 01, rising	2.62	2.76	3.00	
		UVLO[1:0] = 10, falling	5.11	5.40	5.68	
		UVLO[1:0] = 10, rising	5.38	5.70	5.98	
		UVLO[1:0] = 11, falling	7.75	8.10	8.45	
		UVLO[1:0] = 11, rising	8.36	8.73	9.20	

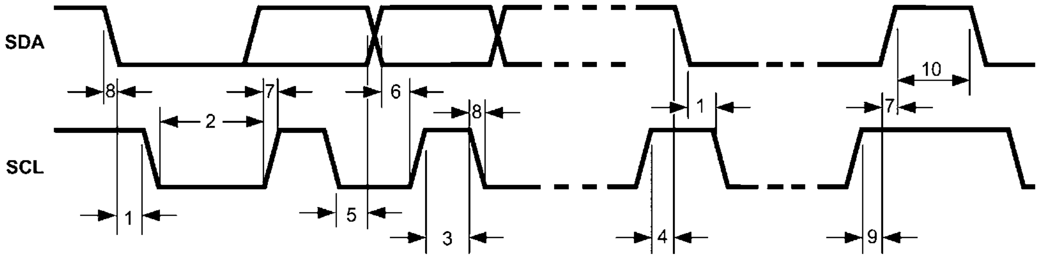
Logic Interface Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Logic Input EN						
V_{IL}	Input Low Level				**0.4**	V
V_{IH}	Input High Level		**1.2**			V
I_I	Input Current		**-1.0**		**1.0**	µA
Logic Input VSYNC						
V_{IL}	Input Low Level				**0.4**	V
V_{IH}	Input High Level		**2.2**			V
I_I	Input Current		**-1.0**		**1.0**	µA
f_{VSYNC}	Frequency Range		58	60	55000	Hz
Logic Input PWM						
V_{IL}	Input Low Level				**0.4**	V
V_{IH}	Input High Level		**2.2**			V
I_I	Input Current		**-1.0**		**1.0**	µA
Logic Inputs SCL, SDA						
V_{IL}	Input Low Level				**$0.2xV_{DDIO}$**	V
V_{IH}	Input High Level		**$0.8xV_{DDIO}$**			V
I_I	Input Current		**-1.0**		**1.0**	µA
Logic Outputs SDA, FAULT						
V_{OL}	Output Low Level	I_{OUT} = 3 mA (pull-up current)		0.3	**0.5**	V
I_L	Output Leakage Current	V_{OUT} = 2.8V	**-1.0**		**1.0**	µA

I²C Serial Bus Timing Parameters (SDA, SCLK) (*Note 13*)

Symbol	Parameter	Limit		Units
		Min	Max	
f_{SCLK}	Clock Frequency		400	kHz
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		µs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time	50		ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	$20+0.1C_b$	300	ns
8	Fall Time of SDA and SCL	$15+0.1C_b$	300	ns
9	Set-up Time for STOP condition	600		ns

10	Bus Free Time between a STOP and a START Condition	1.3		μs
C_b	Capacitive Load Parameter for Each Bus Line Load of 1 pF corresponds to 1 ns.	10	200	ns



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Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pins.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 130°C (typ.).

Note 4: For detailed soldering specifications and information, please refer to National Semiconductor AN1187: *Leadless Leadframe Package (LLP).*

Note 5: Human Body Model, applicable standard JESD22-A114C. Machine Model, applicable standard JESD22- A115-A. Charged Device Model, applicable standard JESD22A-C101.

Note 6: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} - (\theta_{JA} \times P_{D\text{-}MAX})$.

Note 7: Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

Note 8: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Note 9: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

Note 10: Start-up time is measured from the moment boost is activated until the V_{OUT} crosses 90% of its target value.

Note 11: Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current sinks on the part (OUT1 to OUT6), the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Two matching numbers are calculated: (MAX-AVG)/AVG and (AVG-MIN/AVG). The largest number of the two (worst case) is considered the matching figure. The typical specification provided is the most likely norm of the matching figure for all parts. Note that some manufacturers have different definitions in use.

Note 12: Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at 1V.

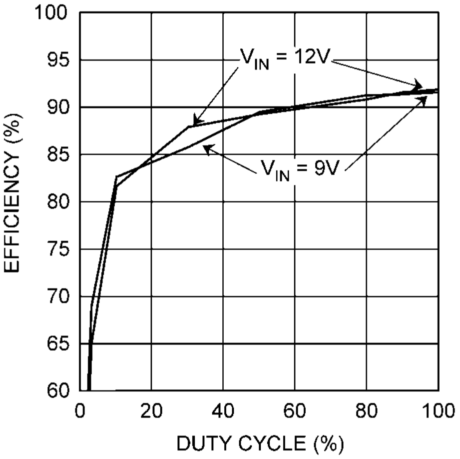
Note 13: Guaranteed by design. V_{DDIO} = 1.65V to 5.5V.

Note 14: PWM output resolution and frequency depend on the PLL settings. Please see section “PWM Frequency Settings” for full description

Typical Performance Characteristics

Unless otherwise specified: V_{BATT} = 12.0V, C_{VLDO} = 1 µF, L1 = 33 µH, C_{IN} = 10 µF, C_{OUT} = 10 µF

LED Drive Efficiency, f_{LED} = 19.2 kHz



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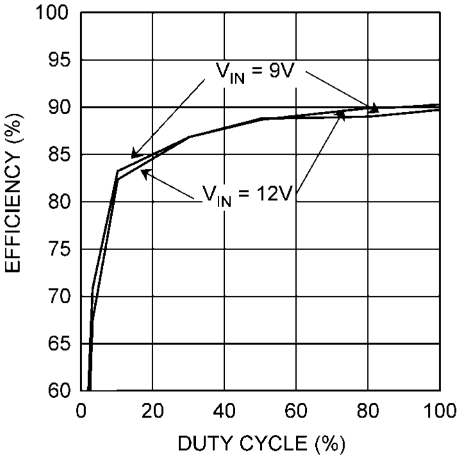
LED Drive Efficiency, f_{LED} = 19.2 kHz, L1 = 15 µH



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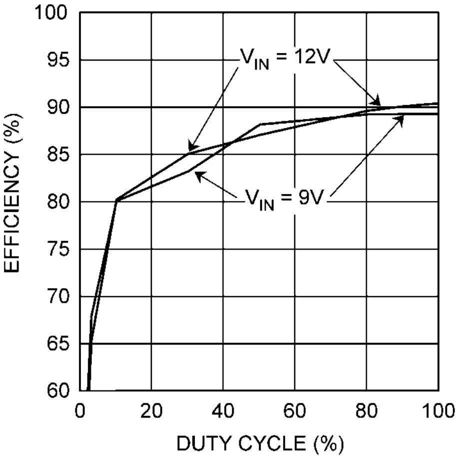
LED Drive Efficiency, f_{LED} = 19.2 kHz, External FET



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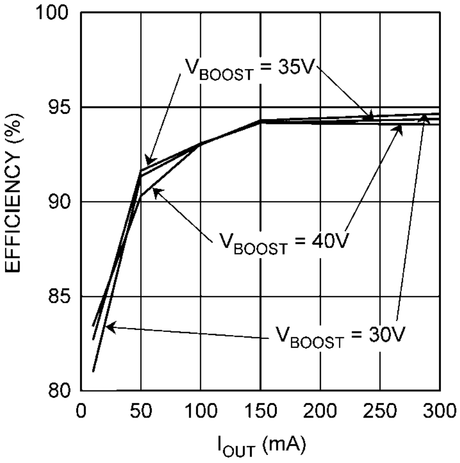
Boost Converter Efficiency



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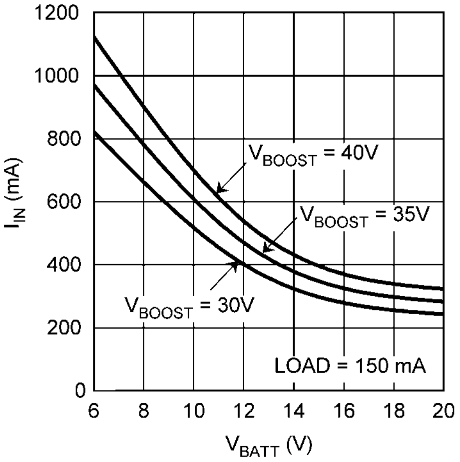
Battery Current



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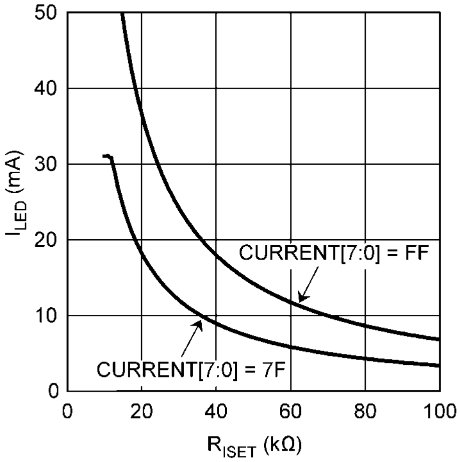
I_{LED} vs. R_{ISET}



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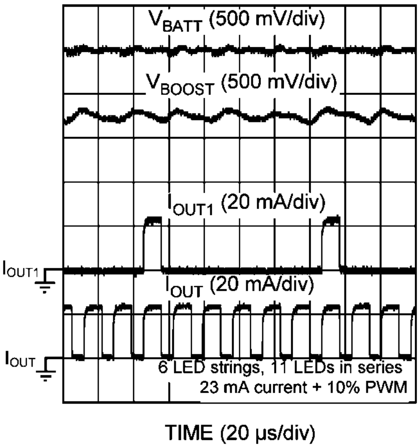
Typical Waveforms, f_{LED} = 9.6 kHz



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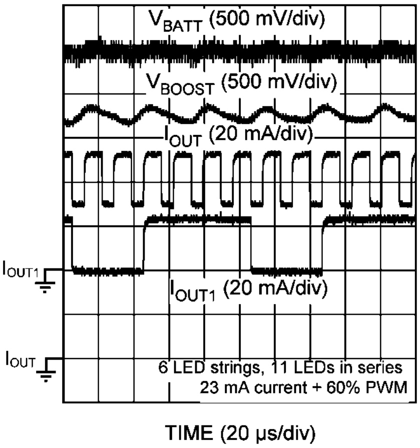
Typical Waveforms, f_{LED} = 9.6 kHz



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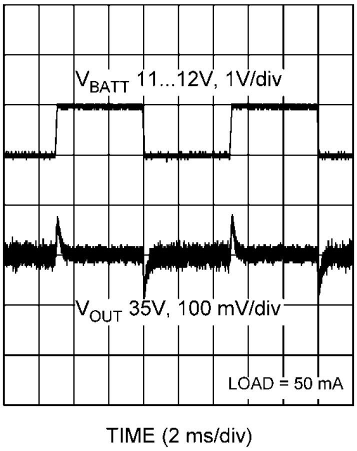
Boost Line Transient Response



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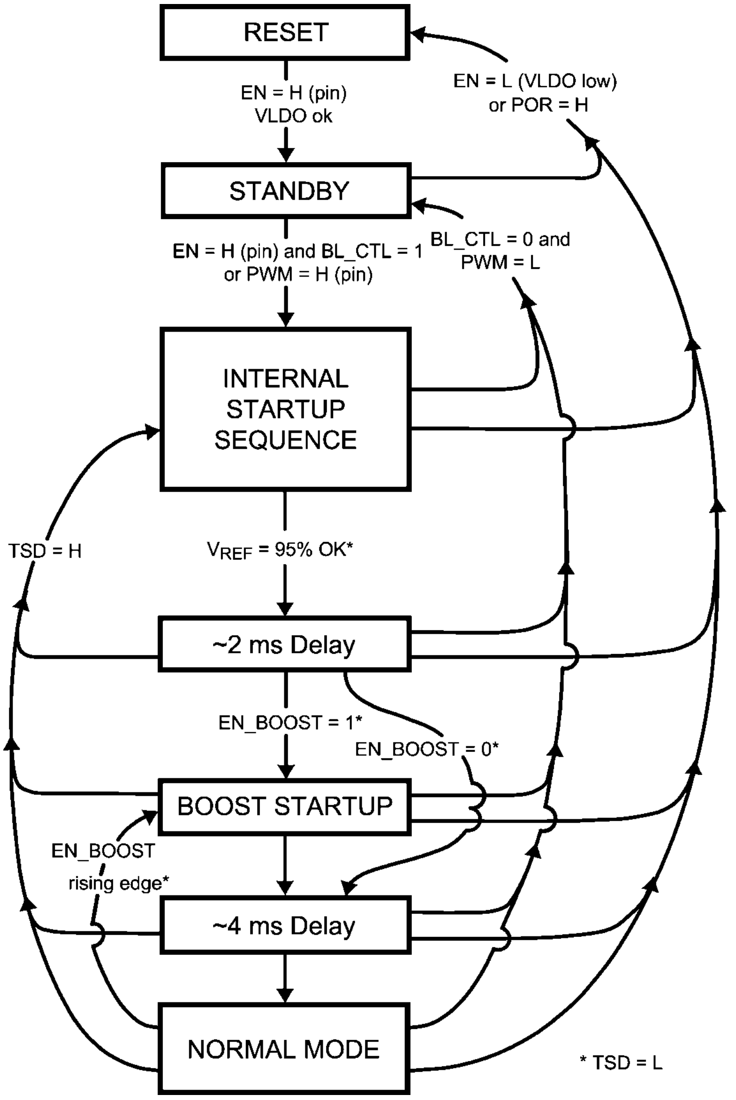
Modes of Operation



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RESET:	In the RESET mode all the internal registers are reset to the default values. Reset is entered always VLDO voltage is low. EN pin is enable for the internal LDO. Power On Reset (POR) will activate during the chip startup or when the supply voltage VLDO fall below POR level. Once VLDO rises above POR level, POR will inactivate and the chip will continue to the STANDBY mode.
STANDBY:	The STANDBY mode is entered if the register bit BL_CTL is LOW and external PWM input is not active and POR is not active. This is the low-power consumption mode, when only internal 5V LDO is enabled. Registers can be written in this mode and the control bits are effective immediately after startup.
STARTUP:	When BL_CTL bit is written high or PWM signal is high, the INTERNAL STARTUP SEQUENCE powers up all the needed internal blocks (VREF, Bias, Oscillator etc.). Internal EPROM and EEPROM are read in this mode. To ensure the correct oscillator initialization etc, a 2 ms delay is generated by the internal state-machine. If the chip temperature rises too high, the Thermal Shutdown (TSD) disables the chip operation and STARTUP mode is entered until no thermal shutdown event is present.
BOOST STARTUP:	Soft start for boost output is generated in the BOOST STARTUP mode. The boost output is raised in low current PWM mode during the 4 ms delay generated by the state-machine. All LED outputs are off during the 4 ms delay to ensure smooth startup. The Boost startup is entered from Internal Startup Sequence if EN_BOOST is HIGH.
NORMAL:	During NORMAL mode the user controls the chip using the external PWM input or with Control Registers through I^{2}C. The registers can be written in any sequence and any number of bits can be altered in a register in one write.

Functional Overview

LP8545 is a high voltage LED driver for medium sized LCD backlight applications. It includes high voltage boost converter which can be used either with internal FET or with external FET depending on boost output voltage requirements. Boost voltage automatically sets to the correct level needed to drive the LED strings. This is done by monitoring LED output voltage drop in real time.

Six constant current sinks with PWM control are used for driving LEDs. Constant current value is set with EEPROM bits and with R_{ISET} resistor. Brightness (PWM) is controlled either with I^2C register or with PWM input. PWM frequencies are set with EEPROM bits and with R_{FSET} resistor. Special Phase-Shift PWM mode can be used to reduce boost output current peak, thus reducing output ripple, capacitor size and audible noise.

With LP8545 it is possible to synchronize the PWM output frequency to V_{SYNC} signal received from video processor. Internal PLL ensures that the PWM output clock is always synchronized to the V_{SYNC} signal.

Special dithering mode makes it possible to increase output resolution during fading between two brightness values and by this making the transition look very smooth with virtually no stepping. Transition slope time can be adjusted with EEPROM bits.

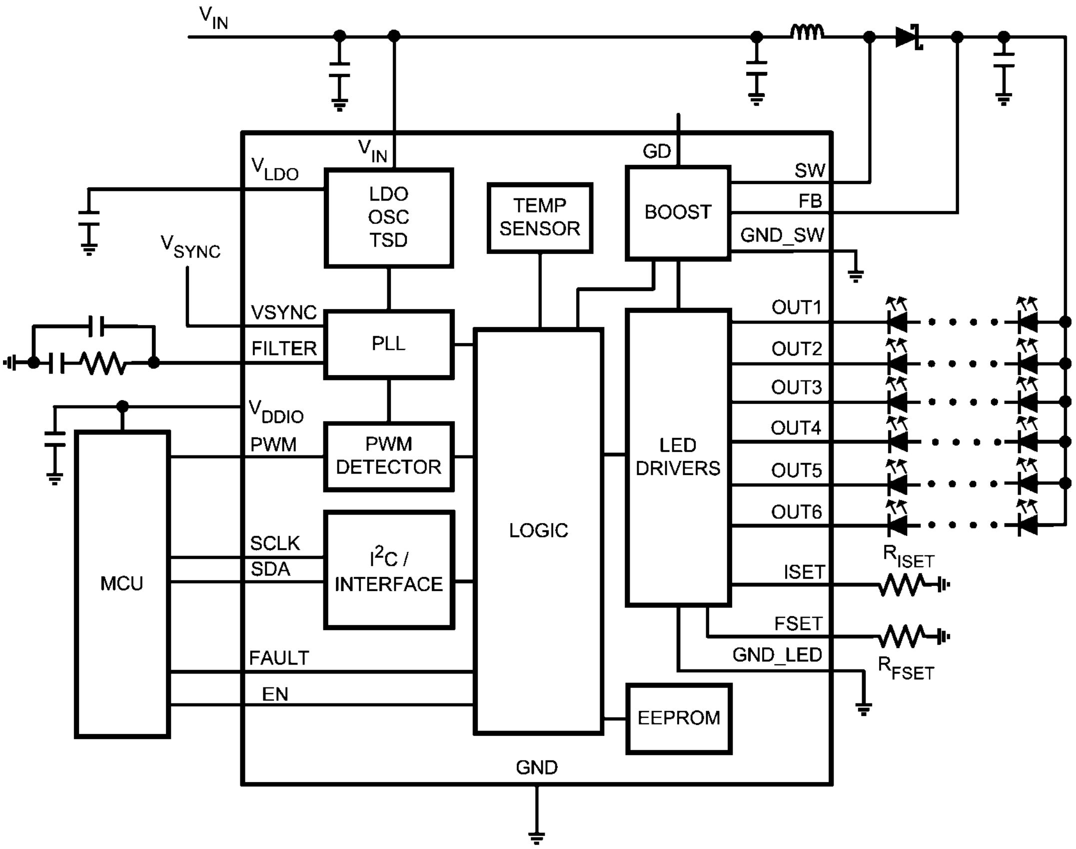
Safety features include LED fault detection with open and short detection. LED fault detection will prevent system overheating in case of open in some of the LED strings. Chip internal temperature is constantly monitored and based on this LP8545 can reduce the brightness of the backlight to reduce thermal loading once certain trip point is reached. Threshold is programmable in EEPROM. If chip internal temperature reaches too high, the boost converter and LED outputs are completely turned off until the internal temperature has reached acceptable level. Boost converter is protected against too high load current and over-voltage. LP8545 notifies the system about the fault through I^2C register and with FAULT pin.

EEPROM programmable functions include:

- PWM frequencies
- Phase shift PWM mode
- LED constant current
- Boost output frequency
- Temperature thresholds
- Slope for brightness changes
- Dithering options
- PWM output resolution
- Boost control bits

External components R_{ISET} and R_{FSET} can also be used for selecting the output current and PWM frequencies.

Block Diagram



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Clock Generation

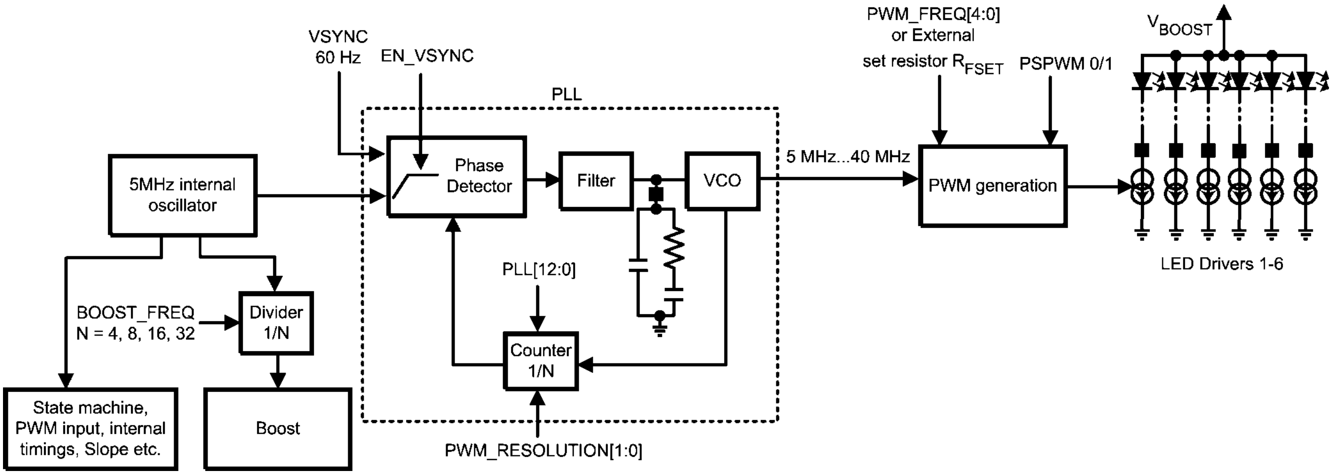
LP8545 has internal 5 MHz oscillator which is used for clocking the boost converter, state machine, PWM input duty cycle measurement, internal timings such as slope time for output brightness changes.

Internal clock can be used for generating the PWM output frequency. In this case the 5 MHz clock can be multiplied with the internal PLL to achieve higher resolution. The higher the clock frequency for PWM generation block, the higher the resolution but the tradeoff is higher IQ of the part. Clock multiplication is set with <PWM_RESOLUTION[1:0]> EEPROM Bits.

The PLL can also be used for generating the required PWM generation clock from the V_{SYNC} signal. This makes sure that the LED output PWM is always synchronized to the V_{SYNC} signal and there is no clock variation between LCD display video update and the LED backlight output frequency. Also H_{SYNC} signal up to 55 kHz can be used.

PLL has internal counter which has 13-bit control <PLL[12:0]> to achieve correct output clock frequency based on the V_{SYNC} frequency.

For the PLL it can take couple of seconds to synchronize to 60 Hz V_{SYNC} signal in startup and before this correct PWM clock frequency is generated from internal oscillator. FILTER pin component selection affects the time it takes from the PLL to lock to V_{SYNC} signal. When backlight is turned off the EN pin must be set low to ensure correct PLL behavior during next startup.



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Principle of the Clock Generation

Brightness Control Methods

LP8545 controls the brightness of the backlight with PWM. PWM control is received either from PWM input pin or from I^{2}C register bits. The PWM source selection is done with <BRT_MODE[1:0]> bits as follows:

BRT_MODE [1]	BRT_MODE [0]	PWM source
0	0	PWM input pin duty cycle control. Default.
0	1	PWM input pin duty cycle control.
1	0	Brightness register
1	1	PWM direct control (PWM in = PWM out)

PWM INPUT DUTY CYCLE

With PWM input pin duty cycle control the output PWM is controlled by PWM input duty cycle. PWM detector block measures the duty cycle in the PWM pin and uses this 13-bit value to generate the output PWM. Output PWM can have different frequency than input in this mode and also phase shift PWM mode can be used. Slope and dither are effective in this mode. PWM input resolution is defined by the input PWM clock frequency.

BRIGHTNESS REGISTER CONTROL

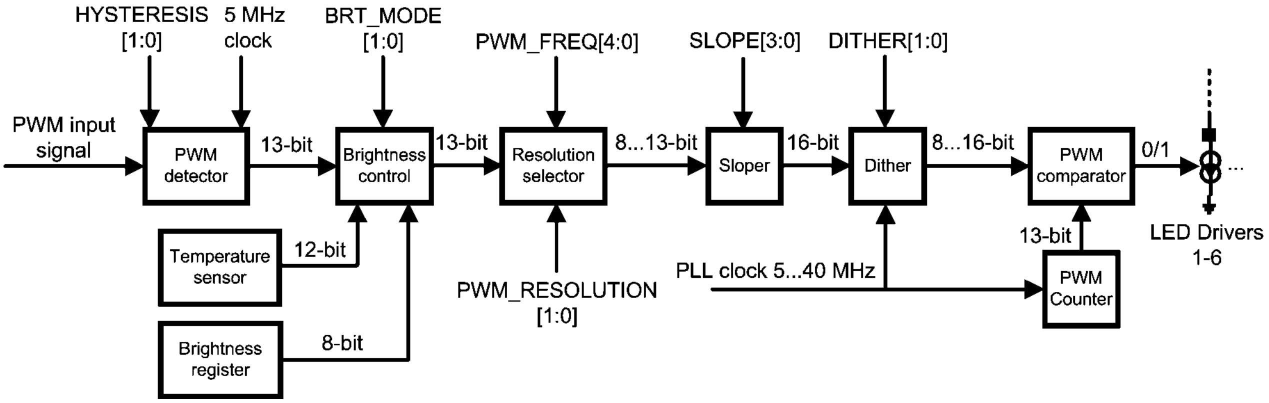
With brightness register control the output PWM is controlled with 8-bit resolution <BRT7:0> register bits. Phase shift scheme can be used with this and the output PWM frequency can be freely selected. Slope and dither are effective in this mode.

PWM DIRECT CONTROL

With PWM direct control the output PWM will directly follow the input PWM. Due to the internal logic structure the input is anyway clocked with the 5 MHz clock or the PLL clock. PSPWM mode is not possible in this mode. Slope and dither are not effective in this mode.

PWM CALCULATION DATA FLOW

Below is flow chart of the PWM calculation data flow. In PWM direct control mode most of the blocks are bypassed and this flow chart does not apply.



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PWM Calculation Data Flow

PWM DETECTOR

PWM detector block measures the duty cycle of the input PWM signal. Resolution depends on the input signal frequency. Hysteresis selection sets the minimum allowable change to the input. If smaller change is detected, it is ignored. With hysteresis the constant changing between two brightness values is avoided if there is small jitter in the input signal.

BRIGHTNESS CONTROL

Brightness control block gets 13-bit value from the PWM detector, 12-bit value from the temperature sensor and also 8-bit value from the brightness register. <BRT_MODE[1:0]> selects whether to use PWM input duty cycle value or the brightness register value as described earlier. Based on the temperature sensor value the duty cycle is reduced if the temperature has reached the temperature limit set to the <TEMP_LIM[1:0]> EEPROM bits.

RESOLUTION SELECTOR

Resolution selector takes the necessary MSB bits from the input data to match the output resolution. For example if 11-bit resolution is used for output, then 11 MSB bits are selected from the input. Dither bits are not taken into account for the output resolution. This is to make sure that in steady state condition, there is no dithering used for the output.

SLOPER

Sloper makes the smooth transition from one brightness value to another. Slope time can be adjusted from 0 to 500 ms with <SLOPE[3:0]> EEPROM bits. The sloper output is 16-bit value.

DITHER

With dithering the output resolution can be “artificially” increased during sloping from one brightness value to another. This way the brightness change steps are not visible to eye. Dithering can be from 0 to 3 bits, and is selected with <DITHER[1:0]> EEPROM bits.

PWM COMPARATOR

The PWM counter clocks the PWM comparator based on the duty cycle value received from Dither block. Output of the PWM comparator controls directly the LED drivers. If PSPWM mode is used, then the signal to each LED output is delayed certain amount.

CURRENT SETTING

Maximum current of the LED outputs is controlled with CURRENT[7:0] EEPROM register bits linearly from 0 to 30 mA. If EN_I_RES = 1 the maximum LED output current can be scaled also with external resistor, R_{ISET}. R_{ISET} controls the LED current as follows:

$$I_{LED} = \frac{600 * 1.23V}{R_{ISET}} * \frac{CURRENT\ [7:0]}{255}$$

Default value for CURRENT[7:0] = 7Fh (127d). Therefore the output current can be calculated as follows:

$$R_{ISET} = \frac{600 * 1.23}{I_{LED}} * \frac{1}{2} = \frac{369}{I_{LED}}$$

E.g. If 16 kΩ R_{ISET} resistor is used, then the LED maximum current is 23 mA. Note: formula is only approximation for the actual current.

PWM FREQUENCY SETTING

PWM frequency is selected with PWM_FREQ[4:0] EEPROM register. If PLL clock frequency multiplication is used, it will effect to the output PWM frequency as well. <PWM_RESOLUTION[1:0]> EEPROM bits will select the PLL output frequency and hence the PWM frequency and resolution. Below are listed PWM frequencies with <EN_VSYNC]> = 0. PWM resolution setting affects the PLL clock frequency (5 MHz… 40 MHz). Highlighted frequencies with boldface can be selected also with external resistor R_{FSET}. To activate R_{FSET} frequency selection the <EN_F_RES> EEPROM bit must be 1.

PWM_RES[1:0]	00	01	10	11	
PWM FREQ[4:0]	**5 MHz**	**10 MHz**	**20 MHz**	**40 MHz**	**Resolution (bits)**
11111	**19232**	-	-	-	8
11110	**16828**	-	-	-	8
11101	**14424**	-	-	-	8
11100	**12020**	-	-	-	8
11011	**9616**	**19232**	-	-	9
11010	**7963**	**15927**	-	-	9
11001	**6386**	**12771**	-	-	9
11000	**4808**	**9616**	**19232**	-	10
10111	4658	9316	18631	-	10
10110	4508	9015	18030	-	10
10101	4357	**8715**	17429	-	10
10100	4207	8414	16828	-	10
10011	4057	8114	**16227**	-	10
10010	3907	**7813**	15626	-	10
10001	3756	7513	15025	-	10
10000	3606	7212	**14424**	-	10
01111	3456	6912	13823	-	10
01110	3306	6611	13222	-	10
01101	3155	**6311**	12621	-	10
01100	3005	6010	**12020**	-	10
01011	2855	5710	11419	-	10
01010	2705	5409	10818	-	10
01001	2554	5109	10217	-	10
01000	2404	**4808**	**9616**	**19232**	11
00111	2179	4357	8715	**17429**	11
00110	1953	3907	**7813**	**15626**	11
00101	1728	3456	6912	13823	11
00100	1503	3005	**6010**	**12020**	11
00011	1202	2404	**4808**	**9616**	12
00010	1052	2104	4207	**8414**	12
00001	826	1653	3306	**6611**	12
00000	601	1202	2404	**4808**	13

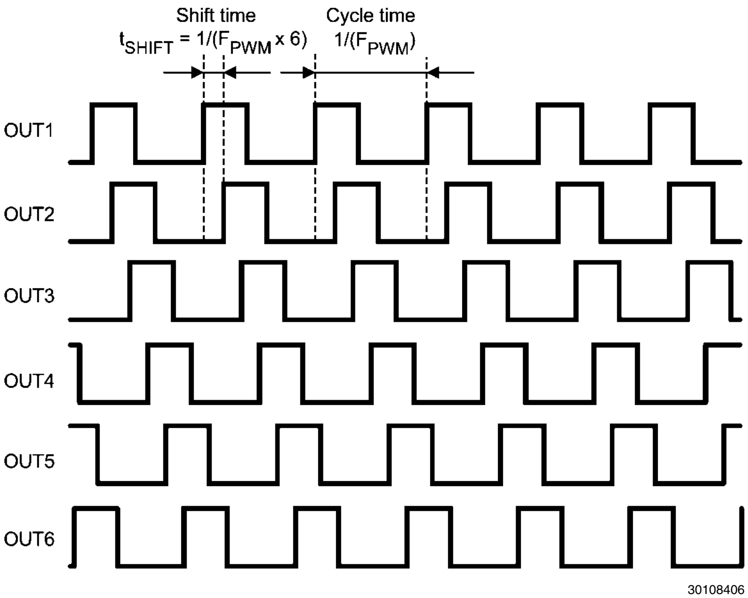
R_{FSET} resistance values with corresponding PWM frequencies:

PWM_RES[1:0]	00		01		10		11	
RFSET (kΩ)	**5 MHz Clock**	**Resolution**	**10 MHz Clock**	**Resolution**	**20 MHz Clock**	**Resolution**	**40 MHz Clock**	**Resolution**
10...15	19232	8	19232	9	19232	10	19232	11
26...29	16828	8	15927	9	16227	10	17429	11
36...41	14424	8	12771	9	14424	10	15626	11
50...60	12020	8	9616	10	12020	10	12020	11
85...100	9616	9	8715	10	9616	11	9616	12
135...150	7963	9	7813	10	7813	11	8414	12
200...300	6386	9	6311	10	6010	11	6811	12
450...	4808	10	4808	11	4808	12	4808	13

PHASE SHIFT PWM SCHEME

Phase shift PWM scheme allows delaying the time when each LED output is active. When the LED output are not activated simultaneously, the peak load current from the boost output is greatly decreased. This reduces the ripple seen on the boost output and allows smaller output capacitors. Reduced ripple also reduces the output ceramic capacitor audible ringing. PSPWM scheme also increases the load frequency seen on boost output by x6 and therefore transfers the possible audible noise to so high frequency that human ear cannot hear it.

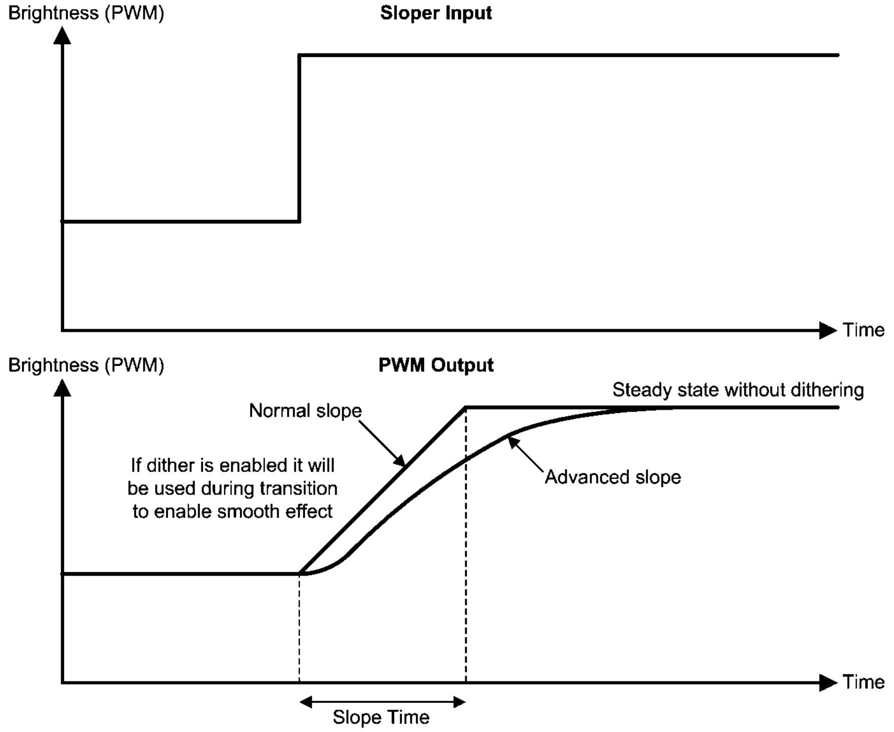
Description of the PSPWM mode is seen on the following diagram. PSPWM mode is enabled by setting <EN_PSPWM> EEPROM bit to 1. Shift time is the delay between outputs and it is defined as 1 / (f_{PWM} x 6). If the <EN_PSPWM> bit is 0, then the delay is 0 and all outputs are active simultaneously.



Phase Shift PWM Mode

SLOPE AND DITHERING

During transition between two brightness (PWM) values special dithering scheme is used if the slope is enabled. It allows increased resolution and smaller average steps size. Dithering is not used in steady state condition. Slope time can be programmed with EEPROM bits <SLOPE[3:0]> from 0 to 500 ms. Same slope time is used for sloping up and down. Advanced slope makes brightness changes smooth for eye. Dithering can be programmed with EEPROM bits <DITHER [1:0]> from 0 to 3 bits. Example below is for 1-bit dithering, e.g., for 3-bit dithering, every 8th pulse is made 1 LSB longer to increase the average value by 1/8 of LSB.



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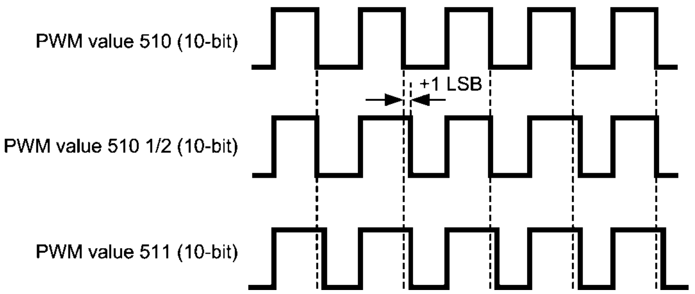
Sloper Operation



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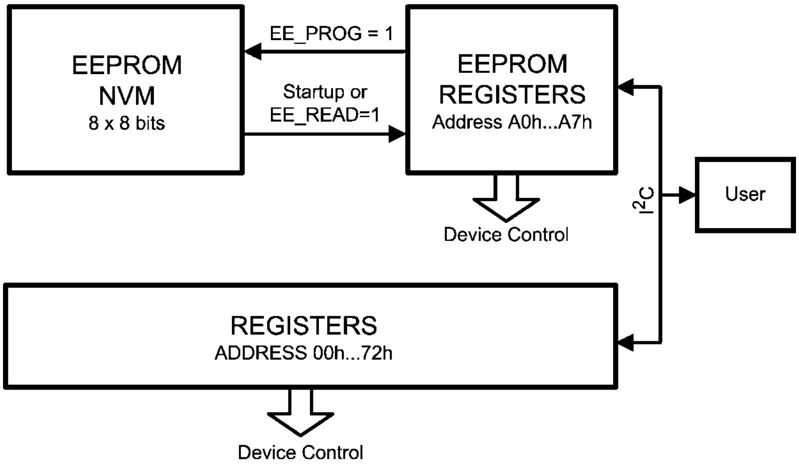
Example of the Dithering, 1-bit dither, 10-bit resolution

DRIVER HEADROOM CONTROL

Driver headroom can be controlled with <DRV_HEADR[2:0]> EEPROM bits. Driver headroom control sets the minimum threshold for the voltage over the LED output which has the smallest driver headroom and controls the boost output voltage accordingly. Boost output voltage step size is 125 mV. The LED output which has the smallest forward voltage is the one which has highest V_F across the LEDs. The strings with highest forward voltage is detected automatically. To achieve best possible efficiency smallest possible headroom voltage should be selected. If there is high variation between LED strings, the headroom can be raised slightly to prevent any visual artifacts.

EEPROM

EEPROM memory stores various parameters for chip control. The 64-bit EEPROM memory is organized as 8 x 8 bits. The EEPROM structure consists of a register front-end and the non-volatile memory (NVM). Register data can be read and written through the serial interface, and data will be effective immediately. To read and program NVM, separate commands need to be sent. Erase and program voltages are generated on-chip charge pump, no other voltages than normal input voltage are required. A complete EEPROM memory map is shown in the chapter LP8545 EEPROM Memory Map.



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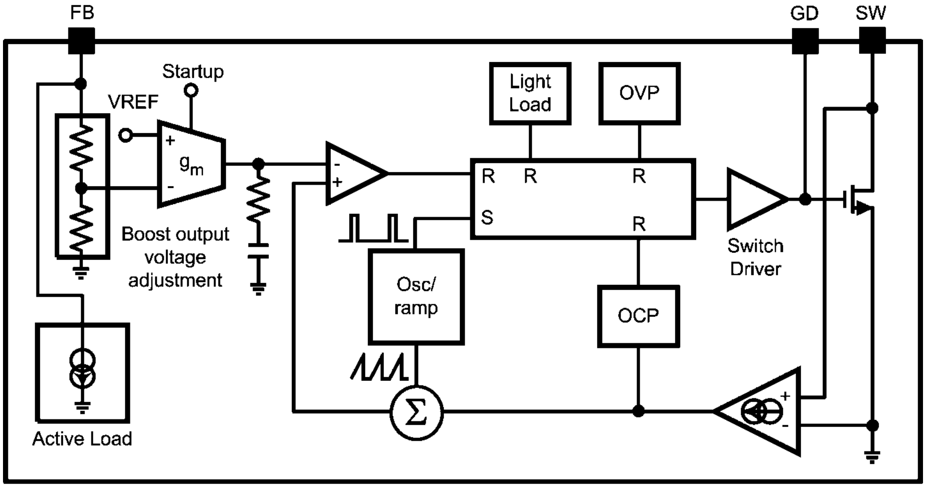
Boost Converter

OPERATION

The LP8545 boost DC/DC converter generates a 10…40V supply voltage for the LEDs from 2.7…22V input voltage. The output voltage can be controlled either with EEPROM register bits <VBOOST[4:0]> or automatic adaptive voltage control can be used. Higher output voltages can be achieved with external FET and by using resistor divider in the FB pin. GD pin operates as gate driver for the external FET in this case. To activate external FET gate driver, <EN_EXT_FET> bit in EEPROM register must be set to 1. The converter is a magnetic switching PWM mode DC/DC converter with a current limit. The topology of the magnetic boost converter is called CPM (current programmed mode) control, where the inductor current is measured and controlled with the feedback. Switching frequency is selectable between 156 kHz and 1.25 MHz with EEPROM bit <BOOST_FREQ[1:0]>. When <EN_BOOST> EEPROM register bit is set to 1, then boost will activate automatically when backlight is enabled.

In adaptive mode the boost output voltage is adjusted automatically based on LED driver headroom voltage. Boost output voltage control step size is, in this case, 125 mV to ensure as small as possible driver headroom and high efficiency. Enabling the adaptive mode is done with <EN_ADAPT> EEPROM bit. If boost is started with adaptive mode enabled, then the initial boost output voltage value is defined with the <VBOOST[4:0]> EEPROM register bits in order to eliminate long output voltage iteration time when boost is started for the first time. The following figure shows the boost topology with the protection circuitry:



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PROTECTION

Three different protection schemes are implemented:

1. Over-voltage protection, limits the maximum output voltage.
    - Over-voltage protection limit changes dynamically based on output voltage setting.
    - Keeps the output below breakdown voltage.
    - Prevents boost operation if battery voltage is much higher than desired output.
2. Over-current protection, limits the maximum inductor current.
3. Duty cycle limiting.

MANUAL OUTPUT VOLTAGE CONTROL

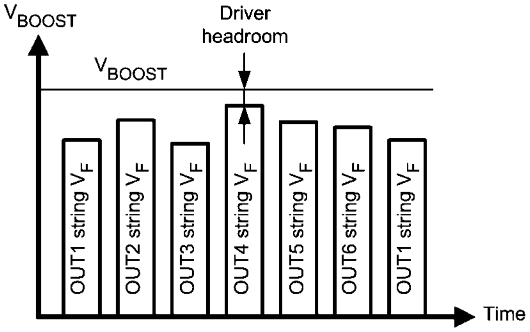
User can control the boost output voltage with <VBOOST[4:0] > EEPROM register bits when adaptive mode is disabled.

VBOOST[4:0]		**Voltage (typical)**
Bin	Dec	Volts
00000	0	10
00001	1	11
00010	2	12
00011	3	13
00100	4	14
...	...	...
11101	29	39
11110	30	40
11111	31	40

If resistor divider is used for the FB pin to get higher output voltage with external FET, the boost output voltages are scaled accordingly.

ADAPTIVE BOOST CONTROL

Adaptive boost control function adjusts the boost output voltage to the minimum sufficient voltage for proper LED driver operation. The output with highest V_F LED string is detected and boost output voltage adjusted accordingly. Driver headroom can be adjusted with <DRIVER_HEADR[2:0]> EEPROM bits from ~300 mV to 1200 mV. Boost adaptive control voltage step size is 125 mV. Boost adaptive control operates similarly with and without PSPWM.



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Boost Adaptive Control Principle with PSPWM

Fault Detection

LP8545 has fault detection for LED fault, low-battery voltage, over-current and thermal shutdown. The open drain output pin (FAULT) can be used to indicate occurred fault. The cause for the fault can be read from status register. Reading the fault register will also reset the fault. Setting the EN pin low will also reset the faults, even if an external 5V line is used to power VLDO pin.

LED FAULT DETECTION

With LED fault detection, the voltages across the LED drivers are constantly monitored. LED fault detection is enabled with <EN_LED_FAULT> EEPROM bit. Shorted or open LED string is detected.

If LED fault is detected:

- The corresponding LED string is taken out of boost adaptive control loop;
- Fault bits are set in the fault register to identify whether the fault has been open/short and how many strings are faulty; and
- Fault open-drain pin is pulled down.

LED fault sensitivity can be adjusted with <LED_FAULT_THR [1:0]> EEPROM bits which sets the allowable variation between LED output voltage from 2.3V to 5.3V. Depending on application and how much variation there can be in normal operation between LED string forward voltages this setting can be adjusted.

Fault is cleared by setting EN pin low or by reading the fault register.

UNDER-VOLTAGE DETECTION

LP8545 has detection for too-low VIN voltage. Threshold level for the voltage is set with EEPROM register bits as seen in the following table:

UVLO[1:0]	Threshold (V)
00	OFF
01	2.7V
10	5.7V
11	8.7V

When under voltage is detected the LED outputs and boost will shutdown, FAULT pin is pulled down and corresponding fault bit is set in fault register. LEDs and boost will start again when the voltage has increased above the threshold level. Hysteresis is implemented to threshold level to avoid continuous triggering of fault when threshold is reached.

Fault is cleared by setting EN pin low or by reading the fault register.

OVER-CURRENT PROTECTION

LP8545 has detection for too-high loading on the boost converter. When over-current fault is detected, the LP8545 will shut down.

Fault is cleared by setting EN pin low or by reading the fault register.

DEVICE THERMAL REGULATION

LP8545 has an internal temperature sensor which can be used to measure the junction temperature of the device and protect the device from overheating. During thermal regulation, LED PWM is reduced by 2% of full scale per °C whenever the temperature threshold is reached. Temperature regulation is enabled automatically when chip is enabled. 11-bit temperature value can be read from Temp MSB and Temp LSB registers, MSB should be read first. Temperature limit can be programmed in EEPROM as shown in the following table.

Thermal regulation function does not generate fault signal.

TEMP_LIM[1:0]	Over-Temp Limit (°C)
00	OFF
01	110
10	120
11	130

THERMAL SHUTDOWN

If the LP8545 reaches thermal shutdown temperature (150° C) the LED outputs and boost will shut down to protect it from damage. Also the fault pin will be pulled down to indicate the fault state. Device will activate again when temperature drops below 130°C degrees.

Fault is cleared by setting EN pin low or by reading the fault register.

I²C Compatible Serial Bus Interface

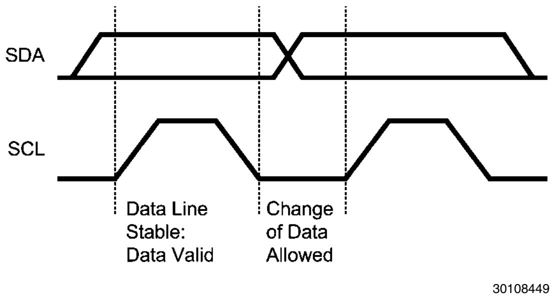
INTERFACE BUS OVERVIEW

The I²C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA) and the Serial Clock Line (SCLK). These lines should be connected to a positive supply, via a pull-up resistor and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the SCLK. The LP8545 is always a slave device.

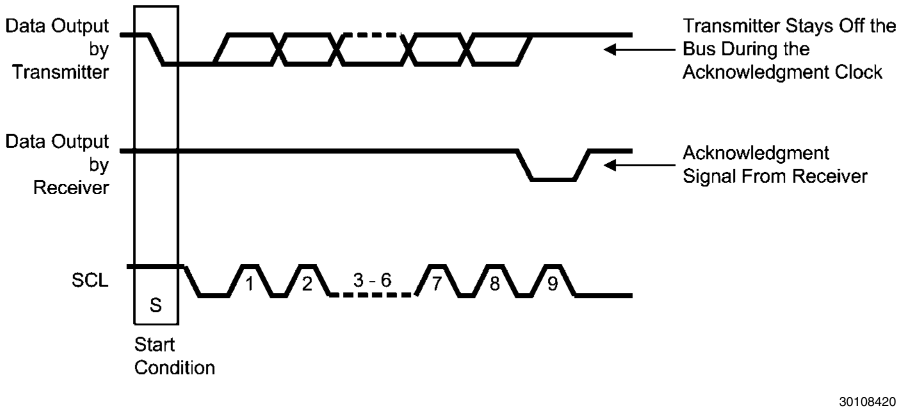
DATA TRANSACTIONS

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock SCLK. Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCLK and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCLK state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.



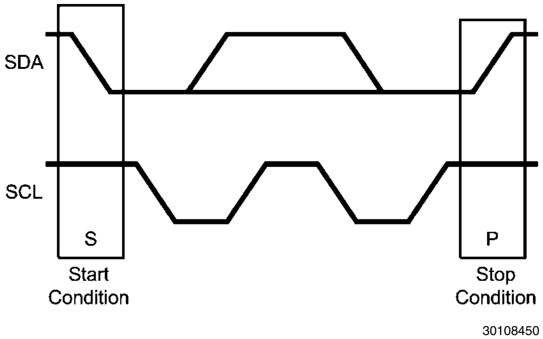
Bit Transfer

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.



Start and Stop

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCLK) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCLK is high indicates a Stop Condition.



Start and Stop Conditions

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

ACKNOWLEDGE CYCLE

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

"ACKNOWLEDGE AFTER EVERY BYTE" RULE

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the "acknowledge after every byte" rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging ("negative acknowledge") the last byte clocked out of the slave. This "negative acknowledge" still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

ADDRESSING TRANSFER FORMATS

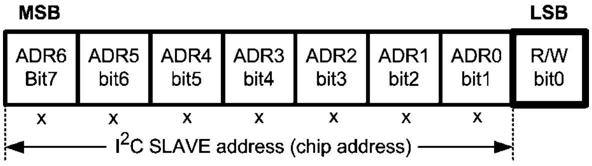
Each device on the bus has a unique slave address. The LP8545 operates as a slave device with 7-bit address combined with data direction bit. Slave address is 2Ch as 7-bit or 58h for write and 59h for read in 8-bit format.

Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.

I^{2}C Chip Address



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Control Register Write Cycle

- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes the control register address will be incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

Control Register Read Cycle

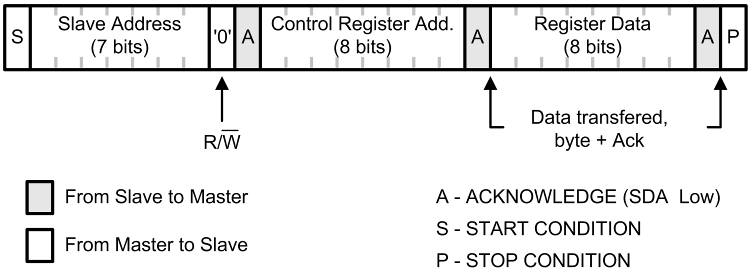
- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = 1).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

Data Read and Write Cycles

	Address Mode
Data Read	<Start Condition> <Slave Address><r/w = 0>[Ack] <Register Addr.>[Ack] <Repeated Start Condition> <Slave Address><r/w = 1>[Ack] [Register Data]<Ack or NAck> … additional reads from subsequent register address possible <Stop Condition>
Data Write	<Start Condition> <Slave Address><r/w='0'>[Ack] <Register Addr.>[Ack] <Register Data>[Ack] … additional writes to subsequent register address possible <Stop Condition>

<>Data from master [ ] Data from slave

Register Read and Write Detail



Register Write Format

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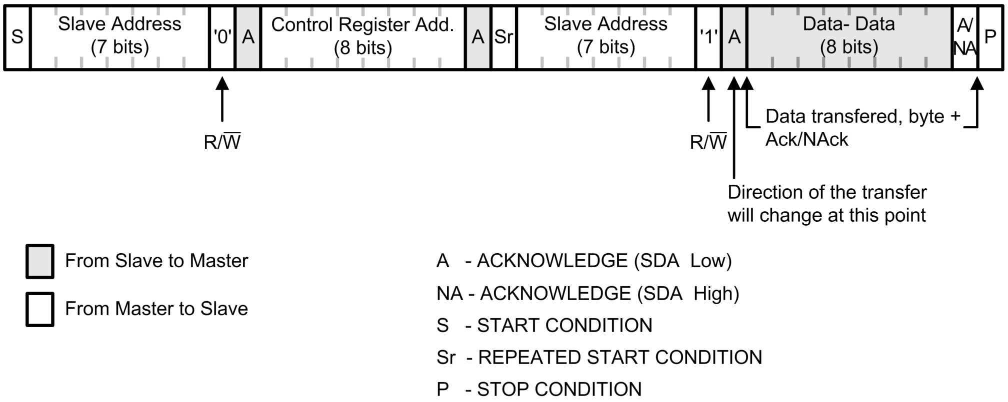

Register Read Format

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Recommended External Components

INDUCTOR SELECTION

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. Shielded inductors radiate less noise and should be preferred.

The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current.

The equation below shows the worst case conditions.

$$I_{SAT} > \frac{I_{OUTMAX}}{D'} + I_{RIPPLE}$$

$$\text{Where } I_{RIPPLE} = \frac{(V_{OUT} - V_{IN})}{(2 \times L \times f)} \times \frac{V_{IN}}{V_{OUT}}$$

$$\text{Where } D = \frac{(V_{OUT} - V_{IN})}{(V_{OUT})} \text{ and } D' = (1 - D)$$

- I_{RIPPLE}: Average to peak inductor current
- I_{OUTMAX}: Maximum load current
- V_{IN}: Maximum input voltage in application
- L: Min inductor value including worst case tolerances
- f: Minimum switching frequency
- D: Duty cycle for CCM Operation
- V_{OUT}: Output voltage

Example using above equations:

- V_{IN} = 12V
- V_{OUT} = 38V
- I_{OUT} = 400 mA
- L = 15 µH – 20% = 12 µH
- f = 1.25 MHz
- I_{SAT} = 1.6A

As a result the inductor should be selected according to the I_{SAT}. A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit of 2.5A. A 15 µH inductor with a saturation current rating of 2.5A is recommended for most applications. The inductor's resistance should be less than 300 mΩ for good efficiency. For high efficiency choose an inductor with high frequency core material such as ferrite to reduce core losses. To minimize radiated noise, use shielded core inductor. Inductor should be placed as close to the SW pin and the IC as possible. Special care should be used when designing the PCB layout to minimize radiated noise and to get good performance from the boost converter.

OUTPUT CAPACITOR

A ceramic capacitor with 50V voltage rating or higher is recommended for the output capacitor. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. For light loads a 4.7 µF capacitor is sufficient. Effectively the capacitance should be 4 µF for < 150 mA loads. For maximum output voltage/current 10 µF capacitor (or two 4.7 µF capacitors) is recommended to minimize the output ripple. For high output voltage (55V) application 100V voltage rating capacitors should be used. 2 x 2.2 µF capacitors are enough.

LDO CAPACITOR

A 1µF ceramic capacitor with 10V voltage rating is recommended for the LDO capacitor.

OUTPUT DIODE

A Schottky diode should be used for the output diode. Peak repetitive current should be greater than inductor peak current (2.5A) to ensure reliable operation. Average current rating should be greater than the maximum output current. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown voltage of the Schottky diode significantly larger (~60V) than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

BOOST CONVERTER TRANSISTOR

FET transistor with high enough voltage rating (VDS at least 60V) should be used. Current rating for the FET should be the same as inductor peak current (2.5A with highest programmed inductor current). Gate drive voltage for the FET is 5V.

RESISTOR DIVIDER FOR THE BOOST FEEDBACK

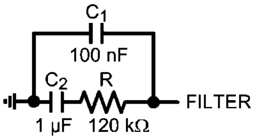
Recommended values for feedback resistor divider to get 55V boost output voltage are R_1 = 63.4 kΩ and R_2 = 59 kΩ. Resistor values can be fine tuned to get desired maximum boost output voltage based on how many LEDs are driven in series and what are the forward voltage specifications for the LEDs. Voltage on FB pin must not exceed 40V any time.

RESISTORS FOR SETTING THE LED CURRENT AND PWM FREQUENCY

See EEPROM register description on how to select values for these resistors

FILTER COMPONENT VALUES

Optimal components for 60 Hz V_{SYNC} frequency and 4 Hz cut-off frequency of the low-pass filter are shown in the typical application diagrams and in the figure below. If 2 Hz cut-off frequency i.e. slower response time is desired, filter components are: C_1 = 1 µF, C_2 = 10 µF and R = 47 kΩ. If different V_{SYNC} frequency or response time is desired, please contact National Semiconductor representative for guidance.



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Register Map

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00H	Brightness Control	BRT[7:0]								0000 0000
01H	Device Control						BRT_MODE[1:0]		BL_CTL	0000 0000
02H	Fault	OPEN	SHORT	2_CHANNELS	1_CHANNEL	BL_FAULT	OCP	TSD	UVLO	0000 0000
03H	ID	PANEL	MFG[3:0]				REV[2:0]			1111 1100
04H	Direct Control			OUT[6:1]						0000 0000
05H	Temp MSB	TEMP[10:3]								0000 0000
06H	Temp LSB	TEMP[2:0]								0000 0000
72H	EEPROM_control	EE_READY					EE_INIT	EE_PROG	EE_READ	0000 0000

EEPROM Memory Map

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
A0H	eeprom addr 0	CURRENT[7:0]							
A1H	eeprom addr 1	BOOST_FREQ[1:0]		EN_LED_FAULT	TEMP_LIM[1:0]		SLOPE[2:0]		
A2H	eeprom addr 2	ADAPTIVE_SPEED[1:0]		ADV_SLOPE	EN_EXT_FET	EN_ADAPT	EN_BOOST	BOOST_MAX[1:0]	
A3H	eeprom addr 3	UVLO[1:0]		EN_PSPWM	PWM_FREQ[4:0]				
A4H	eeprom addr 4	PWM_RESOLUTION[1:0]		EN_I_RES	LED_FAULT_THR[1:0]		DRV_HEADR[2:0]		
A5H	eeprom addr 5	EN_VSYNC	DITHER[1:0]		VBOOST[4:0]				
A6H	eeprom addr 6	PLL[12:5]							
A7H	eeprom addr 7	PLL[4:0]					EN_F_RES	HYSTERESIS[1:0]	

Register Bit Explanations

BRIGHTNESS CONTROL

Address 00h

Reset value 0000 0000b

Brightness Control register

7	6	5	4	3	2	1	0
BRT[7:0]							

Name	Bit	Access	Description
BRT	7:0	R/W	Backlight PWM 8-bit linear control.

DEVICE CONTROL

Address 01h

Reset value 0000 0000b

Device Control register

7	6	5	4	3	2	1	0
					BRT_MODE[1:0]		BL_CTL

Name	Bit	Access	Description
BRT_MODE	2:1	R/W	PWM source mode 00b = PWM input pin duty cycle control (default) 01b = PWM input pin duty cycle control 10b = Brightness register 11b = Direct PWM control from PWM input pin
BL_CTL	0	R/W	Enable backlight 0 = Backlight disabled and chip turned off if BRT_MODE[1:0] = 10. In external PWM pin control the state of the chip is defined with the PWM pin and this bit has no effect. 1 = Backlight enabled and chip turned on if BRT_MODE[1:0] = 10. In external PWM pin control the state of the chip is defined with the PWM pin and this bit has no effect.

FAULT

Address 02h

Reset value 0000 0000b

Fault register

7	6	5	4	3	2	1	0
OPEN	SHORT	2_CHANNELS	1_CHANNEL	BL_FAULT	OCP	TSD	UVLO

Name	Bit	Access	Description
OPEN	7	R	LED open fault detection 0 = No fault 1 = LED open fault detected. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.
SHORT	6	R	LED short fault detection 0 = No fault 1 = LED short fault detected. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.

Fault register			
2_CHANNELS	5	R	LED fault detection 0 = No fault 1 = 2 or more channels have generated either short or open fault. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.
1_CHANNEL	4	R	LED fault detection 0 = No fault 1 = 1 channel has generated either short or open fault. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.
BL_FAULT	3	R	LED fault detection 0 = No fault 1 = LED fault detected. Generated with OR function of all LED faults. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.
OCP	2	R	Over current protection 0 = No fault 1 = Over current detected in boost output. OCP detection block monitors the boost output and if the boost output has been too low for more than 50 ms it will generate OCP fault and disable the boost. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low. After clearing the fault boost will startup again.
TSD	1	R	Thermal shutdown 0 = No fault 1 = Thermal fault generated, 150°C reached. Boost converted and LED outputs will be disabled until the temperature has dropped down to 130°C. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.
UVLO	0	R	Under voltage detection 0 = No fault 1 = Under voltage detected in VIN pin. Boost converted and LED outputs will be disabled until V_{IN} voltage is above the threshold voltage. Threshold voltage is set with EEPROM bits from 3V...9V. Fault pin is pulled to GND. Fault is cleared by reading the register 02h or setting EN pin low.

IDENTIFICATION

Address 03h

Reset value 1111 1100b

Identification register							
7	6	5	4	3	2	1	0
PANEL	MFG[3:0]				REV[2:0]		

Name	Bit	Access	Description
PANEL	7	R	Panel ID code
MFG	6:3	R	Manufacturer ID code
REV	2:0	R	Revision ID code

DIRECT CONTROL

Address 04h

Reset value 0000 0000b

Direct Control register							
7	6	5	4	3	2	1	0
		OUT[6:1]					
Name	Bit	Access	Description				
OUT	5:0	R/W	Direct control of the LED outputs 0 = Normal operation. LED output are controlled with PWM. 1 = LED output is forced to 100% PWM.				

TEMP MSB

Address 05h

Reset value 0000 0000b

Temp MSB register							
7	6	5	4	3	2	1	0
TEMP[10:3]							
Name	Bit	Access	Description				
TEMP	7:0	R	Device internal temperature sensor reading first 8 MSB. MSB must be read before LSB, because reading of MSB register latches the data.				

TEMP LSB

Address 06h

Reset value 0000 0000b

Temp LSB register							
7	6	5	4	3	2	1	0
TEMP[2:0]							
Name	Bit	Access	Description				
TEMP	7:5	R	Device internal temperature sensor reading last 3 LSB. MSB must be read before LSB, because reading of MSB register latches the data.				

EEPROM CONTROL

Address 72h

Reset value 0000 0000b

EEPROM Control register							
7	6	5	4	3	2	1	0
EE_READY					EE_INIT	EE_PROG	EE_READ

Name	Bit	Access	Description
EE_READY	7	R	EEPROM ready 0 = EEPROM programming or read in progress 1 = EEPROM ready, not busy
EE_INIT	2	R/W	EEPROM initialization bit. This bit must be written 1 before EEPROM read or programming.
EE_PROG	1	R/W	EEPROM programming. 0 = Normal operation 1 = Start the EEPROM programming sequence. EE_INIT must be written 1 before EEPROM programming can be started. Programs data currently in the EEPROM registers to non volatile memory (NVM). Programming sequence takes about 200 ms. Programming voltage is generated inside the chip.
EE_READ	0	R/W	EEPROM read 0 = Normal operation 1 = Reads the data from NVM to the EEPROM registers. Can be used to restore default values if EEPROM registers are changed during testing.

Programming sequence (program data permanently from registers to NVM):

1. Turn on the chip by writing BL_CTL bit to 1 and BRT_MODE[1:0] to 10b (05h to address 01h)
2. Write data to EEPROM registers (address A0h…A7h).
3. Write EE_INIT to 1 in address 72h. (04h to address 72h).
4. Write EE_PROG to 1 and EE_INIT to 0 in address 72h. (02h to address 72h).
5. Wait 200 ms.
6. Write EE_PROG to 0 in address 72h. (00h to address 72h).

Read sequence (load data from NVM to registers):

1. Turn on the chip by writing BL_CTL bit to 1 and BRT_MODE[1:0] to 10b (05h to address 01h).
2. Write EE_INIT to 1 in address 72h. (04h to address 72h).
3. Write EE_READ to 1 and EE_INIT to 0 in address 72h. (01h to address 72h).
4. Wait 200 ms.
5. Write EE_READ to 0 in address 72h. (00h to address 72h).

Note: Data written to EEPROM registers is effective immediately even if the EEPROM programming sequence has not been done. When power is turned off, the device will however lose the data if it is not programmed to the NVM. During startup device automatically loads the data from NVM to registers.

EEPROM Bit Explanations

EEPROM Default Values

ADDR	LP8545SQX
A0H	0111 1111
A1H	1011 0101
A2H	1010 1111
A3H	0111 1011
A4H	0010 1000
A5H	1100 1111
A6H	0110 0100
A7H	0010 1101

EEPROM ADDRESS 0

Address A0h

EEPROM ADDRESS 0 register							
7	6	5	4	3	2	1	0
CURRENT[7:0]							

Name	Bit	Access	Description		
CURRENT	7:0	R/W	Backlight current adjustment. If EN_I_RES = 0 the maximum backlight current is defined only with these bits as described below. If EN_I_RES = 1, then the external resistor connected to ISET pin also scales the LED current. With 16 kΩ resistor and CURRENT set to 7FH the output current is then 23 mA.		
				EN_I_RES = 0	EN_I_RES = 1
			0000 0000	0 mA	0 mA
			0000 0001	0.12 mA	(1/255) x 600 x 1.23V/R_{ISET}
			0000 0010	0.24 mA	(2/255) x 600 x 1.23V/R_{ISET}
			...	...	...
			0111 1111 (default)	**15.00 mA**	**(127/255) x 600 x 1.23V/R_{ISET}**
			...	...	...
			1111 1101	29.76 mA	(253/255) x 600 x 1.23V/R_{ISET}
			1111 1110	29.88 mA	(254/255) x 600 x 1.23V/R_{ISET}
			1111 1111	30.00 mA	(255/255) x 600 x 1.23V/R_{ISET}

EEPROM ADDRESS 1

Address A1h

EEPROM ADDRESS 1 register							
7	6	5	4	3	2	1	0
BOOST_FREQ[1:0]		EN_LED_FAULT	TEMP_LIM[1:0]		SLOPE[2:0]		

Name	Bit	Access	Description
BOOST_FREQ	7:6	R/W	Boost Converter Switch Frequency 00 = 156 kHz 01 = 312 kHz 10 = 625 kHz 11 = 1250 kHz

EEPROM ADDRESS 1 register			
EN_LED_FAULT	5	R/W	Enable LED fault detection 0 = LED fault detection disabled 1 = LED fault detection enabled
TEMP_LIM	4:3	R/W	Thermal deration function temperature threshold 00 = thermal deration function disabled 01 = 110°C 10 = 120°C 11 = 130°C
SLOPE	2:0	R/W	Slope time for brightness change 000 = Slope function disabled, immediate brightness change 001 = 50 ms 010 = 75 ms 011 = 100 ms 100 = 150 ms 101 = 200 ms 110 = 300 ms 111 = 500 ms

EEPROM ADDRESS 2

Address A2h

<table>
<tr><th colspan="8">EEPROM ADDRESS 2 register</th></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">ADAPTIVE_SPEED[1:0]</td><td>ADV_SLOPE</td><td>EN_EXT_FET</td><td>EN_ADAPT</td><td>EN_BOOST</td><td colspan="2">BOOST_IMAX[1:0]</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td>Name</td><td>Bit</td><td>Access</td><td colspan="5">Description</td></tr>
<tr><td>ADAPTIVE SPEED[1]</td><td>7</td><td>R/W</td><td colspan="5">Boost converter adaptive control speed adjustment
0 = Normal mode
1 = Adaptive mode optimized for light loads. Activating this helps the voltage droop with light loads during boost / backlight startup.</td></tr>
<tr><td>ADAPTIVE SPEED[0]</td><td>6</td><td>R/W</td><td colspan="5">Boost converter adaptive control speed adjustment
0 = Adjust boost once for each phase shift cycle or normal PWM cycle
1 = Adjust boost every 16th phase shift cycle or normal PWM cycle</td></tr>
<tr><td>ADV_SLOPE</td><td>5</td><td>R/W</td><td colspan="5">Advanced slope
0 = Advanced slope is disabled
1 = Use advanced slope for brightness change to make brightness changes smooth for eye</td></tr>
<tr><td>EN_EXT_FET</td><td>4</td><td>R/W</td><td colspan="5">Enable external FET gate driver
0 = Internal FET used
1 = External FET used and GD pin used for driving the external FET gate</td></tr>
<tr><td>EN_ADAPT</td><td>3</td><td>R/W</td><td colspan="5">Enable boost converter adaptive mode
0 = adaptive mode disabled, boost converter output voltage is set with VBOOST EEPROM register bits
1 = adaptive mode enabled. Boost converter startup voltage is set with VBOOST EEPROM register bits, and after startup voltage is reached the boost converter will adapt to the highest LED string V_F. LED driver output headroom is set with DRV_HEADR EEPROM control bits.</td></tr>
<tr><td>EN_BOOST</td><td>2</td><td>R/W</td><td colspan="5">Enable boost converter
0 = boost is disabled
1 = boost is enabled and will turn on automatically when backlight is enabled</td></tr>
</table>

EEPROM ADDRESS 2 register			
BOOST_IMAX	1:0	R/W	Boost converter inductor maximum current 00 = 0.9A 01 = 1.4A 10 = 2.0A 11 = 2.5A (recommended)

EEPROM ADDRESS 3

Address A3h

EEPROM ADDRESS 3 register							
7	6	5	4	3	2	1	0
UVLO[1:0]		EN_PSPWM	PWM_FREQ[4:0]				

Name	Bit	Access	Description
UVLO	7:6	R/W	00 = Disabled 01 = 2.7V 10 = 6V 11 = 9V
EN_PSPWM	5	R/W	Enable phase shift PWM scheme 0 = phase shift PWM disabled, normal PWM mode used 1 = phase shift PWM enabled
PWM_FREQ	4:0	R/W	PWM output frequency setting. See pg. 15 for full description of selectable PWM frequencies.

EEPROM ADDRESS 4

Address A4h

EEPROM ADDRESS 4 register							
7	6	5	4	3	2	1	0
PWM_RESOLUTION[1:0]		EN_I_RES	LED_FAULT_THR[1:0]		DRV_HEADR[2:0]		

Name	Bit	Access	Description
PWM RESOLUTION	7:6	R/W	PWM output resolution selection. Actual resolution depends also on the output frequency. See pg. 15 for full description. 00 = 8...10 bits (19.2 kHz...4.8 kHz) 01 = 9...11 bits (19.2 kHz... 4.8 kHz) 10 = 10...12 bits (19.2 kHz...4.8 kHz) 11 = 11...13 bits (19.2 kHz...4.8 kHz)
EN_I_RES	5	R/W	Enable LED current set resistor 0 = Resistor is disabled and current is set only with CURRENT EEPROM register bits 1 = Enable LED current set resistor. LED current is defined by the R_{ISET} resistor and the CURRENT EEPROM register bits.
LED_FAULT_THR	4:3	R/W	LED fault detector thresholds. V_{SAT} is the saturation voltage of the driver, typically 200 mV. 00 = 2.3V 01 = 3.3V 10 = 4.3V 11 = 5.3V

EEPROM ADDRESS 4 register			
DRV_HEADR	2:0	R/W	LED output driver headroom control. V_{SAT} is the saturation voltage of the driver, typically 200 mV. 000 = V_{SAT} + 125 mV 001 = V_{SAT} + 250 mV 010 = V_{SAT} + 375 mV 011 = V_{SAT} + 500 mV 100 = V_{SAT} + 625 mV 101 = V_{SAT} + 750 mV 110 = V_{SAT} + 875 mV 111 = V_{SAT} + 1000 mV

EEPROM ADDRESS 5

Address A5h

EEPROM ADDRESS 5 register							
7	6	5	4	3	2	1	0
EN_VSYNC	DITHER[1:0]		VBOOST[4:0]				
Name	Bit	Access	Description				
EN_VSYNC	7	R/W	Enable V_{SYNC} function 0 = V_{SYNC} input disabled 1 = V_{SYNC} input enabled. V_{SYNC} signal is used by the internal PLL to generate PWM output and boost frequency.				
DITHER	6:5	R/W	Dither function controls 00 = Dither function disabled 01 = 1-bit dither used for output PWM transitions 10 = 2-bit dither used for output PWM transitions 11 = 3-bit dither used for output PWM transitions				
VBOOST	4:0	R/W	Boost voltage control from 10V to 40V with 1V step (without FB resistor divider). If adaptive boost control is enabled, this sets the initial start voltage for the boost converter. If adaptive mode is disabled, this will directly set the output voltage of the boost converter. 0 0000 = 10V 0 0001 = 11V 0 0010 = 12V ... 1 1101 = 39V 1 1110 = 40V 1 1111 = 40V				

EEPROM ADDRESS 6

Address A6h

EEPROM ADDRESS 6 register							
7	6	5	4	3	2	1	0
PLL[12:5]							

Name	Bit	Access	Description
PLL	7:0	R/W	13-bit counter value for PLL, 8 MSB bits. PLL[12:0] bits are used when en_vsync = 1. See table below for PLL value calculation.

EEPROM ADDRESS 7

Address A7h

EEPROM ADDRESS 7 register							
7	6	5	4	3	2	1	0
PLL[4:0]					EN_F_RES	HYSTERESIS[1:0]	

Name	Bit	Access	Description
PLL	7:3	R/W	13-bit counter value for PLL, 5 LSB bits. PLL[12:0] bits are used when en_vsync = 1. See table below for PLL value calculation.
EN_F_RES	2	R/W	Enable PWM output frequency set resistor 0 = Resistor is disabled and PWM output frequency is set with PWM_FREQ EEPROM register bits 1 = PWM frequency set resistor is enabled. R_{FSET} defines the output PWM frequency. See pg. 15 for full description of the PWM frequencies.
HYSTERESIS	1:0	R/W	PWM input hysteresis function. Will define how small changes in the PWM input are ignored to remove constant switching between two values. 00 = OFF 01 = 1-bit hysteresis with 11-bit resolution 10 = 1-bit hysteresis with 10-bit resolution 11 = 1-bit hysteresis with 8-bit resolution

PLL value calculation

en_vsync	PLL frequency [MHz]	PLL[12:0]
0	5, 10, 20, 40	not used
1	5	5 MHz / (26 x f_{VSYNC})
	10	10 MHz / (50 x f_{VSYNC})
	20	20 MHz / (98 x f_{VSYNC})
	40	40 MHz / (196 x f_{VSYNC})

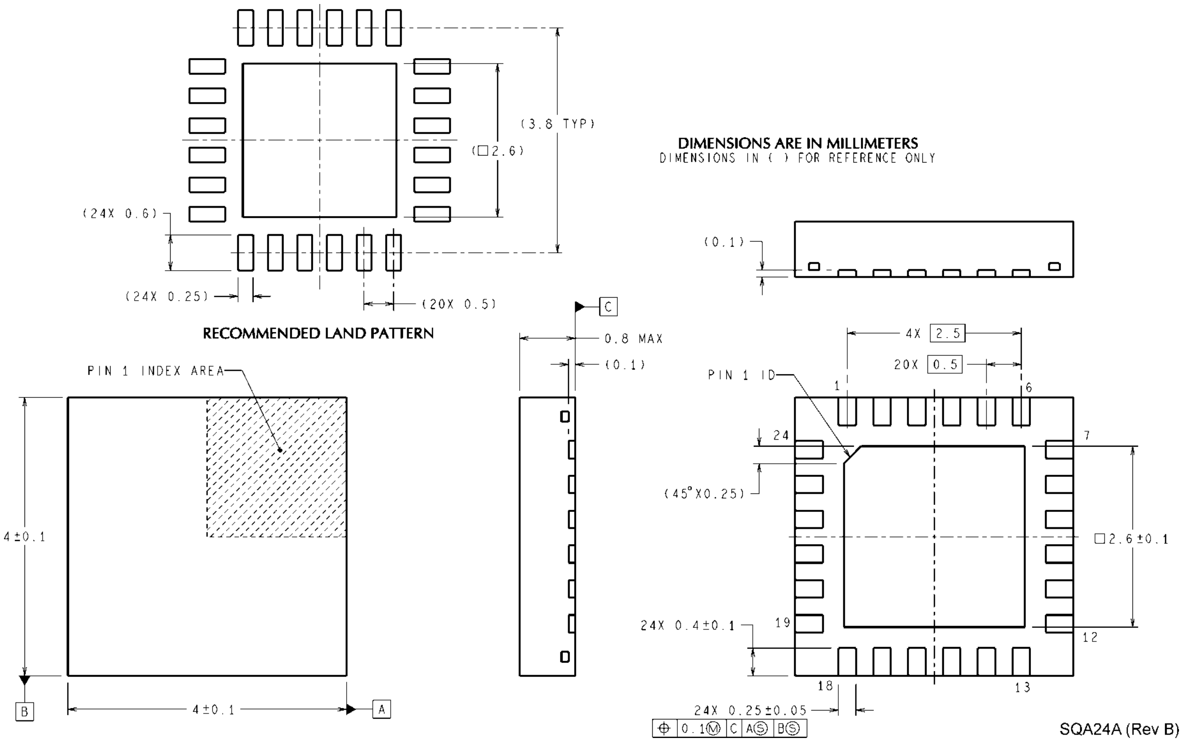
PLL frequency is set by PWM_RESOLUTION[1:0] bits.

For Example:

If f_{PLL} = 5 MHz and f_{VSYNC} = 60 Hz, then PLL[12:0] = 5000000 Hz / (26 * 60 Hz) = 3205d = C85h.

If f_{PLL} = 10 MHz and f_{VSYNC} = 75 Hz, then PLL[12:0] = 10000000 Hz / (50 * 75 Hz) = 2667d = A6Bh.

Physical Dimensions inches (millimeters) unless otherwise noted



SQA24A (Rev B)

SQA24A: LLP-24, 0.5mm pitch, no pullback

Notes

Notes

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