

30V P-Channel Enhancement-Mode MOSFET

$V_{DS} = -30V$

$R_{DS(ON)}, V_{GS@-10V}, I_{ds@-5.3A} = 70m\Omega$

$R_{DS(ON)}, V_{GS@-4.5V}, I_{ds@-4.2A} = 100m\Omega$

Features

Advanced trench process technology

High Density Cell Design For Ultra Low On-Resistance

Improved Shoot-Through FOM

S- Prefix for Automotive and Other Applications Requiring

Unique Site and Control Change Requirements; AEC-Q101

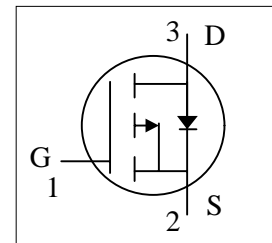
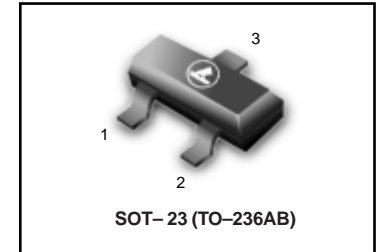
Qualified and PPAP Capable.

▼ Simple Drive Requirement

▼ Small Package Outline

▼ Surface Mount Device

LP9435LT1G
S-LP9435LT1G



Ordering Information

Device	Marking	Shipping
LP9435LT1G S-LP9435LT1G	P94	3000/Tape&Reel
LP9435LT3G S-LP9435LT3G	P94	10000/Tape&Reel

Maximum Ratings and Thermal Characteristics ($T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit	
V_{DS}	Drain-Source Voltage	-30	V	
V_{GS}	Gate-Source Voltage	± 20		
I_D	Continuous Drain Current	-5.3	A	
I_{DM}	Pulsed Drain Current ¹⁾	-20		
P_D	Maximum Power Dissipation	$T_A = 25^\circ C$	1.4	W
		$T_A = 75^\circ C$	0.8	
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ C$	
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	50	$^\circ C/W$	
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance (PCB mounted) ²⁾	90		

Note: 1. Repetitive Rating: Pulse width limited by the maximum junction temperature

2. 1-in² 2oz Cu PCB board

3. Guaranteed by design; not subject to production testing

LP9435LT1G , S-LP9435LT1G

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Static						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
$R_{DS(on)}$	Drain-Source On-State Resistance	$V_{GS} = -4.5V, I_D = -4.2A$		70.0	100.0	m Ω
$R_{DS(on)}$	Drain-Source On-State Resistance	$V_{GS} = -10V, I_D = -5.3A$		50.0	70.0	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1	-1.7	-3	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24V, V_{GS} = 0V$			1	μA
I_{GSS}	Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$			± 100	nA
g_{fs}	Forward Transconductance	$V_{DS} = -10V, I_D = -5.3A$		10		S
Dynamic³⁾						
Q_g	Total Gate Charge	$V_{DS} = -15V, I_D = -5.3A$ $V_{GS} = -10V$		28		nC
Q_{gs}	Gate-Source Charge			3		
Q_{gd}	Gate-Drain Charge			7		
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15V, R_L = 15\Omega$ $I_D = -1A, V_{GEN} = -10V$ $R_G = 6$		9		ns
t_r	Turn-On Rise Time			15		
$t_{d(off)}$	Turn-Off Delay Time			75		
t_f	Turn-Off Fall Time			40		
C_{iss}	Input Capacitance	$V_{DS} = -15V, V_{GS} = 0V$ $f = 1.0\text{ MHz}$		745		pF
C_{oss}	Output Capacitance			440		
C_{rss}	Reverse Transfer Capacitance			120		
Source-Drain Diode						
I_S	Max. Diode Forward Current				-2.6	A
V_{SD}	Diode Forward Voltage	$I_S = -2.6A, V_{GS} = 0V$			-1.3	V

Note Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

LP9435LT1G , S-LP9435LT1G

TYPICAL ELECTRICAL CHARACTERISTICS

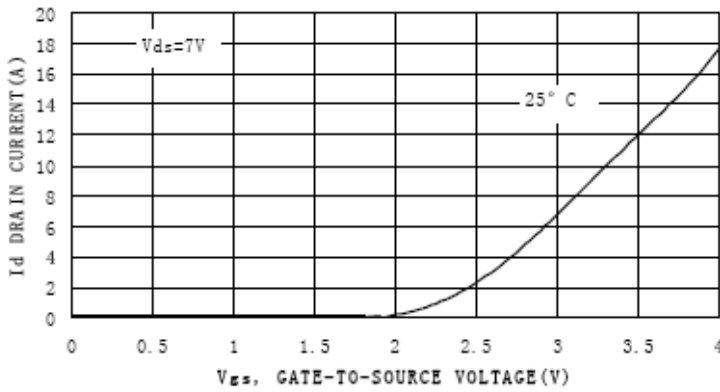


Figure 1. Transfer Characteristics

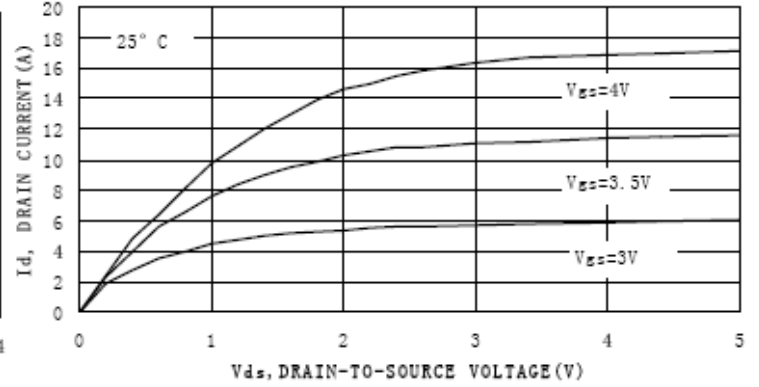


Figure 2. On-Region Characteristics

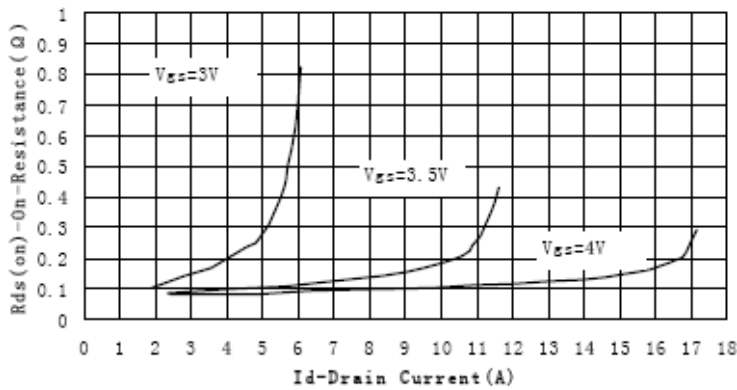


Figure 3. On-Resistance versus Drain Current

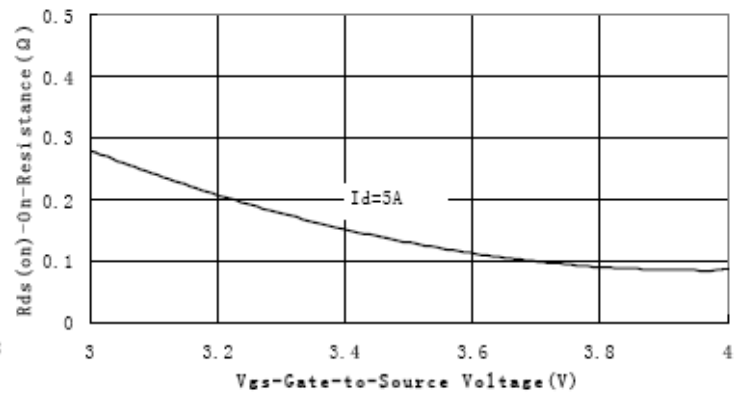


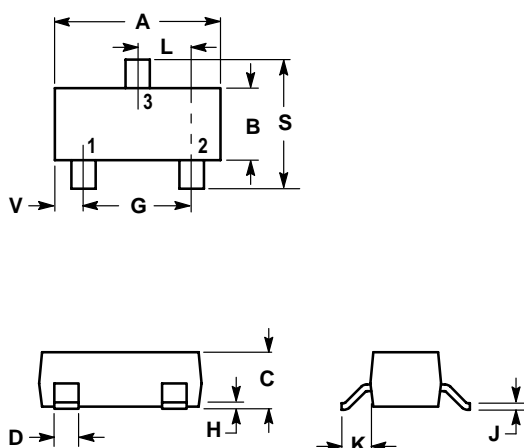
Figure 4. On-Resistance vs. Gate-to-Source Voltage

LP9435LT1G , S-LP9435LT1G

SOT-23

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M,1982
2. CONTROLLING DIMENSION: INCH.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

