



# LPC2142/2148

Single-chip 16/32-bit microcontrollers; 64/512 kB flash with ISP/IAP, USB 2.0 full-speed device, 10-bit ADC and DAC

Rev. 01 — 22 June 2005

Preliminary data sheet

## 1. General description

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The LPC2142/2148 microcontrollers are based on a 32/16-bit ARM7TDMI-S CPU with real-time emulation and embedded trace support, that combines the microcontroller with 64 kB and 512 kB of embedded high-speed flash memory. A 128-bit wide memory interface and a unique accelerator architecture enable 32-bit code execution at the maximum clock rate. For critical code size applications, the alternative 16-bit Thumb mode reduces code by more than 30 % with minimal performance penalty.

Due to their tiny size and low power consumption, LPC2142/2148 are ideal for applications where miniaturization is a key requirement, such as access control and point-of-sale. A blend of serial communications interfaces ranging from a USB 2.0 Full-speed device, multiple UARTs, SPI, SSP to I<sup>2</sup>C-bus and on-chip SRAM of 16 kB/40 kB, make these devices very well suited for communication gateways and protocol converters, soft modems, voice recognition and low end imaging, providing both large buffer size and high processing power. Various 32-bit timers, single or dual 10-bit ADC(s), 10-bit DAC, PWM channels and 45 fast GPIO lines with up to nine edge or level sensitive external interrupt pins make these microcontrollers particularly suitable for industrial control and medical systems.

## 2. Features

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### 2.1 Key features

- 16/32-bit ARM7TDMI-S microcontroller in a tiny LQFP64 package.
- 16 kB/40 kB of on-chip static RAM and 64 kB/512 kB of on-chip flash program memory.
  - 128-bit wide interface/accelerator enables high-speed 60 MHz operation.
- In-System Programming/In-Application Programming (ISP/IAP) via on-chip boot-loader software. Single flash sector or full chip erase in 400 ms and programming of 256 bytes in 1 ms.
- EmbeddedICE RT and Embedded Trace interfaces offer real-time debugging with the on-chip RealMonitor software and high-speed tracing of instruction execution.
- USB 2.0 Full-speed compliant device controller with 2 kB of endpoint RAM.
  - In addition, the LPC2148 provides 8 kB of on-chip RAM accessible to USB by DMA.
- One or two (LPC2142/48) 10-bit ADCs provide a total of 6/14 analog inputs, with conversion times as low as 2.44  $\mu$ s per channel.
- Single 10-bit DAC provides variable analog output.
- Two 32-bit timers/external event counters (with four capture and four compare channels each), PWM unit (six outputs) and watchdog.

- Low power Real-Time Clock (RTC) with independent power and dedicated 32 kHz clock input.
- Multiple serial interfaces including two UARTs (16C550), two Fast I<sup>2</sup>C-bus (400 kbit/s), SPI and SSP with buffering and variable data length capabilities.
- Vectored Interrupt Controller (VIC) with configurable priorities and vector addresses.
- Up to 45 of 5 V tolerant fast general purpose I/O pins in a tiny LQFP64 package.
- Up to nine edge or level sensitive external interrupt pins available.
- 60 MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100  $\mu$ s.
- On-chip integrated oscillator operates with an external crystal in range from 1 MHz to 30 MHz and with an external oscillator up to 50 MHz.
- Power saving modes include Idle and Power-down.
- Individual enable/disable of peripheral functions as well as peripheral clock scaling for additional power optimization.
- Processor wake-up from Power-down mode via external interrupt or BOD.
- Single power supply chip with POR and BOD circuits:
  - ◆ CPU operating voltage range of 3.0 V to 3.6 V (3.3 V  $\pm$  10 %) with 5 V tolerant I/O pads.

### 3. Ordering information

Table 1: Ordering information

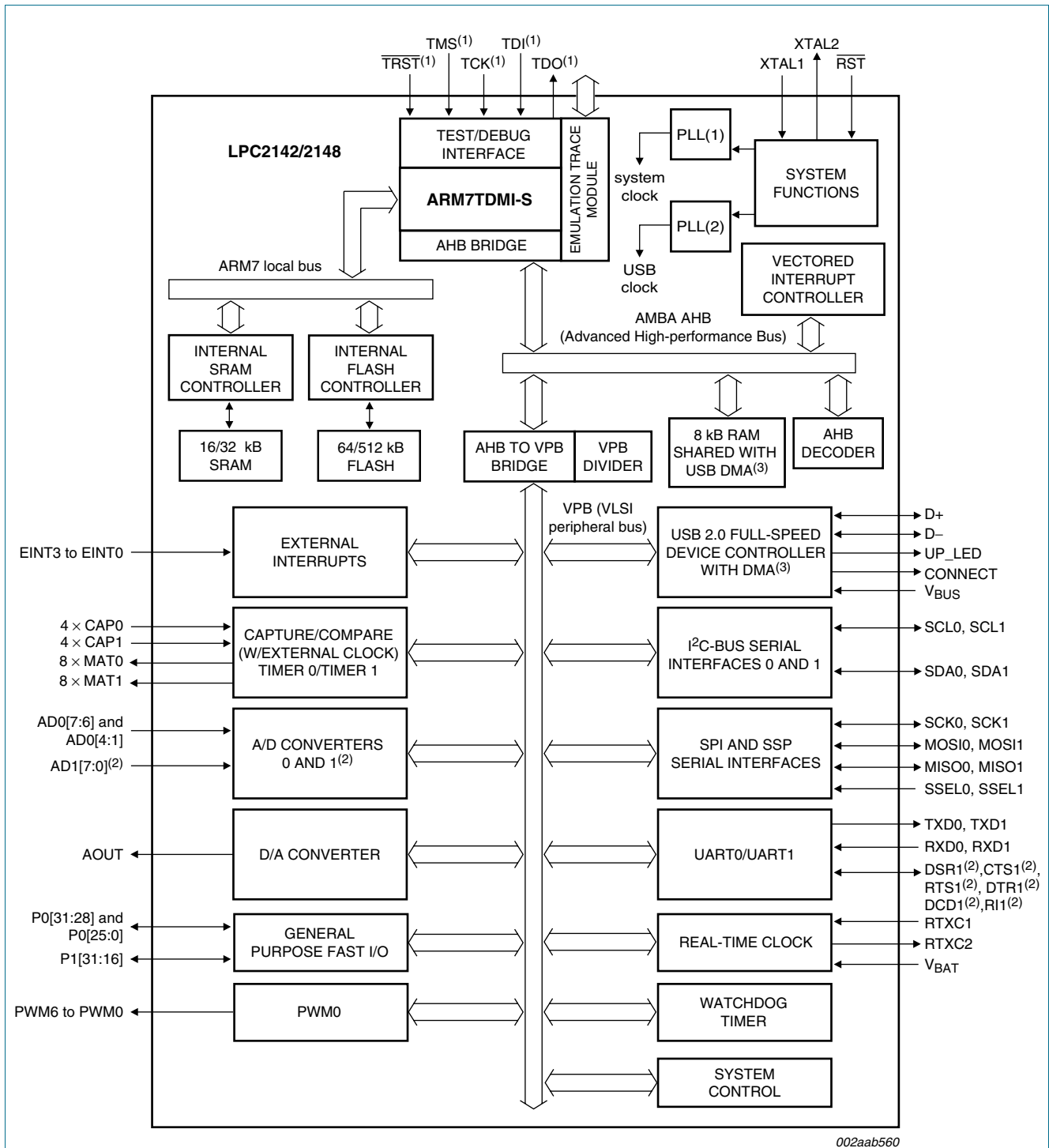
Type number	Package		
	Name	Description	Version
LPC2142FBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 $\times$ 10 $\times$ 1.4 mm	SOT314-2
LPC2148FBD64			

#### 3.1 Ordering options

Table 2: Ordering options

Type number	Flash memory	RAM	Endpoint USB RAM	ADC (channels overall)	DAC	Temperature range (°C)
LPC2142FBD64	64 kB	16 kB	2 kB	1 (6 channels)	1	-40 to +85
LPC2148FBD64	512 kB	32 kB + 8 kB shared with USB DMA	2 kB	2 (14 channels)	1	-40 to +85

### 4. Block diagram



002aab560

(1) Pins shared with GPIO.

(2) LPC2148 only.

(3) USB DMA controller with 8 kB of RAM accessible as general purpose RAM and/or DMA is available in LPC2148 only.

Fig 1. Block diagram

## 5. Pinning information

### 5.1 Pinning

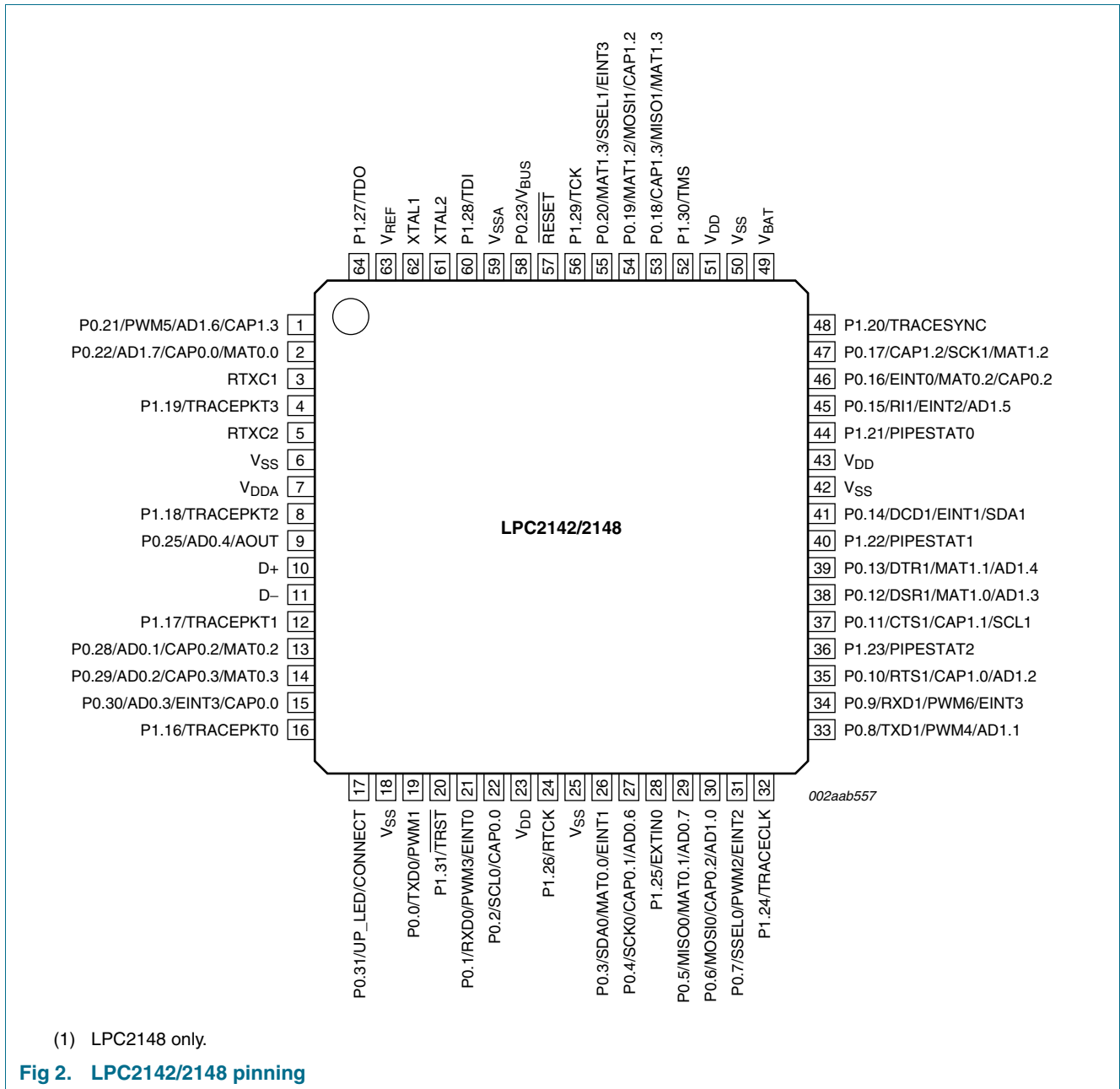


Fig 2. LPC2142/2148 pinning

## 5.2 Pin description

Table 3: Pin description

Symbol	Pin	Type	Description
P0.0 to P0.31		I/O	<b>Port 0:</b> Port 0 is a 32-bit I/O port with individual direction controls for each bit. Total of 31 pins of the Port 0 can be used as a general purpose bidirectional digital I/Os while P0.31 is output only pin. The operation of port 0 pins depends upon the pin function selected via the pin connect block. Pins P0.24, P0.26 and P0.27 are not available.
P0.0/TXD0/ PWM1	19 <a href="#">[1]</a>	I/O	<b>P0.0</b> — General purpose input/output digital pin (GPIO).
		O	<b>TXD0</b> — Transmitter output for UART0.
		O	<b>PWM1</b> — Pulse Width Modulator output 1.
P0.1/RXD0/ PWM3/EINT0	21 <a href="#">[2]</a>	I/O	<b>P0.1</b> — General purpose input/output digital pin (GPIO).
		I	<b>RXD0</b> — Receiver input for UART0.
		O	<b>PWM3</b> — Pulse Width Modulator output 3.
		I	<b>EINT0</b> — External interrupt 0 input
P0.2/SCL0/ CAP0.0	22 <a href="#">[3]</a>	I/O	<b>P0.2</b> — General purpose input/output digital pin (GPIO).
		I/O	<b>SCL0</b> — I <sup>2</sup> C0 clock input/output. Open-drain output (for I <sup>2</sup> C-bus compliance).
		I	<b>CAP0.0</b> — Capture input for Timer 0, channel 0.
P0.3/SDA0/ MAT0.0/EINT1	26 <a href="#">[3]</a>	I/O	<b>P0.3</b> — General purpose input/output digital pin (GPIO).
		I/O	<b>SDA0</b> — I <sup>2</sup> C0 data input/output. Open-drain output (for I <sup>2</sup> C-bus compliance).
		O	<b>MAT0.0</b> — Match output for Timer 0, channel 0.
		I	<b>EINT1</b> — External interrupt 1 input.
P0.4/SCK0/ CAP0.1/AD0.6	27 <a href="#">[4]</a>	I/O	<b>P0.4</b> — General purpose input/output digital pin (GPIO).
		I/O	<b>SCK0</b> — Serial clock for SPI0. SPI clock output from master or input to slave.
		I	<b>CAP0.1</b> — Capture input for Timer 0, channel 0.
		I	<b>AD0.6</b> — ADC 0, input 6.
P0.5/MISO0/ MAT0.1/AD0.7	29 <a href="#">[4]</a>	I/O	<b>P0.5</b> — General purpose input/output digital pin (GPIO).
		I/O	<b>MISO0</b> — Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave.
		O	<b>MAT0.1</b> — Match output for Timer 0, channel 1.
		I	<b>AD0.7</b> — ADC 0, input 7.
P0.6/MOSI0/ CAP0.2/AD1.0	30 <a href="#">[4]</a>	I/O	<b>P0.6</b> — General purpose input/output digital pin (GPIO).
		I/O	<b>MOSI0</b> — Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	<b>CAP0.2</b> — Capture input for Timer 0, channel 2.
		I	<b>AD1.0</b> — ADC 1, input 0. Available in LPC2148 only.
P0.7/SSEL0/ PWM2/EINT2	31 <a href="#">[2]</a>	I/O	<b>P0.7</b> — General purpose input/output digital pin (GPIO).
		I	<b>SSEL0</b> — Slave Select for SPI0. Selects the SPI interface as a slave.
		O	<b>PWM2</b> — Pulse Width Modulator output 2.
		I	<b>EINT2</b> — External interrupt 2 input.
P0.8/TXD1/ PWM4/AD1.1	33 <a href="#">[4]</a>	I/O	<b>P0.8</b> — General purpose input/output digital pin (GPIO).
		O	<b>TXD1</b> — Transmitter output for UART1.
		O	<b>PWM4</b> — Pulse Width Modulator output 4.
		I	<b>AD1.1</b> — ADC 1, input 1. Available in LPC2148 only.

Table 3: Pin description ...continued

Symbol	Pin	Type	Description
P0.9/RXD1/ PWM6/EINT3	34 <a href="#">[2]</a>	I/O	<b>P0.9</b> — General purpose input/output digital pin (GPIO).
		I	<b>RXD1</b> — Receiver input for UART1.
		O	<b>PWM6</b> — Pulse Width Modulator output 6.
		I	<b>EINT3</b> — External interrupt 3 input.
P0.10/RTS1/ CAP1.0/AD1.2	35 <a href="#">[4]</a>	I/O	<b>P0.10</b> — General purpose input/output digital pin (GPIO).
		O	<b>RTS1</b> — Request to Send output for UART1. Available in LPC2148 only.
		I	<b>CAP1.0</b> — Capture input for Timer 1, channel 0.
		I	<b>AD1.2</b> — ADC 1, input 2. Available in LPC2148 only.
P0.11/CTS1/ CAP1.1/SCL1	37 <a href="#">[3]</a>	I/O	<b>P0.11</b> — General purpose input/output digital pin (GPIO).
		I	<b>CTS1</b> — Clear to Send input for UART1. Available in LPC2148 only.
		I	<b>CAP1.1</b> — Capture input for Timer 1, channel 1.
		I/O	<b>SCL1</b> — I <sup>2</sup> C1 clock input/output. Open-drain output (for I <sup>2</sup> C-bus compliance)
P0.12/DSR1/ MAT1.0/AD1.3	38 <a href="#">[4]</a>	I/O	<b>P0.12</b> — General purpose input/output digital pin (GPIO).
		I	<b>DSR1</b> — Data Set Ready input for UART1. Available in LPC2148 only.
		O	<b>MAT1.0</b> — Match output for Timer 1, channel 0.
		I	<b>AD1.3</b> — ADC input 3. Available in LPC2148 only.
P0.13/DTR1/ MAT1.1/AD1.4	39 <a href="#">[4]</a>	I/O	<b>P0.13</b> — General purpose input/output digital pin (GPIO).
		O	<b>DTR1</b> — Data Terminal Ready output for UART1. Available in LPC2148 only.
		O	<b>MAT1.1</b> — Match output for Timer 1, channel 1.
		I	<b>AD1.4</b> — ADC input 4. Available in LPC2148 only.
P0.14/DCD1/ EINT1/SDA1	41 <a href="#">[3]</a>	I/O	<b>P0.14</b> — General purpose input/output digital pin (GPIO).
		I	<b>DCD1</b> — Data Carrier Detect input for UART1. Available in LPC2148 only.
		I	<b>EINT1</b> — External interrupt 1 input.
		I/O	<b>SDA1</b> — I <sup>2</sup> C1 data input/output. Open-drain output (for I <sup>2</sup> C-bus compliance)
P0.15/RI1/ EINT2/AD1.5	45 <a href="#">[4]</a>	I/O	<b>P0.15</b> — General purpose input/output digital pin (GPIO).
		I	<b>RI1</b> — Ring Indicator input for UART1. Available in LPC2148 only.
		I	<b>EINT2</b> — External interrupt 2 input.
		I	<b>AD1.5</b> — ADC 1, input 5. Available in LPC2148 only.
P0.16/EINT0/ MAT0.2/CAP0.2	46 <a href="#">[2]</a>	I/O	<b>P0.16</b> — General purpose input/output digital pin (GPIO).
		I	<b>EINT0</b> — External interrupt 0 input.
		O	<b>MAT0.2</b> — Match output for Timer 0, channel 2.
		I	<b>CAP0.2</b> — Capture input for Timer 0, channel 2.
P0.17/CAP1.2/ SCK1/MAT1.2	47 <a href="#">[1]</a>	I/O	<b>P0.17</b> — General purpose input/output digital pin (GPIO).
		I	<b>CAP1.2</b> — Capture input for Timer 1, channel 2.
		I/O	<b>SCK1</b> — Serial Clock for SSP. Clock output from master or input to slave.
		O	<b>MAT1.2</b> — Match output for Timer 1, channel 2.
P0.18/CAP1.3/ MISO1/MAT1.3	53 <a href="#">[1]</a>	I/O	<b>P0.18</b> — General purpose input/output digital pin (GPIO).
		I	<b>CAP1.3</b> — Capture input for Timer 1, channel 3.
		I/O	<b>MISO1</b> — Master In Slave Out for SSP. Data input to SPI master or data output from SSP slave.
		O	<b>MAT1.3</b> — Match output for Timer 1, channel 3.

Table 3: Pin description ...continued

Symbol	Pin	Type	Description
P0.19/MAT1.2/ MOSI1/CAP1.2	54 <a href="#">[1]</a>	I/O	<b>P0.19</b> — General purpose input/output digital pin (GPIO).
		O	<b>MAT1.2</b> — Match output for Timer 1, channel 2.
		I/O	<b>MOSI1</b> — Master Out Slave In for SSP. Data output from SSP master or data input to SSP slave.
		I	<b>CAP1.2</b> — Capture input for Timer 1, channel 2.
P0.20/MAT1.3/ SSEL1/EINT3	55 <a href="#">[2]</a>	I/O	<b>P0.20</b> — General purpose input/output digital pin (GPIO).
		O	<b>MAT1.3</b> — Match output for Timer 1, channel 3.
		I	<b>SSEL1</b> — Slave Select for SSP. Selects the SSP interface as a slave.
		I	<b>EINT3</b> — External interrupt 3 input.
P0.21/PWM5/ AD1.6/CAP1.3	1 <a href="#">[4]</a>	I/O	<b>P0.21</b> — General purpose input/output digital pin (GPIO).
		O	<b>PWM5</b> — Pulse Width Modulator output 5.
		I	<b>AD1.6</b> — ADC 1, input 6. Available in LPC2148 only.
		I	<b>CAP1.3</b> — Capture input for Timer 1, channel 3.
P0.22/AD1.7/ CAP0.0/MAT0.0	2 <a href="#">[4]</a>	I/O	<b>P0.22</b> — General purpose input/output digital pin (GPIO).
		I	<b>AD1.7</b> — ADC 1, input 7. Available in LPC2148 only.
		I	<b>CAP0.0</b> — Capture input for Timer 0, channel 0.
		O	<b>MAT0.0</b> — Match output for Timer 0, channel 0.
P0.23	58 <a href="#">[1]</a>	I/O	<b>P0.23</b> — General purpose input/output digital pin (GPIO).
		I/O	<b>V<sub>BUS</sub></b> — Indicates the presence of USB bus power.
P0.25/AD0.4/ AOUT	9 <a href="#">[5]</a>	I/O	<b>P0.25</b> — General purpose input/output digital pin (GPIO).
		I	<b>AD0.4</b> — ADC 0, input 4.
		O	<b>AOUT</b> — DAC output.
P0.28/AD0.1/ CAP0.2/MAT0.2	13 <a href="#">[4]</a>	I/O	<b>P0.28</b> — General purpose input/output digital pin (GPIO).
		I	<b>AD0.1</b> — ADC 0, input 1.
		I	<b>CAP0.2</b> — Capture input for Timer 0, channel 2.
		O	<b>MAT0.2</b> — Match output for Timer 0, channel 2.
P0.29/AD0.2/ CAP0.3/MAT0.3	14 <a href="#">[4]</a>	I/O	<b>P0.29</b> — General purpose input/output digital pin (GPIO).
		I	<b>AD0.2</b> — ADC 0, input 2.
		I	<b>CAP0.3</b> — Capture input for Timer 0, Channel 3.
		O	<b>MAT0.3</b> — Match output for Timer 0, channel 3.
P0.30/AD0.3/ EINT3/CAP0.0	15 <a href="#">[4]</a>	I/O	<b>P0.30</b> — General purpose input/output digital pin (GPIO).
		I	<b>AD0.3</b> — ADC 0, input 3.
		I	<b>EINT3</b> — External interrupt 3 input.
		I	<b>CAP0.0</b> — Capture input for Timer 0, channel 0.

Table 3: Pin description ...continued

Symbol	Pin	Type	Description
P0.31/UP_LED/ CONNECT	17 <a href="#">[6]</a>	O	<b>P0.31</b> — General purpose output only digital pin (GPO).
		O	<b>UP_LED</b> — USB Good Link LED indicator. It is LOW when device is configured (non-control endpoints enabled). It is HIGH when the device is not configured or during global suspend.
		O	<b>CONNECT</b> — Signal used to switch an external 1.5 kΩ resistor under the software control. Used with the Soft Connect USB feature. <b>Important:</b> This is an digital output only pin. This pin <b>MUST NOT</b> be externally pulled LOW when RESET pin is LOW or the JTAG port will be disabled.
P1.0 to P1.31		I/O	<b>Port 1:</b> Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block. Pins 0 through 15 of port 1 are not available.
P1.16/ TRACEPKT0	16 <a href="#">[6]</a>	I/O	<b>P1.16</b> — General purpose input/output digital pin (GPIO).
		O	<b>TRACEPKT0</b> — Trace Packet, bit 0. Standard I/O port with internal pull-up.
P1.17/ TRACEPKT1	12 <a href="#">[6]</a>	I/O	<b>P1.17</b> — General purpose input/output digital pin (GPIO).
		O	<b>TRACEPKT1</b> — Trace Packet, bit 1. Standard I/O port with internal pull-up.
P1.18/ TRACEPKT2	8 <a href="#">[6]</a>	I/O	<b>P1.18</b> — General purpose input/output digital pin (GPIO).
		O	<b>TRACEPKT2</b> — Trace Packet, bit 2. Standard I/O port with internal pull-up.
P1.19/ TRACEPKT3	4 <a href="#">[6]</a>	I/O	<b>P1.19</b> — General purpose input/output digital pin (GPIO).
		O	<b>TRACEPKT3</b> — Trace Packet, bit 3. Standard I/O port with internal pull-up.
P1.20/ TRACESYNC	48 <a href="#">[6]</a>	I/O	<b>P1.20</b> — General purpose input/output digital pin (GPIO).
		O	<b>TRACESYNC</b> — Trace Synchronization. Standard I/O port with internal pull-up. LOW on TRACESYNC while RESET is LOW enables pins P1[25:16] to operate as Trace port after reset.
P1.21/ PIPESTAT0	44 <a href="#">[6]</a>	I/O	<b>P1.21</b> — General purpose input/output digital pin (GPIO).
		O	<b>PIPESTAT0</b> — Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P1.22/ PIPESTAT1	40 <a href="#">[6]</a>	I/O	<b>P1.22</b> — General purpose input/output digital pin (GPIO).
		O	<b>PIPESTAT1</b> — Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P1.23/ PIPESTAT2	36 <a href="#">[6]</a>	I/O	<b>P1.23</b> — General purpose input/output digital pin (GPIO).
		O	<b>PIPESTAT2</b> — Pipeline Status, bit 2. Standard I/O port with internal pull-up.
P1.24/ TRACECLK	32 <a href="#">[6]</a>	I/O	<b>P1.24</b> — General purpose input/output digital pin (GPIO).
		O	<b>TRACECLK</b> — Trace Clock. Standard I/O port with internal pull-up.
P1.25/EXTINO	28 <a href="#">[6]</a>	I/O	<b>P1.25</b> — General purpose input/output digital pin (GPIO).
		I	<b>EXTINO</b> — External Trigger Input. Standard I/O with internal pull-up.
P1.26/RTCK	24 <a href="#">[6]</a>	I/O	<b>P1.26</b> — General purpose input/output digital pin (GPIO).
		I/O	<b>RTCK</b> — Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. LOW on RTCK while RESET is LOW enables pins P1.31:26 to operate as Debug port after reset.
P1.27/TDO	64 <a href="#">[6]</a>	I/O	<b>P1.27</b> — General purpose input/output digital pin (GPIO).
		O	<b>TDO</b> — Test Data out for JTAG interface.
P1.28/TDI	60 <a href="#">[6]</a>	I/O	<b>P1.28</b> — General purpose input/output digital pin (GPIO).
		I	<b>TDI</b> — Test Data in for JTAG interface.



Table 3: Pin description ...continued

Symbol	Pin	Type	Description
P1.29/TCK	56 [6]	I/O	<b>P1.29</b> — General purpose input/output digital pin (GPIO).
		I	<b>TCK</b> — Test Clock for JTAG interface.
P1.30/TMS	52 [6]	I/O	<b>P1.30</b> — General purpose input/output digital pin (GPIO).
		I	<b>TMS</b> — Test Mode Select for JTAG interface.
P1.31/ $\overline{\text{TRST}}$	20 [6]	I/O	<b>P1.31</b> — General purpose input/output digital pin (GPIO).
		I	<b><math>\overline{\text{TRST}}</math></b> — Test Reset for JTAG interface.
D+	10 [7]	I/O	USB bidirectional D+ line.
D-	11 [7]	I/O	USB bidirectional D- line.
$\overline{\text{RESET}}$	57 [8]	I	<b>External reset input:</b> A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	62 [9]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	61 [9]	O	Output from the oscillator amplifier.
RTXC1	3 [9]	I	Input to the RTC oscillator circuit.
RTXC2	5 [9]	O	Output from the RTC oscillator circuit.
V <sub>SS</sub>	6, 18, 25, 42, 50	I	<b>Ground:</b> 0 V reference.
V <sub>SSA</sub>	59	I	<b>Analog ground:</b> 0 V reference. This should nominally be the same voltage as V <sub>SS</sub> , but should be isolated to minimize noise and error.
V <sub>DD</sub>	23, 43, 51	I	<b>3.3 V power supply:</b> This is the power supply voltage for the core and I/O ports.
V <sub>DDA</sub>	7	I	<b>Analog 3.3 V power supply:</b> This should be nominally the same voltage as V <sub>DD</sub> but should be isolated to minimize noise and error. This voltage is used to power the on-chip PLL.
V <sub>REF</sub>	63	I	<b>ADC reference:</b> This should be nominally the same voltage as V <sub>DD</sub> but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC(s) and DAC(s).
V <sub>BAT</sub>	49	I	<b>RTC power supply:</b> 3.3 V on this pin supplies the power to the RTC.

- [1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control.
- [2] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns.
- [3] Open-drain 5 V tolerant digital I/O I<sup>2</sup>C-bus 400 kHz specification compatible pad. It requires external pull-up to provide an output functionality.
- [4] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog input function. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns. When configured as an ADC input, digital section of the pad is disabled.
- [5] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog output function. When configured as the DAC output, digital section of the pad is disabled.
- [6] 5 V tolerant pad with built-in pull-up resistor providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. The pull-up resistor's value typically ranges from 60 k $\Omega$  to 300 k $\Omega$ .
- [7] Pad is designed in accordance with the Universal Serial Bus (USB) specification, revision 2.0 (Full-speed and Low-speed mode only).
- [8] 5 V tolerant pad providing digital input (with TTL levels and hysteresis) function only.
- [9] Pad provides special analog functionality.

## 6. Functional description

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### 6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

### 6.2 On-chip flash program memory

The LPC2142/2148 incorporate a 64 kB and 512 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. Due to the architectural solution chosen for an on-chip bootloader, flash memory available for user's code on LPC2142/2148 is 64 and 500 kB respectively.

The LPC2142/2148 flash memory provides a minimum of 100,000 erase/write cycles and 20 years of data-retention.

### 6.3 On-chip static RAM

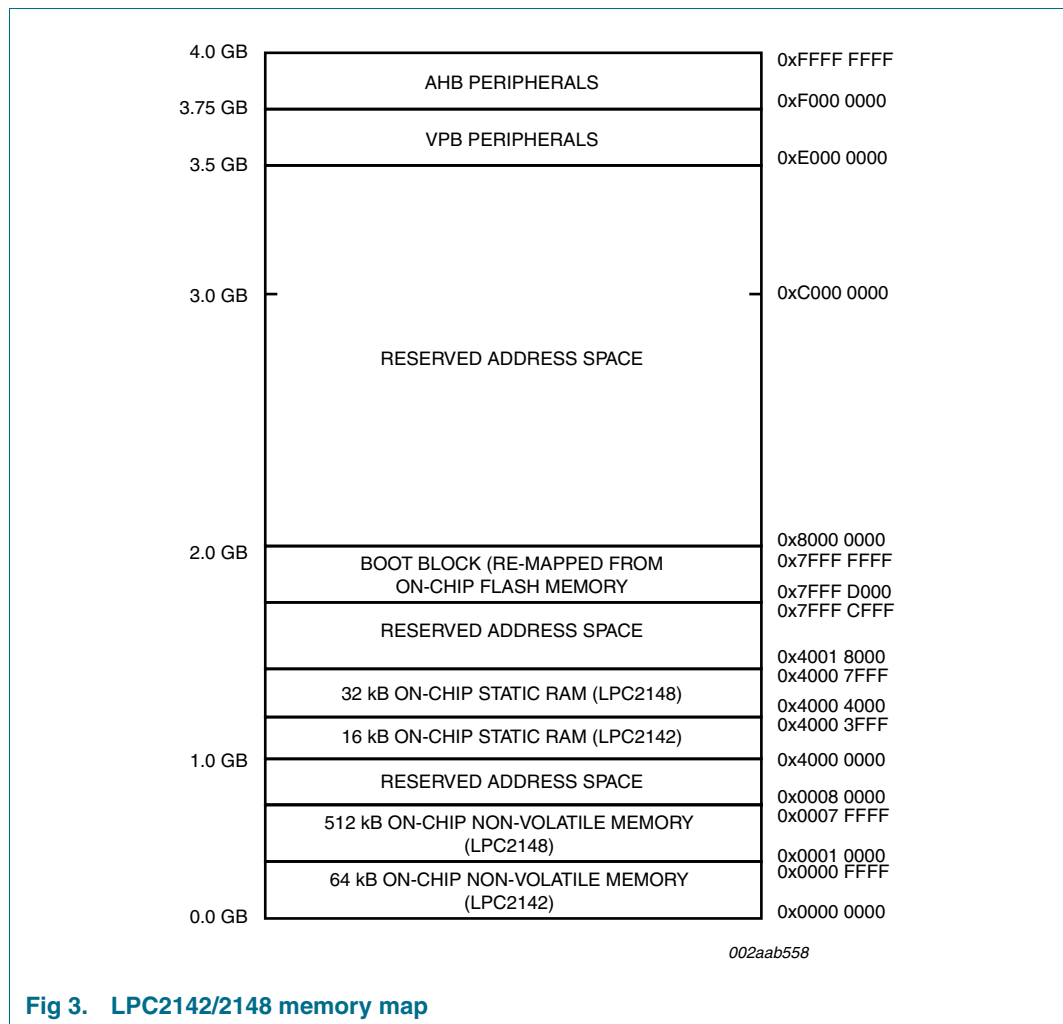
On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8-bits, 16-bits, and 32-bits. The LPC2142/2148 provide 16 kB and 32 kB of static RAM.

In case of LPC2148 only, an 8 kB SRAM block intended to be utilized mainly by the USB can also be used as a general purpose RAM for data storage and code storage and execution.

### 6.4 Memory map

The LPC2142/2148 memory map incorporates several distinct regions, as shown in [Figure 3](#).

In addition, the CPU interrupt vectors may be remapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in [Section 6.22](#) “System control”.



### 6.5 Interrupt controller

The VIC accepts all of the interrupt request inputs and categorizes them as Fast Interrupt Request (FIQ), vectored Interrupt Request (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are requesting, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

### 6.5.1 Interrupt sources

[Table 4](#) lists the interrupt sources for each peripheral function. Each peripheral device has one interrupt line connected to the VIC, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

**Table 4: Interrupt sources**

Block	Flag(s)	VIC channel #
WDT	Watchdog Interrupt (WDINT)	0
-	Reserved for software interrupts only	1
ARM Core	Embedded ICE, DbgCommRX	2
ARM Core	Embedded ICE, DbgCommTX	3
TIMER0	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	4
TIMER1	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	5
UART0	RX Line Status (RLS) Transmit Holding Register empty (THRE) RX Data Available (RDA) Character Time-out Indicator (CTI)	6
UART1	RX Line Status (RLS) Transmit Holding Register empty (THRE) RX Data Available (RDA) Character Time-out Indicator (CTI) Modem Status Interrupt (MSI) (LPC2148 only)	7
PWM0	Match 0 to 6 (MR0, MR1, MR2, MR3, MR4, MR5, MR6) Capture 0 to 3 (CR0, CR1, CR2, CR3)	8
I <sup>2</sup> C0	SI (state change)	9
SPI0	SPIF, MODF	10

**Table 4:** Interrupt sources ...continued

Block	Flag(s)	VIC channel #
SSP	TX FIFO at least half empty (TXRIS)	11
	RX FIFO at least half full (RXRIS)	
	Receive Timeout (RTRIS)	
	Receive Overrun (RORRIS)	
PLL	PLL Lock (PLOCK)	12
RTC	RTCCIF (Counter Increment), RTCALF (Alarm)	13
System Control	External Interrupt 0 (EINT0)	14
	External Interrupt 1 (EINT1)	15
	External Interrupt 2 (EINT2)	16
	External Interrupt 3 (EINT3)	17
AD0	ADC 0	18
I2C1	SI (state change)	19
BOD	Brownout Detect	20
AD1	ADC 1	21
USB	DMA interrupt, USB high priority interrupts, USB low priority interrupts	22

## 6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

The Pin Control Module contains three registers as shown in [Table 5](#).

**Table 5:** Pin control module registers

Address	Name	Description	Access
0xE002 C000	PINSEL0	Pin function select register 0	Read/Write
0xE002 C004	PINSEL1	Pin function select register 1	Read/Write
0xE002 C014	PINSEL2	Pin function select register 2	Read/Write

## 6.7 Pin function select register 0 (PINSEL0 - 0xE002 C000)

The PINSEL0 register controls the functions of the pins as per the settings listed in [Table 6](#). The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically. Settings other than those shown in [Table 6](#) are reserved, and should not be used.

**Table 6: Pin function select register 0 (PINSEL0 - 0xE002 C000)**

PINSEL0	Pin name	Value		Function	Value after reset
1:0	P0.0	0	0	GPIO Port 0.0	0
		0	1	TXD (UART0)	
		1	0	PWM1	
		1	1	Reserved	
3:2	P0.1	0	0	GPIO Port 0.1	0
		0	1	RXD (UART0)	
		1	0	PWM3	
		1	1	EINT0	
5:4	P0.2	0	0	GPIO Port 0.2	0
		0	1	SCL0 (I <sup>2</sup> C0)	
		1	0	Capture 0.0 (Timer 0)	
		1	1	Reserved	
7:6	P0.3	0	0	GPIO Port 0.3	0
		0	1	SDA0 (I <sup>2</sup> C0)	
		1	0	Match 0.0 (Timer 0)	
		1	1	EINT1	
9:8	P0.4	0	0	GPIO Port 0.4	0
		0	1	SCK0 (SPI0)	
		1	0	Capture 0.1 (Timer 0)	
		1	1	AD0.6	
11:10	P0.5	0	0	GPIO Port 0.5	0
		0	1	MISO0 (SPI0)	
		1	0	Match 0.1 (Timer 0)	
		1	1	AD0.7	
13:12	P0.6	0	0	GPIO Port 0.6	0
		0	1	MOSI0 (SPI0)	
		1	0	Capture 0.2 (Timer 0)	
		1	1	Reserved (LPC2142) AD1.0 (LPC2148)	
15:14	P0.7	0	0	GPIO Port 0.7	0
		0	1	SSEL0 (SPI0)	
		1	0	PWM2	
		1	1	EINT2	

Table 6: Pin function select register 0 (PINSEL0 - 0xE002 C000) ...continued

PINSEL0	Pin name	Value	Value	Function	Value after reset
17:16	P0.8	0	0	GPIO Port 0.8	0
		0	1	TXD UART1	
		1	0	PWM4	
		1	1	Reserved (LPC2142) AD1.1 (LPC2148)	
19:18	P0.9	0	0	GPIO Port 0.9	0
		0	1	RXD (UART1)	
		1	0	PWM6	
		1	1	EINT3	
21:20	P0.10	0	0	GPIO Port 0.10	0
		0	1	Reserved (LPC2142) RTS (UART1) (LPC2148)	
		1	0	Capture 1.0 (Timer 1)	
		1	1	Reserved (LPC2142) AD1.2 (LPC2148)	
23:22	P0.11	0	0	GPIO Port 0.11	0
		0	1	Reserved (LPC2142) CTS (UART1) (LPC2148)	
		1	0	Capture 1.1 (Timer 1)	
		1	1	SCL1 (I <sup>2</sup> C1)	
25:24	P0.12	0	0	GPIO Port 0.12	0
		0	1	Reserved (LPC2142) DSR (UART1) (LPC2148)	
		1	0	Match 1.0 (Timer 1)	
		1	1	Reserved (LPC2142) AD1.3 (LPC2148)	
27:26	P0.13	0	0	GPIO Port 0.13	0
		0	1	Reserved (LPC2142) DTR (UART1) (LPC2148)	
		1	0	Match 1.1 (Timer 1)	
		1	1	Reserved (LPC2142) AD1.4 (LPC2148)	
29:28	P0.14	0	0	GPIO Port 0.14	0
		0	1	Reserved (LPC2142) DCD (UART1) (LPC2148)	
		1	0	EINT1	
		1	1	SDA1 (I <sup>2</sup> C1)	
31:30	P0.15	0	0	GPIO Port 0.15	0
		0	1	Reserved (LPC2142) RI (UART1) (LPC2148)	
		1	0	EINT2	
		1	1	Reserved (LPC2142) AD1.5 (LPC2148)	

## 6.8 Pin function select register 1 (PINSEL1 - 0xE002 C004)

The PINSEL1 register controls the functions of the pins as per the settings listed in [Table 7](#). The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions direction is controlled automatically. Settings other than those shown in [Table 7](#) are reserved, and should not be used.

**Table 7: Pin function select register 1 (PINSEL1 - 0xE002 C004)**

PINSEL1	Pin Name	Value		Function	Value after reset
1:0	P0.16	0	0	GPIO Port 0.16	0
		0	1	EINT0	
		1	0	Match 0.2 (Timer 0)	
		1	1	Capture 0.2 (Timer 0)	
3:2	P0.17	0	0	GPIO Port 0.17	0
		0	1	Capture 1.2 (Timer 1)	
		1	0	SCK (SSP)	
		1	1	Match 1.2 (Timer 1)	
5:4	P0.18	0	0	GPIO Port 0.18	0
		0	1	Capture 1.3 (Timer 1)	
		1	0	MISO (SSP)	
		1	1	Match 1.3 (Timer 1)	
7:6	P0.19	0	0	GPIO Port 0.19	0
		0	1	Match 1.2 (Timer 1)	
		1	0	MOSI (SSP)	
		1	1	Capture 1.2 (Timer 1)	
9:8	P0.20	0	0	GPIO Port 0.20	0
		0	1	Match 1.3 (Timer 1)	
		1	0	SSEL (SSP)	
		1	1	EINT3	
11:10	P0.21	0	0	GPIO Port 0.21	0
		0	1	PWM5	
		1	0	Reserved (LPC2142) AD1.6 (LPC2148)	
		1	1	Capture 1.3 (Timer 1)	
13:12	P0.22	0	0	GPIO Port 0.22	0
		0	1	Reserved (LPC2142) AD1.7 (LPC2148)	
		1	0	Capture 0.0 (Timer 0)	
		1	1	Match 0.0 (Timer 0)	
15:14	P0.23	0	0	GPIO Port 0.23	0
		0	1	V <sub>BUS</sub>	
		1	0	Reserved	
		1	1	Reserved	



Table 7: Pin function select register 1 (PINSEL1 - 0xE002 C004) ...continued

PINSEL1	Pin Name	Value	Value	Function	Value after reset
17:16	P0.24	0	0	Reserved	0
		0	1	Reserved	
		1	0	Reserved	
		1	1	Reserved	
19:18	P0.25	0	0	GPIO Port 0.25	0
		0	1	AD0.4	
		1	0	AOUT (DAC)	
		1	1	Reserved	
21:20	P0.26	0	0	Reserved	0
		0	1	Reserved	
		1	0	Reserved	
		1	1	Reserved	
23:22	P0.27	0	0	Reserved	0
		0	1	Reserved	
		1	0	Reserved	
		1	1	Reserved	
25:24	P0.28	0	0	GPIO Port 0.28	0
		0	1	AD0.1	
		1	0	Capture 0.2 (Timer 0)	
		1	1	Match 0.2 (Timer 0)	
27:26	P0.29	0	0	GPIO Port 0.29	0
		0	1	AD0.2	
		1	0	Capture 0.3 (Timer 0)	
		1	1	Match 0.3 (Timer 0)	
29:28	P0.30	0	0	GPIO Port 0.30	0
		0	1	AD0.3	
		1	0	EINT3	
		1	1	Capture 0.0 (Timer 0)	
31:30	P0.31	0	0	GPIO Port	0
		0	1	UP_LED	
		1	0	CONNECT	
		1	1	Reserved	

## 6.9 Pin function select register 2 (PINSEL2 - 0xE002 C014)

The PINSEL2 register controls the functions of the pins as per the settings listed in [Table 8](#). The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions direction is controlled automatically. Settings other than those shown in [Table 8](#) are reserved, and should not be used.

Table 8: Pin function select register 2 (PINSEL2 - 0xE002 C014)

PINSEL2 bits	Description	Reset value
1:0	Reserved	-
2	When 0, pins P1.31:26 are GPIO pins. When 1, P1.31:26 are used as Debug port.	0
3	When 0, pins P1.25:16 are used as GPIO pins. When 1, P1.25:16 are used as Trace port.	0
31:30	Reserved	-

## 6.10 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

LPC2142/2148 introduce accelerated GPIO functions over prior LPC2000 devices:

- GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte addressable.
- Entire port value can be written in one instruction.

### 6.10.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

## 6.11 10-bit ADC

The LPC2142 contains one and the LPC2148 contains two analog to digital converters. These converters are single 10-bit successive approximation analog to digital converters. While ADC0 has six channels, ADC1 has eight channels. Therefore, total number of available ADC inputs for LPC2142 is six and for LPC2148 is 14.

### 6.11.1 Features

- Measurement range of 0 V to 3.3 V.
- Each converter capable of performing more than 400,000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or timer match signal.
- Global Start command for both converters (LPC2148 only).

## 6.12 10-bit DAC

The DAC enables the LPC2142/2148 to generate a variable analog output.

### 6.12.1 Features

- 10-bit DAC.
- Buffered output.
- Power-down mode available.
- Selectable speed versus power.

## 6.13 USB 2.0 device controller

The USB is a 4-wire serial bus that supports communication between a host and a number (127 max) of peripherals. The host controller allocates the USB bandwidth to attached devices through a token based protocol. The bus supports hot plugging, unplugging, and dynamic configuration of the devices. All transactions are initiated by the host controller.

The LPC2142/2148 is equipped with a USB device controller that enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory and DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate end point buffer memory. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

A DMA controller (available in LPC2148 only) can transfer data between an endpoint buffer and the USB RAM.

### 6.13.1 Features

- Fully compliant with USB 2.0 Full-speed specification.
- Supports 32 physical (16 logical) endpoints.
- Supports control, bulk, interrupt and isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint maximum packet size selection (up to USB maximum specification) by software at run time.
- RAM message buffer size based on endpoint realization and maximum packet size.
- Supports SoftConnect and GoodLink LED indicator. These two functions are sharing one pin.
- Supports bus-powered capability with low suspend current.
- Supports DMA transfer on all non-control endpoints (LPC2148 only).
- One duplex DMA channel serves all endpoints (LPC2148 only).
- Allows dynamic switching between CPU controlled and DMA modes (LPC2148 only).
- Double buffer implementation for bulk and isochronous endpoints.

## 6.14 UARTs

The LPC2142/2148 each contain two UARTs. In addition to standard transmit and receive data lines, the LPC2148 UART1 also provides a full modem control handshake interface.

Compared to previous LPC2000 microcontrollers, UARTs in LPC2142/2148 introduce fractional baud rate generator (in both UARTs) and auto-CTS/RTS flow-control functions fully implemented in hardware (UART1 in LPC2148 only).

### 6.14.1 Features

- 16 byte Receive and Transmit FIFOs.
- Register locations conform to '550 industry standard.
- Receiver FIFO trigger points at 1, 4, 8, and 14 bytes
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs.
- LPC2148 UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).

## 6.15 I<sup>2</sup>C-bus serial I/O controller

The LPC2142/2148 each contain two I<sup>2</sup>C-bus controllers.

The I<sup>2</sup>C-bus is bidirectional, for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory)). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I<sup>2</sup>C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I<sup>2</sup>C-bus implemented in LPC2142/2148 supports bit rates up to 400 kbit/s (Fast I<sup>2</sup>C-bus).

### 6.15.1 Features

- Compliant with standard I<sup>2</sup>C-bus interface.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.

- The I<sup>2</sup>C-bus may be used for test and diagnostic purposes.

## 6.16 SPI serial I/O controller

The LPC2142/2148 each contain one SPI controller. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

### 6.16.1 Features

- Compliant with SPI specification.
- Synchronous, serial, full duplex, communication.
- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.

## 6.17 SSP serial I/O controller

The LPC2142/2148 each contain one SSP. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. However, only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. Often only one of these data flows carries meaningful data.

### 6.17.1 Features

- Compatible with Motorola's SPI, TI's 4-wire SSI and National Semiconductor's Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- Four bits to 16 bits per frame.

## 6.18 General purpose timers/external event counters

The Timer/Counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with 'or' and 'and', as well as 'broadcast' functions among them.

The LPC2142/2148 can count external events on one of the capture inputs if the minimum external pulse is equal or longer than a period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs.

### 6.18.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.

- External event counter or timer operation.
- Four 32-bit capture channels per timer/counter that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Four external outputs per timer/counter corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

## 6.19 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

### 6.19.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from ( $T_{PCLK} \times 256 \times 4$ ) to ( $T_{PCLK} \times 2^{32} \times 4$ ) in multiples of  $T_{PCLK} \times 4$ .

## 6.20 Real-time clock

The RTC is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

### 6.20.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.

- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Can use either the RTC dedicated 32 kHz oscillator input or clock derived from the external crystal/oscillator input at XTAL1. Programmable reference clock divider allows fine adjustment of the RTC.
- Dedicated power supply pin can be connected to a battery or the main 3.3 V.

## 6.21 Pulse width modulator

The PWM is based on the standard timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2142/2148. The timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

### 6.21.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.

- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must 'release' new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.

## 6.22 System control

### 6.22.1 Crystal oscillator

On-chip integrated oscillator operates with external crystal in range of 1 MHz to 30 MHz and with external oscillator up to 50 MHz. The oscillator output frequency is called  $f_{osc}$  and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc.  $f_{osc}$  and CCLK are the same value unless the PLL is running and connected. Refer to [Section 6.22.2 "PLL"](#) for additional information.

### 6.22.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100  $\mu$ s.

### 6.22.3 Reset and wake-up timer

Reset has two sources on the LPC2142/2148: the  $\overline{\text{RESET}}$  pin and watchdog reset. The  $\overline{\text{RESET}}$  pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the wake-up timer (see wake-up timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.



When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The wake-up timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up timer.

The wake-up timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of  $V_{DD}$  ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

#### 6.22.4 Brownout detector

The LPC2142/2148 include 2-stage monitoring of the voltage on the  $V_{DD}$  pins. If this voltage falls below 2.9 V, the BOD asserts an interrupt signal to the VIC. This signal can be enabled for interrupt; if not, software can monitor the signal by reading dedicated register.

The second stage of low voltage detection asserts reset to inactivate the LPC2142/2148 when the voltage on the  $V_{DD}$  pins falls below 2.6 V. This reset prevents alteration of the flash as operation of the various elements of the chip would otherwise become unreliable due to low voltage. The BOD circuit maintains this reset down below 1 V, at which point the POR circuitry maintains the overall reset.

Both the 2.9 V and 2.6 V thresholds include some hysteresis. In normal operation, this hysteresis allows the 2.9 V detection to reliably interrupt, or a regularly-executed event loop to sense the condition.

#### 6.22.5 Code security

This feature of the LPC2142/2148 allow an application to control whether it can be debugged or protected from observation.

If after reset on-chip boot-loader detects a valid checksum in flash and reads 0x8765 4321 from address 0x1FC in flash, debugging will be disabled and thus the code in flash will be protected from observation. Once debugging is disabled, it can be enabled only by performing a full chip erase using the ISP.

#### 6.22.6 External interrupt inputs

The LPC2142/2148 include up to nine edge or level sensitive External Interrupt Inputs as selectable pin functions. When the pins are combined, external events can be processed as four independent interrupt signals. The External Interrupt Inputs can optionally be used to wake-up the processor from Power-down mode.

### 6.22.7 Memory mapping control

The Memory Mapping Control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

### 6.22.8 Power control

The LPC2142/2148 supports two reduced power modes: Idle mode and Power-down mode.

In Idle mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

Selecting an external 32 kHz clock instead of the PCLK as a clock-source for the on-chip RTC will enable the microcontroller to have the RTC active during Power-down mode. Power-down current is increased with RTC active. However, it is significantly lower than in Idle mode.

A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

### 6.22.9 VPB bus

The VPB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The VPB divider serves two purposes. The first is to provide peripherals with the desired PCLK via VPB bus so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the VPB bus may be slowed down to  $\frac{1}{2}$  to  $\frac{1}{4}$  of the processor clock rate. Because the VPB bus must work properly at power-up (and its timing cannot be altered if it does not work since the VPB divider control registers reside on the VPB bus), the default condition at reset is for the VPB bus to run at  $\frac{1}{4}$  of the processor clock rate. The second purpose of the VPB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the VPB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

## 6.23 Emulation and debugging

The LPC2142/2148 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on Port 1. This means that all communication, timer and interface peripherals residing on Port 0 are available during the development and debugging phase as they are when the application is run in the embedded system itself.

### 6.23.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel (DCC) function built-in. The DCC allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The DCC is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The DCC allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The DCC data and control registers are mapped in to addresses in the EmbeddedICE logic.

### 6.23.2 Embedded trace

Since the LPC2142/2148 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell (ETM) provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

### 6.23.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real-time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC, which is present in the EmbeddedICE logic. The LPC2142/2148 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

## 7. Limiting values

**Table 9: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). [\[1\]](#)

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage, core and external rail		-0.5	+3.6	V
V <sub>DDA</sub>	analog 3.3 V pad supply voltage		-0.5	4.6	V
V <sub>BAT</sub>	RTC power supply voltage		-0.5	4.6	V
V <sub>REF</sub>	ADC reference voltage		-0.5	4.6	V
V <sub>IA</sub>	analog input voltage on ADC related pins		-0.5	5.1	V
V <sub>I</sub>	DC input voltage, 5 V tolerant I/O pins		<a href="#">[2]</a> <a href="#">[3]</a> -0.5	6.0	V
V <sub>I</sub>	DC input voltage, other I/O pins		<a href="#">[2]</a> -0.5	V <sub>DD</sub> + 0.5 <a href="#">[4]</a>	V
I <sub>DD</sub>	DC supply current per supply pin		-	100 <a href="#">[5]</a>	mA
I <sub>SS</sub>	DC ground current per ground pin		-	100 <a href="#">[5]</a>	mA
T <sub>stg</sub>	storage temperature <a href="#">[6]</a>		-40	125	°C
P <sub>tot(pack)</sub>	total power dissipation	based on package heat transfer, not device power consumption	-	1.5	W

[1] The following applies to the Limiting values:

- a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
- b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V<sub>SS</sub> unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] Only valid when the V<sub>DD</sub> supply voltage is present.

[4] Not to exceed 4.6 V.

[5] The peak current is limited to 25 times the corresponding maximum current.

[6] Dependent on package type.

## 8. Static characteristics

**Table 10: Static characteristics**
*T<sub>a</sub> = -40 °C to +85 °C for commercial applications, unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
V <sub>DD</sub>	supply voltage, core and external rail		3.0	3.3	3.6	V
V <sub>DDA</sub>	analog 3.3 V pad supply voltage		2.5	3.3	3.6	V
V <sub>BAT</sub>	RTC supply voltage		2.0 <sup>[2]</sup>	3.3	3.6	V
V <sub>REF</sub>	ADC reference voltage		3.0	3.3	3.6	V
<b>Standard port pins, <math>\overline{\text{RESET}}</math>, <math>\overline{\text{RTCK}}</math></b>						
I <sub>IL</sub>	LOW-state input current	V <sub>I</sub> = 0 V; no pull-up	-	-	3	μA
I <sub>IH</sub>	HIGH-state input current	V <sub>I</sub> = V <sub>DD</sub> ; no-pull-down	-	-	3	μA
I <sub>OZ</sub>	3-state output leakage current	V <sub>O</sub> = 0 V, V <sub>O</sub> = V <sub>DD</sub> ; no pull-up/down	-	-	3	μA
I <sub>latch</sub>	I/O latch-up current	-(0.5 V <sub>DD</sub> ) < V < (1.5 V <sub>DD</sub> ) T <sub>j</sub> < 125 °C	-	-	100	mA
V <sub>I</sub>	input voltage	pin configured to provide a digital function	0 <sup>[3] [4] [5]</sup>	-	5.5	V
V <sub>O</sub>	output voltage	output active	0	-	V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH-state input voltage		2.0	-	-	V
V <sub>IL</sub>	LOW-state input voltage		-	-	0.8	V
V <sub>hys</sub>	hysteresis voltage		-	0.4	-	V
V <sub>OH</sub>	HIGH-state output voltage <sup>[6]</sup>	I <sub>OH</sub> = -4 mA	V <sub>DD</sub> - 0.4	-	-	V
V <sub>OL</sub>	LOW-state output voltage <sup>[6]</sup>	I <sub>OL</sub> = -4 mA	-	-	0.4	V
I <sub>OH</sub>	HIGH-state output current <sup>[6]</sup>	V <sub>OH</sub> = V <sub>DD</sub> - 0.4 V	-4	-	-	mA
I <sub>OL</sub>	LOW-state output current <sup>[6]</sup>	V <sub>OL</sub> = 0.4 V	4	-	-	mA
I <sub>OHS</sub>	HIGH-state short circuit current <sup>[7]</sup>	V <sub>OH</sub> = 0 V	-	-	-45	mA
I <sub>OLS</sub>	LOW-state short circuit current <sup>[7]</sup>	V <sub>OL</sub> = V <sub>DDA</sub>	-	-	50	mA
I <sub>pd</sub>	pull-down current	V <sub>I</sub> = 5 V <sup>[8]</sup>	10	50	150	μA
I <sub>pu</sub>	pull-up current (applies to P1.16 to P1.25)	V <sub>I</sub> = 0 V	-15	-50	-85	μA
		V <sub>DD</sub> < V <sub>I</sub> < 5 V <sup>[8]</sup>	0	0	0	μA
I <sub>DD</sub>	active mode supply current	V <sub>DD</sub> = 3.3 V, T <sub>a</sub> = 25 °C, code while(1){} executed from flash, no active peripherals CCLK = 10 MHz	<td>	<td>	<td>	mA
		CCLK = 60 MHz (other parameters as above)	<td>	<td>	<td>	mA
		Power-down mode	<td>	<td>	<td>	μA
		V <sub>DD</sub> = 3.3 V, T <sub>a</sub> = +85 °C	<td>	<td>	<td>	μA

**Table 10: Static characteristics ...continued**

$T_a = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$  for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$I_{BAT}$	Power-down mode $V_{BAT}$ supply current—	RTC clock = 32 kHz (from RTXC pins), $T_a = +25\text{ }^\circ\text{C}$ $V_{DD} = 3.0\text{ V}$ , $V_{BAT} = 2.5\text{ V}$	<td>	<td>	<td>	$\mu\text{A}$
		$V_{DD} = 3.0\text{ V}$ , $V_{BAT} = 3.0\text{ V}$	<td>	<td>	<td>	$\mu\text{A}$
		active mode $V_{BAT}$ supply current	CCLK = 60 MHz, PCLK = 15 MHz, PCLK enabled to RTCK, RTC clock = 32 kHz (from RTXC pins), $T_a = +25\text{ }^\circ\text{C}$ $V_{DD} = 3.0\text{ V}$ , $V_{BAT} = 3.0\text{ V}$	<td>	<td>	<td>
$I_{BAT}$	active mode $V_{BAT}$ supply current optimized for low battery consumption	PCLK disabled to RTCK in the PCONP register, RTC clock = 32 kHz (from RTXC pins), $T_a = +25\text{ }^\circ\text{C}$ , $V_{BAT} = 3.3\text{ V}$ CCLK = 6 MHz	<td>	<td>	<td>	$\mu\text{A}$
		CCLK = 25 MHz	<td>	<td>	<td>	$\mu\text{A}$
		CCLK = 50 MHz	<td>	<td>	<td>	$\mu\text{A}$
		CCLK = 60 MHz	<td>	<td>	<td>	$\mu\text{A}$

**I<sup>2</sup>C-bus pins**

$V_{IH}$	HIGH-state input voltage		$0.7V_{DD(3V3)}$	-	-	V
$V_{IL}$	LOW-state input voltage		-	-	$0.3V_{DD(3V3)}$	V
$V_{hys}$	hysteresis voltage		-	$0.5V_{DD(3V3)}$	-	V
$V_{OL}$	LOW-state output voltage [6]	$I_{OLS} = 3\text{ mA}$	-	-	0.4	V
$I_{LI}$	input leakage current to $V_{SS}$	$V_I = V_{DD}$	-	2	4	$\mu\text{A}$
		$V_I = 5\text{ V}$	-	10	22	$\mu\text{A}$

**Oscillator pins**

$V_{XTAL1}$	XTAL1 input voltages		0	-	1.8	V
$V_{XTAL2}$	XTAL2 output voltages		0	-	1.8	V
$V_{RTXC1}$	RTXC1 input voltages		0	-	1.8	V
$V_{RTXC2}$	RTXC2 output voltages		0	-	1.8	V

**USB pins**

$I_{LO}$	high-Z state data line leakage	$0\text{ V} < V_I < 3.3\text{ V}$	-	-	$\pm 10$	$\mu\text{A}$
$V_{DI}$	differential input sensitivity	$ D(+) - D(-) $	0.2	-	-	V
$V_{CM}$	differential common mode range	includes $V_{DI}$ range	0.8	-	2.5	V
$V_{SE}$	single-ended receiver threshold		0.8	-	2.0	V
$V_{OL}$	static output LOW	$R_L$ of $1.5\text{ k}\Omega$ to $3.6\text{ V}$	-	-	0.3	V
$V_{OH}$	static output HIGH	$R_L$ of $15\text{ k}\Omega$ to GND	2.8	-	3.6	V

**Table 10: Static characteristics ...continued** $T_a = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$  for commercial applications, unless otherwise specified.

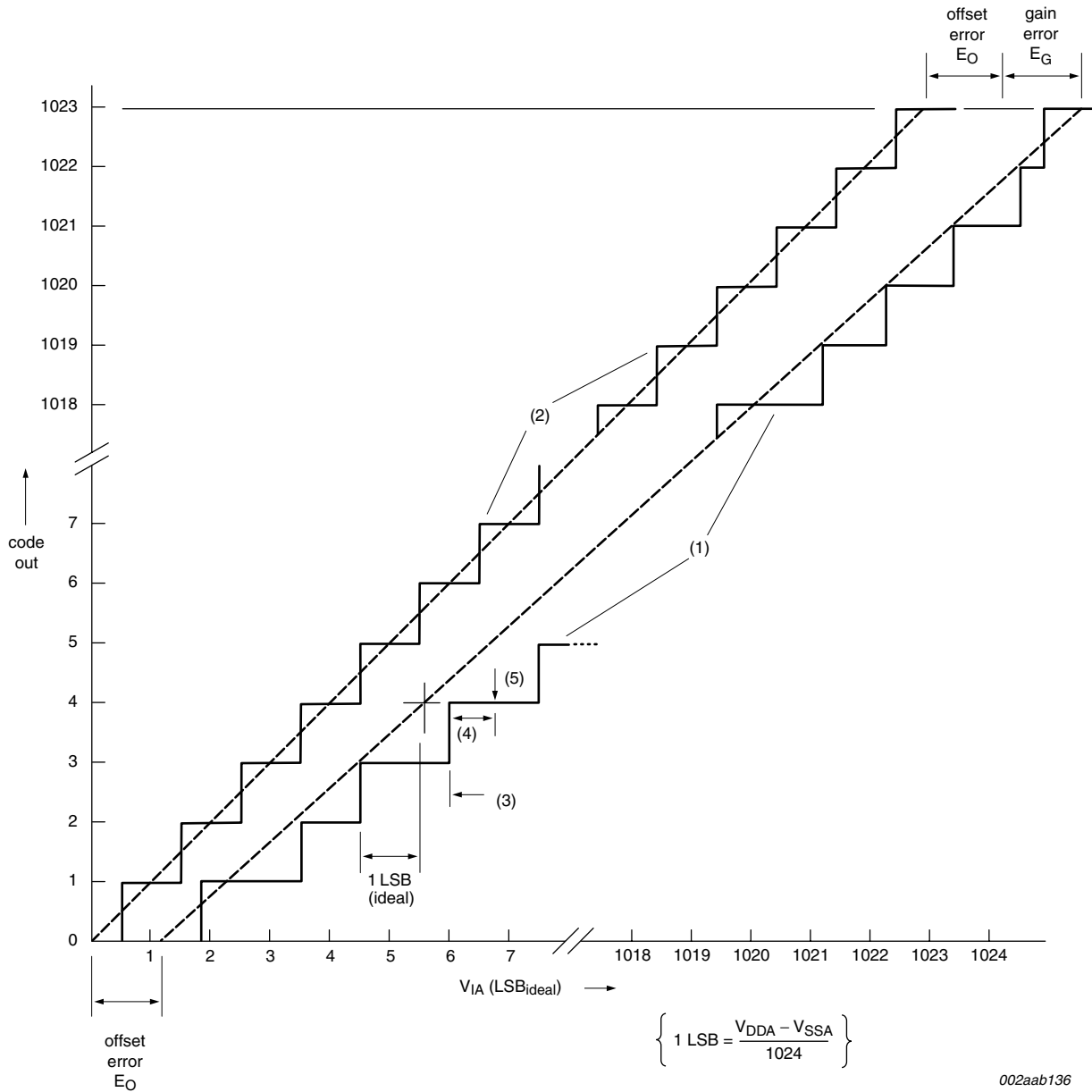
Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$C_{IN}$	transceiver capacitance	pin to GND	-	-	20	pF
$Z_{DRV}$ [9]	driver output resistance	steady state drive	29	-	44	$\Omega$
$Z_{PU}$	pull-up resistance	SoftConnect = ON	1.1	-	1.9	k $\Omega$

- [1] Typical ratings are not guaranteed. The values listed are at room temperature ( $+25\text{ }^\circ\text{C}$ ), nominal supply voltages.
- [2] The RTC typically fails when  $V_{BAT}$  drops below 1.6 V.
- [3] Including voltage on outputs in 3-state mode.
- [4]  $V_{DD}$  supply voltages must be present.
- [5] 3-state outputs go into 3-state mode when  $V_{DD}$  is grounded.
- [6] Accounts for 100 mV voltage drop in all supply lines.
- [7] Only allowed for a short time period.
- [8] Minimum condition for  $V_1 = 4.5\text{ V}$ , maximum condition for  $V_1 = 5.5\text{ V}$ .
- [9] Includes external resistors of  $18\text{ W} \pm 1\%$  on D+ and D-.

**Table 11: ADC static electrical characteristics** $V_{DDA} = 2.5\text{ V}$  to  $3.6\text{ V}$ ;  $T_a = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$  unless otherwise specified. ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IA}$	analog input voltage		0	-	$V_{DDA}$	V
$C_{ISS}$	analog input capacitance		-	-	1	pF
$E_D$	differential non-linearity		[1] [2] [3]	-	$\pm 1$	LSB
$E_{L(adj)}$	integral non-linearity		[1] [4]	-	$\pm 2$	LSB
$E_O$	offset error		[1] [5]	-	$\pm 3$	LSB
$E_G$	gain error		[1] [6]	-	$\pm 0.5$	%
$E_T$	absolute error		[1] [7]	-	$\pm 4$	LSB

- [1] Conditions:  $V_{SSA} = 0\text{ V}$ ,  $V_{DDA} = 3.3\text{ V}$ .
- [2] The ADC is monotonic, there are no missing codes.
- [3] The differential non-linearity ( $E_D$ ) is the difference between the actual step width and the ideal step width. See [Figure 4](#).
- [4] The integral non-linearity ( $E_{L(adj)}$ ) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See [Figure 4](#).
- [5] The offset error ( $E_O$ ) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See [Figure 4](#).
- [6] The gain error ( $E_G$ ) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See [Figure 4](#).
- [7] The absolute voltage error ( $E_T$ ) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See [Figure 4](#).



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- (1) Example of an actual transfer curve.
- (2) The ideal transfer curve.
- (3) Differential non-linearity (E<sub>D</sub>).
- (4) Integral non-linearity (E<sub>L(adj)</sub>).
- (5) Center of a step of the actual transfer curve.

Fig 4. ADC characteristics



## 9. Dynamic characteristics

**Table 12: Dynamic characteristics of USB pins (full-speed)**

$C_L = 50 \text{ pF}$ ;  $R_{PU} = 1.5 \text{ k}\Omega$  on  $D+$  to  $V_{3V3}$ ; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_r$	rise time	10 % to 90 %	4	-	20	ns
$t_f$	fall time	10 % to 90 %	4	-	20	ns
$t_{RFM}$	rise/fall time matching ( $t_r/t_f$ )		90	-	110	%
$V_{CRS}$	output signal crossover voltage		1.3	-	2.0	V
$t_{EOPT}$	source EOP width	see <a href="#">Figure 6</a>	160	-	175	ns
$t_{DEOP}$	differential data to EOP transition skew	see <a href="#">Figure 6</a>	-2	-	+5	ns
$t_{JR1}$	receiver data jitter tolerance to next transition		-18.5	-	+18.5	ns
$t_{JR2}$	receiver data jitter tolerance for paired transitions	10 % to 90 %	-9	-	+9	ns
$t_{EOPR1}$	EOP width at receiver <sup>[1]</sup>	must reject as EOP; see <a href="#">Figure 6</a>	40	-	-	ns
$t_{EOPR2}$	EOP width at receiver <sup>[1]</sup>	must accept as EOP; see <a href="#">Figure 6</a>	82	-	-	ns

[1] Characterized but not implemented as production set. Guaranteed by design.

**Table 13: Dynamic characteristics**

$T_a = 0 \text{ }^\circ\text{C}$  to  $+70 \text{ }^\circ\text{C}$  for commercial applications,  $-40 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$  for industrial applications,  $V_{DD}$  over specified ranges <sup>[1]</sup>

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
<b>External clock</b>						
$f_{osc}$	oscillator frequency		10	-	25	MHz
$T_{clk}$	oscillator clock period		40	-	100	ns
$t_{CHCX}$	clock HIGH time		$T_{clk} \times 0.4$	-	-	ns
$t_{CLCX}$	clock LOW time		$T_{clk} \times 0.4$	-	-	ns
$t_{CLCH}$	clock rise time		-	-	5	ns
$t_{CHCL}$	clock fall time		-	-	5	ns
<b>Port pins (except P0.2 and P0.3)</b>						
$t_{r(O)}$	output rise time		-	10	-	ns
$t_{f(O)}$	output fall time		-	10	-	ns
<b>I<sup>2</sup>C-bus pins (P0.2 and P0.3)</b>						
$t_{of}$	output fall time	$V_{IH}$ to $V_{IL}$	$20 + 0.1 \times C_b$ <sup>[2]</sup>	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance  $C_b$  in pF, from 10 pF to 400 pF.

### 9.1 Timing

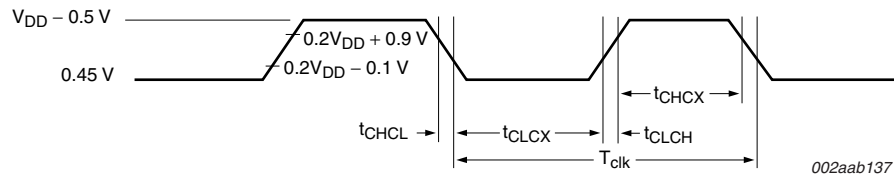


Fig 5. External clock timing

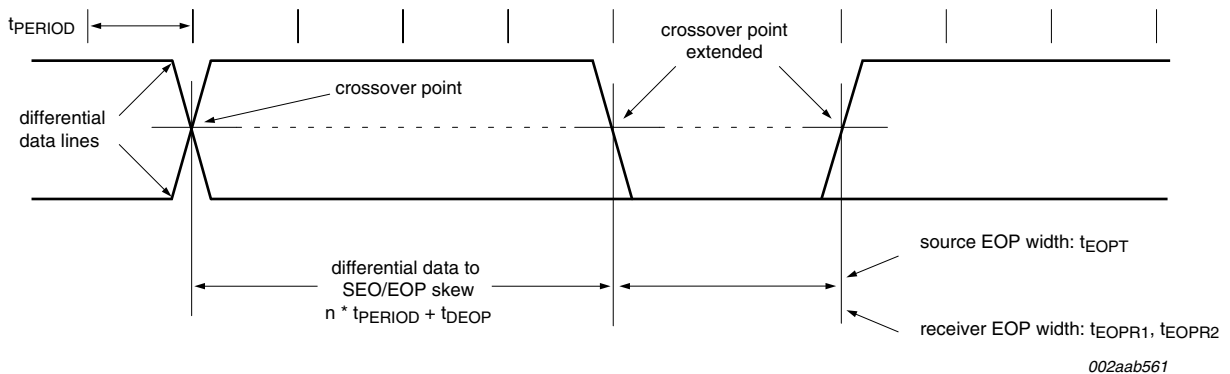


Fig 6. Differential data-to-EOP transition skew and EOP width

## 10. Application information

### 10.1 Suggested USB interface solutions

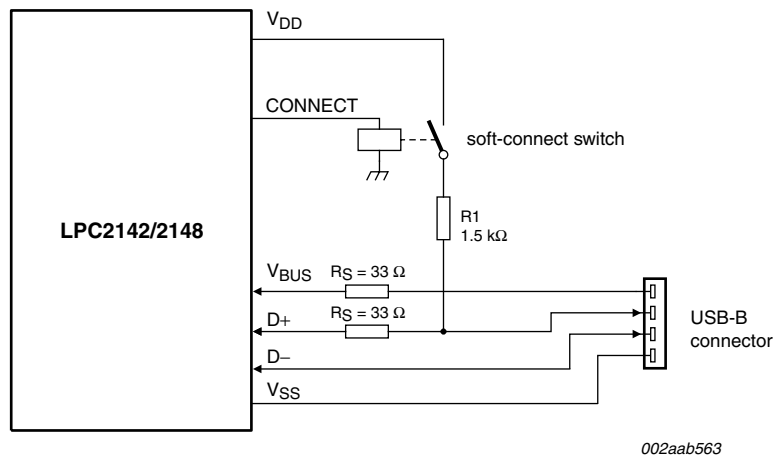


Fig 7. LPC2142/2148 USB interface using the CONNECT function on pin 17

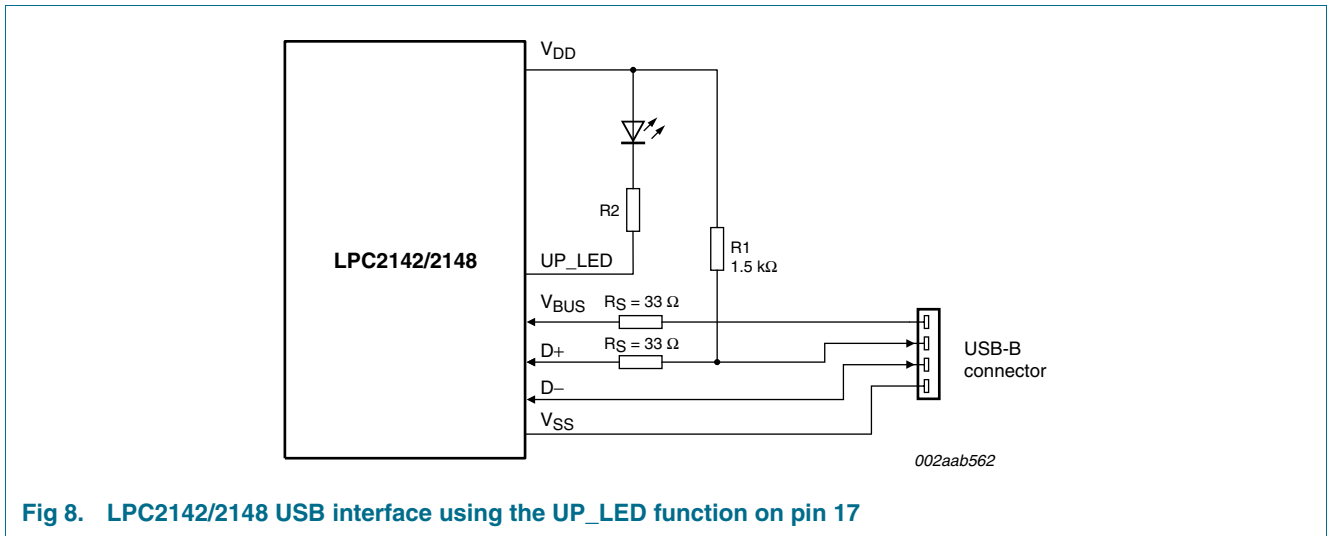


Fig 8. LPC2142/2148 USB interface using the UP\_LED function on pin 17

# 11. Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm

SOT314-2

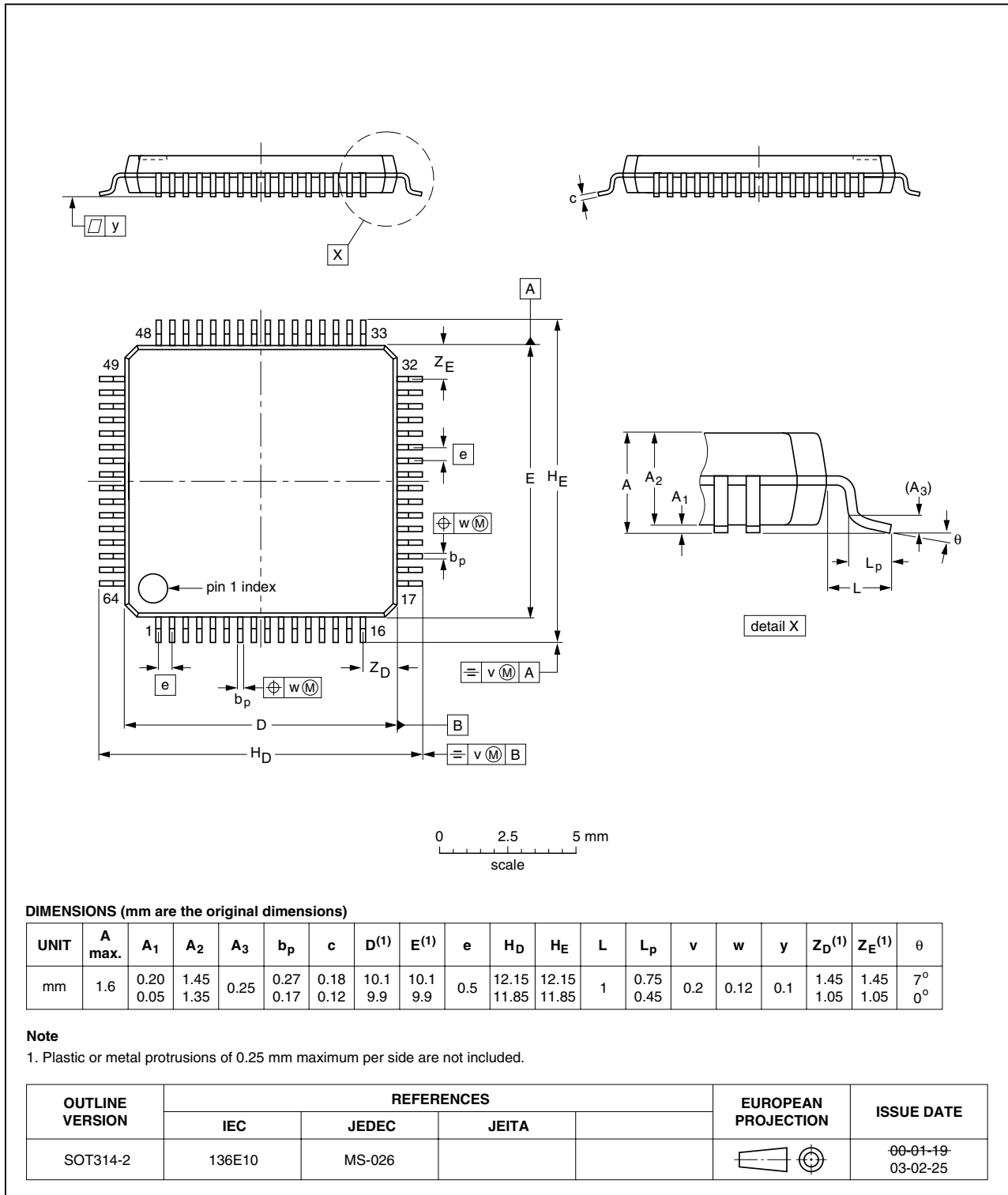


Fig 9. Package outline SOT314-2 (LQFP64)

## 12. Abbreviations

**Table 14: Acronym list**

Acronym	Description
ADC	Analog-to-Digital Converter
BOD	Brown-Out Detection
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DCC	Debug Communications Channel
DMA	Direct Memory Access
FIFO	First In, First Out
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulator
RAM	Random Access Memory
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSP	Synchronous Serial Port
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VPB	VLSI Peripheral Bus

## 13. Revision history

Table 15: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
LPC2142_2148_1	<tbd>	Preliminary data sheet	-	9397 750 14985	-

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Level	Data sheet status [1]	Product status [2] [3]	Definition
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