



15V/4A P-Channel Enhancement Mode Field Effect Transistor

General Description

The LPM3401 is the P-channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

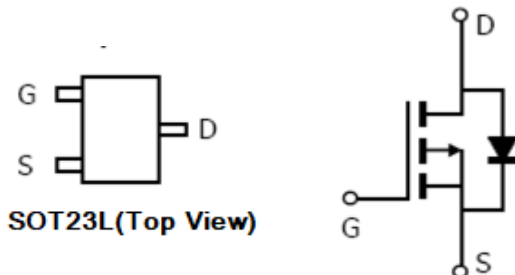
This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

Order Information

LPM3401 □ □ □
 F: Pb-Free
 Package Type
 B3: SOT23

Pin Configurations



Features

- ◆ -15V/-4.0A, $R_{DS(ON)} < 58m\Omega$ (typ.) @ $V_{GS} = -10V$
- ◆ -15V/-3.0A, $R_{DS(ON)} < 68m\Omega$ (typ.) @ $V_{GS} = -4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ SOT23 Package

Applications

- ✧ Portable Media Players/MP3 players
- ✧ Cellular and Smart mobile phone
- ✧ LCD
- ✧ DSC Sensor
- ✧ Wireless Card

Marking Information

Device	Marking	Package	Shipping
LPM3401		SOT23	3K/REEL
Y: Year code. W: Batch numbers			

Pin Description

Pin Number	Pin Description
1	Gate Pin
2	Source Pin
3	Drain Pin



Absolute Maximum Ratings

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-15	V
Gate-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current	$T_A = 25^\circ\text{C}$	I_D	-4	A
Pulsed Drain Current B		I_{DM}	-15	
Power Dissipation A	$T_A = 25^\circ\text{C}$	P_D	1.4	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal resistance ratings

Parameter	Symbol	Typ.	Max.	Units
Maximum Junction-to-Ambient	$R_{\theta JA}$	100	125	$^\circ\text{C/W}$





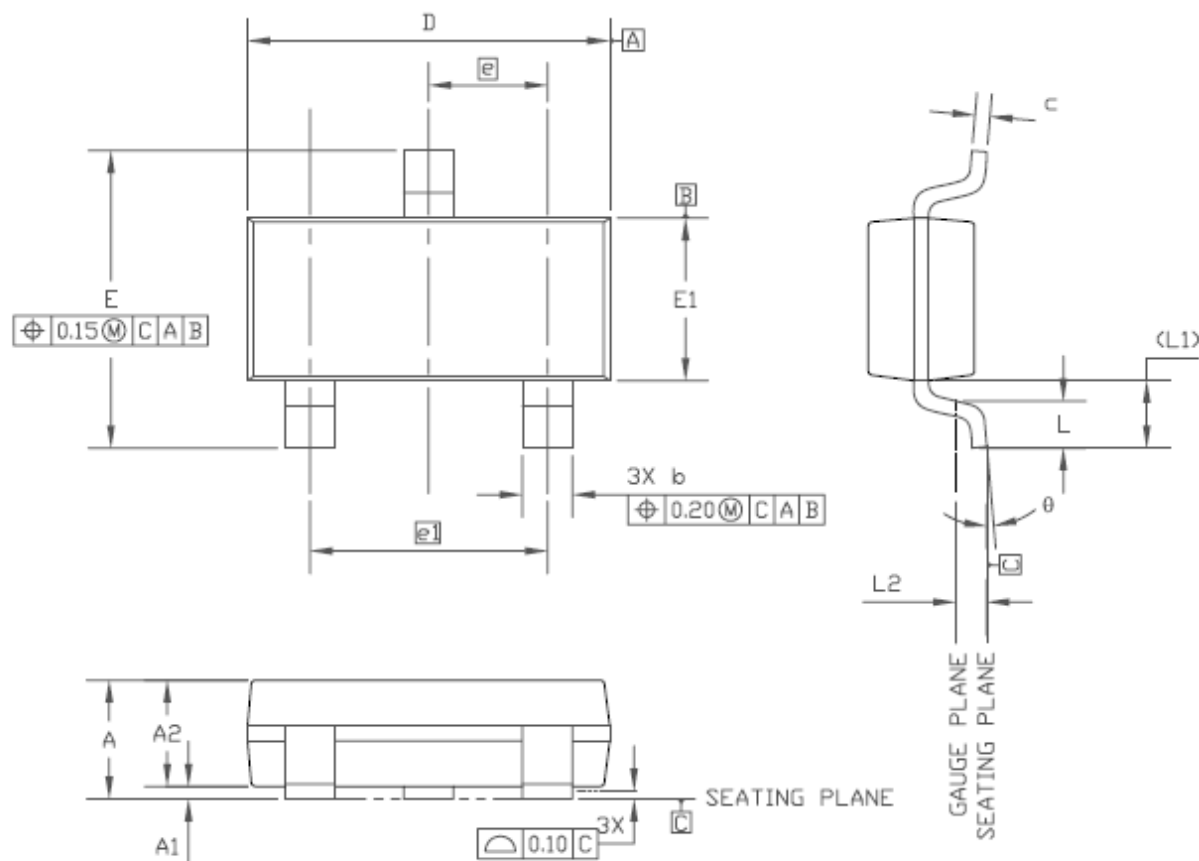
Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ.	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-15			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-12V, V _{GS} =0V T _J =55°C			-1 -10	uA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±12V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =-250μA	-0.6		-1.2	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-4A		55	58	mΩ
		V _{GS} =-4.5V, I _D =-3A		64	68	
		V _{GS} =-2.5V, I _D =-2A		85	95	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-4A		10		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.7	-1	V
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz		680		pF
C _{oss}	Output Capacitance			320		pF
C _{rss}	Reverse Transfer Capacitance			65		pF
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =-10V, V _{DS} =-15V, I _D =-4A		7		nC
Q _{gs}	Gate Source Charge			13		nC
Q _{gd}	Gate Drain Charge			1.8		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-15V, R _L =3.6Ω, R _{GEN} =6Ω		12	18	nS
t _r	Turn-On Rise Time			3	7	
t _{D(off)}	Turn-Off DelayTime			34	42	
t _f	Turn-Off Fall Time			3	7	

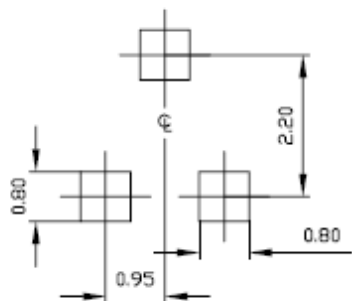


Packaging Information

SOT-23 STANDARD PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	1.17	0.030	—	0.046
A1	0.05	—	0.15	0.002	—	0.006
A2	0.70	0.85	1.02	0.028	0.033	0.040
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.20	0.003	—	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	2.10	—	2.64	0.083	—	0.104
E1	1.20	1.30	1.40	0.047	0.051	0.055
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.54 REF			0.021 REF		
L2	0.25			0.010		
θ1	0°	—	8°	0°	—	8°