30V/4A P-Channel Enhancement Mode Field Effect Transistor

General Description

The LPM9007 is the P-channel logic enhancement mode power field effect transistors are produced in using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage applications, notebook computer power management and other battery powered circuits where it is high-side switching.

Features

- -30V/-3.0A, RDC(ON)=52mΩ(typ.)@VGS=-4.5V
- ■ -30V/-3.0A,RDC(ON)=80mΩ(typ.)@VGS=-2.5V
- ■ Super high density cell design for extremely low RDC(ON)
- ■ SOT23 Package

Applications

- ✧ Portable Media Players
- ✧ Cellular and Smart mobile phone
- ✧ LCD
- ✧ DSC Sensor
- ✧ Wireless Card

Order Information

LPM9007 □ □ □

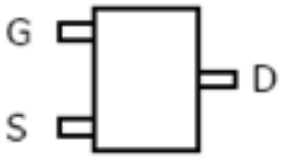
- F: Pb-Free
- Package Type
  - B3: SOT23-3

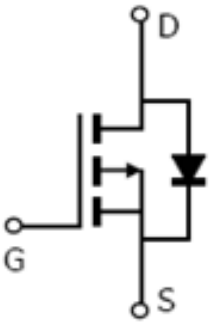
Marking Information

Device	Marking	Package	Shipping
LPM9007		SOT23-3	3K/REEL

Pin Configurations

TO-236
(SOT-23)
Top View





Absolute Maximum Ratings

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current A	T_A=25°C	I_D	-4.2	A
	T_A=70°C		-3.5	
Pulsed Drain Current B		I_{DM}	-30	
Power Dissipation A	T_A=25°C	P_D	1.4	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal resistance ratings

Parameter	Symbol	Typ. Max.	Units
Maximum Junction-to-Ambient	$R_{\theta JA}$	125	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ.	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250μA, V_{GS}=0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0V			-1	uA
		T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±12V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250μA	-0.7	-1	-1.3	V
$I_{D(ON)}$	On state drain current	V_{GS}=-4.5V, V_{DS}=-5V	-25			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-4.2A		42	50	mΩ
		(T_J=125°C)			75	
		V_{GS}=-4.5V, I_D=-4A		53	65	mΩ
		V_{GS}=-2.5V, I_D=-1A		80	120	mΩ
g_{FS}	Forward Transconductance	VDS=-5V, ID=-5A	7	11		S
V_{SD}	Diode Forward Voltage	IS=-1A,VGS=0V		-0.75	-1	V

I_S	Maximum Body-Diode Continuous Current				-2.2	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz		954		pF
C_{oss}	Output Capacitance			115		pF
C_{rss}	Reverse Transfer Capacitance			77		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		6		Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=-4.5V, V_{DS}=-15V, I_D=-4A		9.4		nC
Q_{gs}	Gate Source Charge			2		nC
Q_{gd}	Gate Drain Charge			3		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=3.6Ω, R_{GEN}=6Ω		6.3		nS
t_r	Turn-On Rise Time			3.2		
$t_{D(off)}$	Turn-Off DelayTime			38.2		
t_f	Turn-Off Fall Time			12		
t_{rr}	Body Diode Reverse Recovery Time	I_F=-4A, dI/dt=100A/μs		20.2		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-4A, dI/dt=100A/μs		11.2		nC

A: The value of R θJA is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T A =25°C. The value in any a given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The R θJA is the sum of the thermal impedence from junction to lead R θJL and lead to ambient.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using 80 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T A=25°C. The

SOA curve provides a single pulse rating.

Typical Characteristics

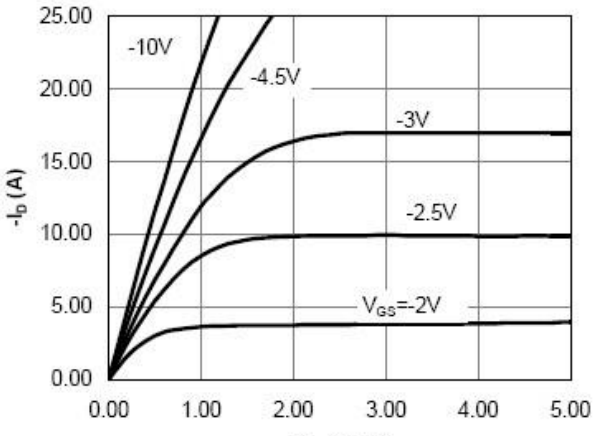


Fig 1: On-Region Characteristics

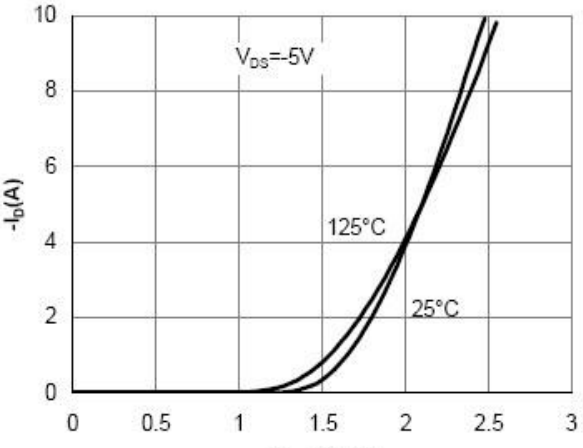


Figure 2: Transfer Characteristics

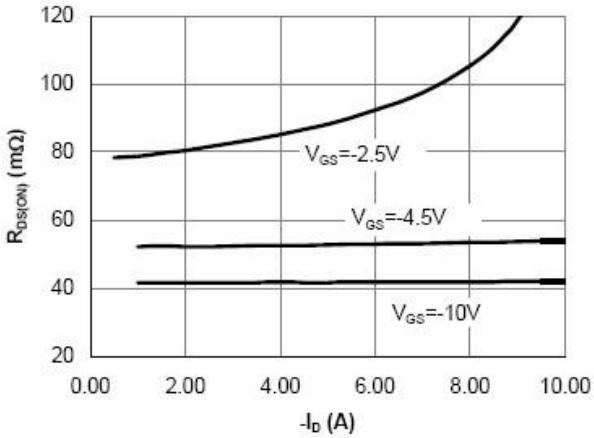


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

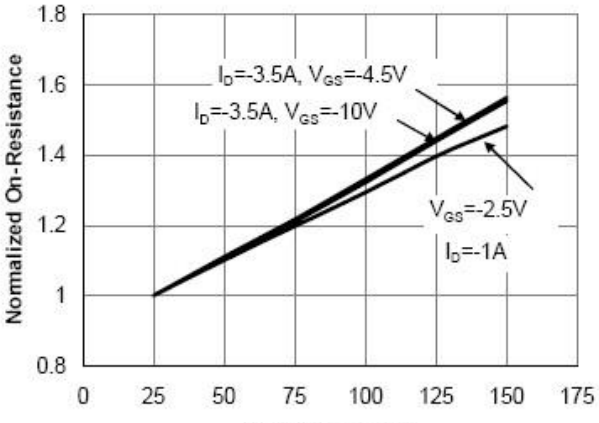


Figure 4: On-Resistance vs. Junction Temperature

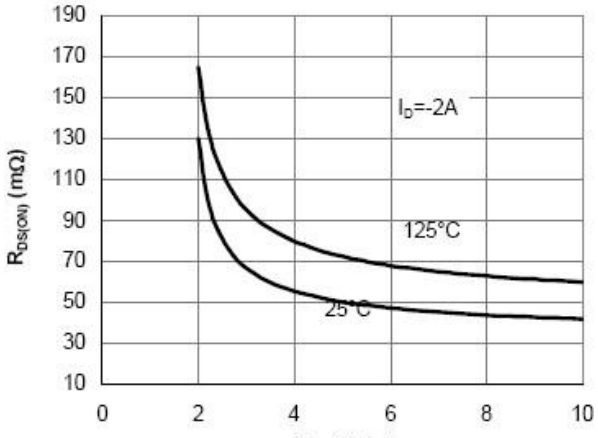


Figure 5: On-Resistance vs. Gate-Source Voltage

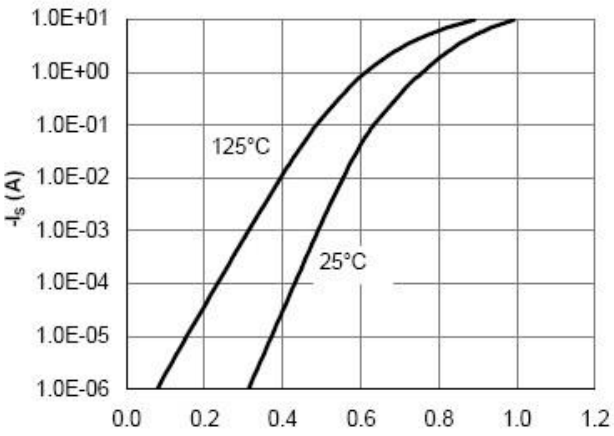


Figure 6: Body-Diode Characteristics

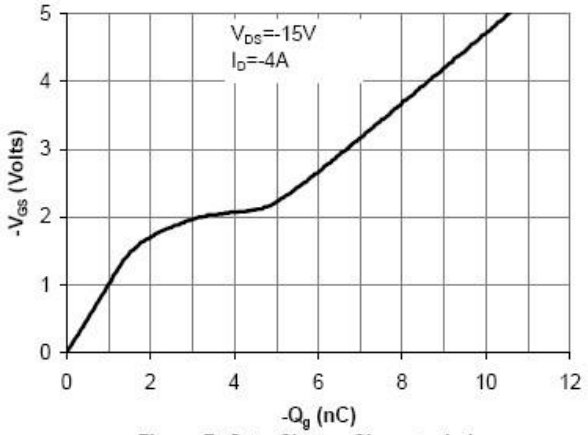


Figure 7: Gate-Charge Characteristics

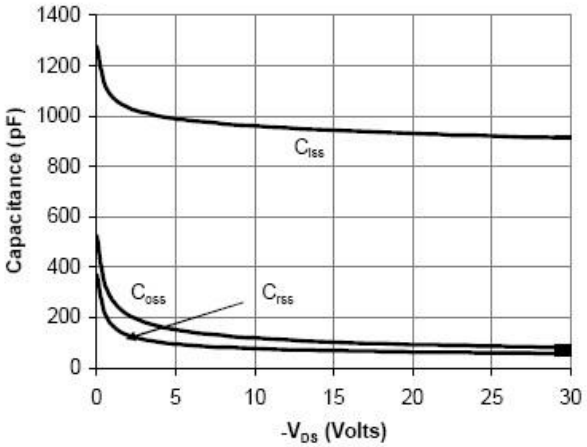


Figure 8: Capacitance Characteristics

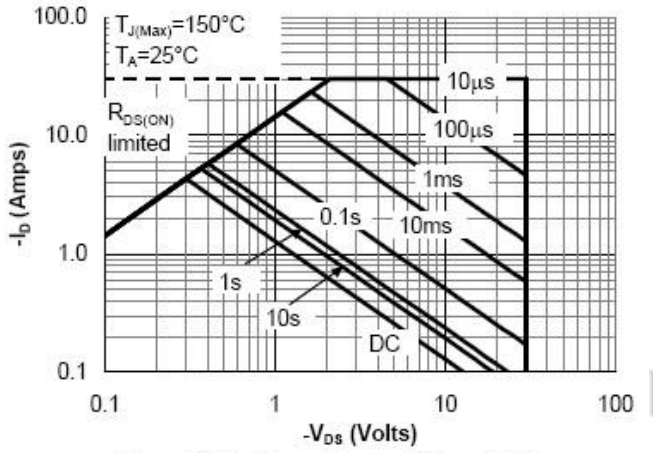


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

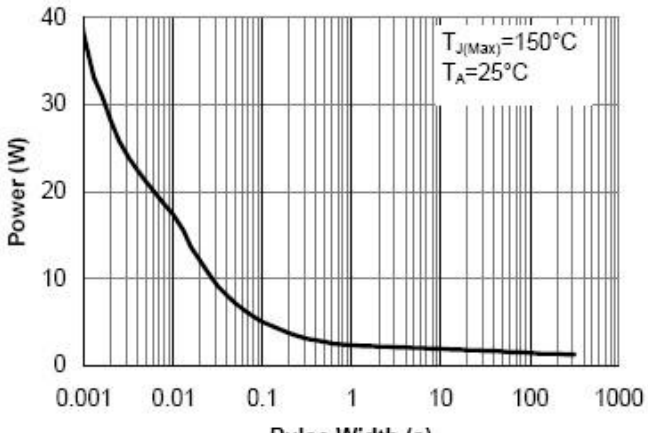


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

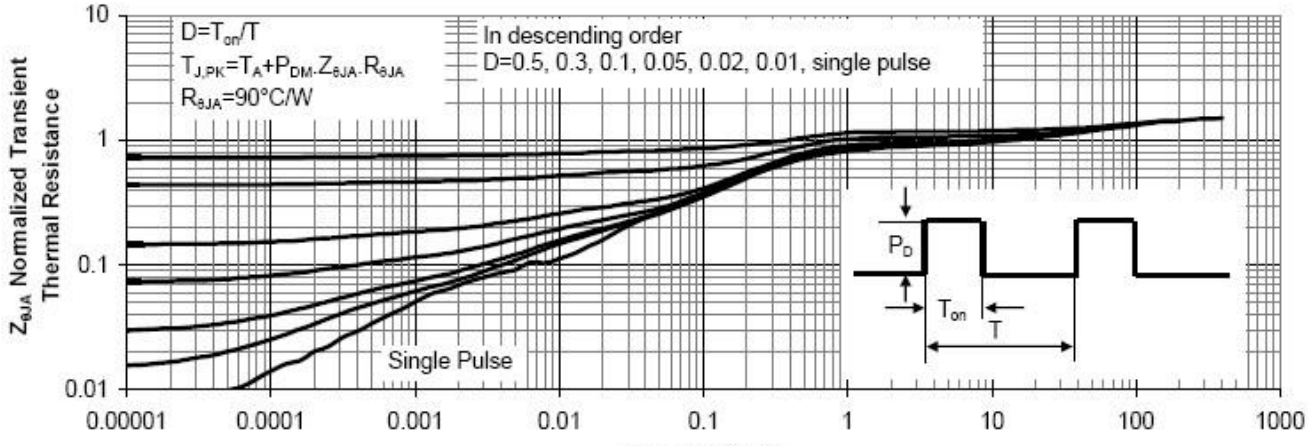
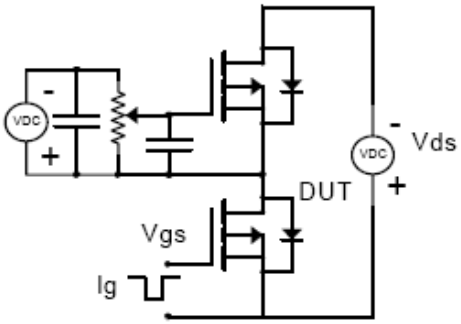
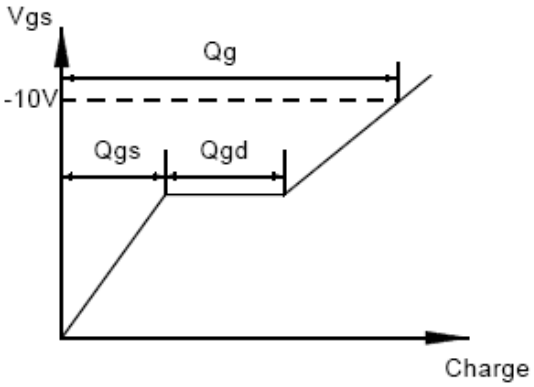


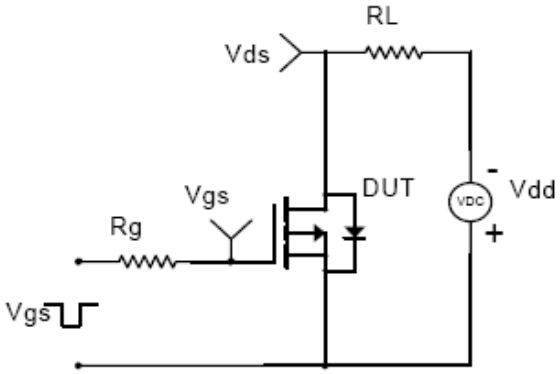
Figure 11: Normalized Maximum Transient Thermal Impedance

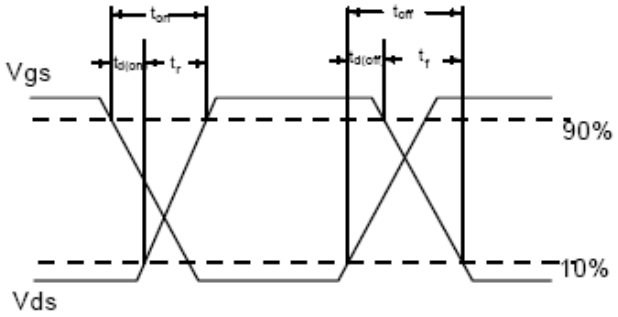
Gate Charge Test Circuit & Waveform



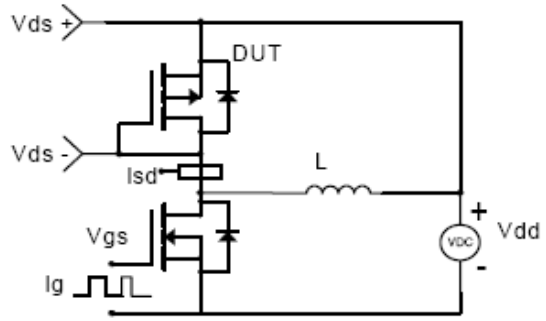


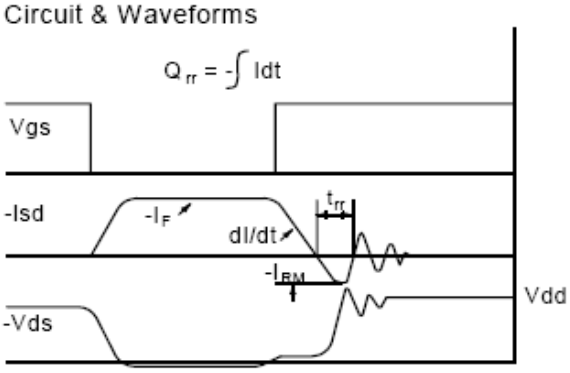
Resistive Switching Test Circuit & Waveforms





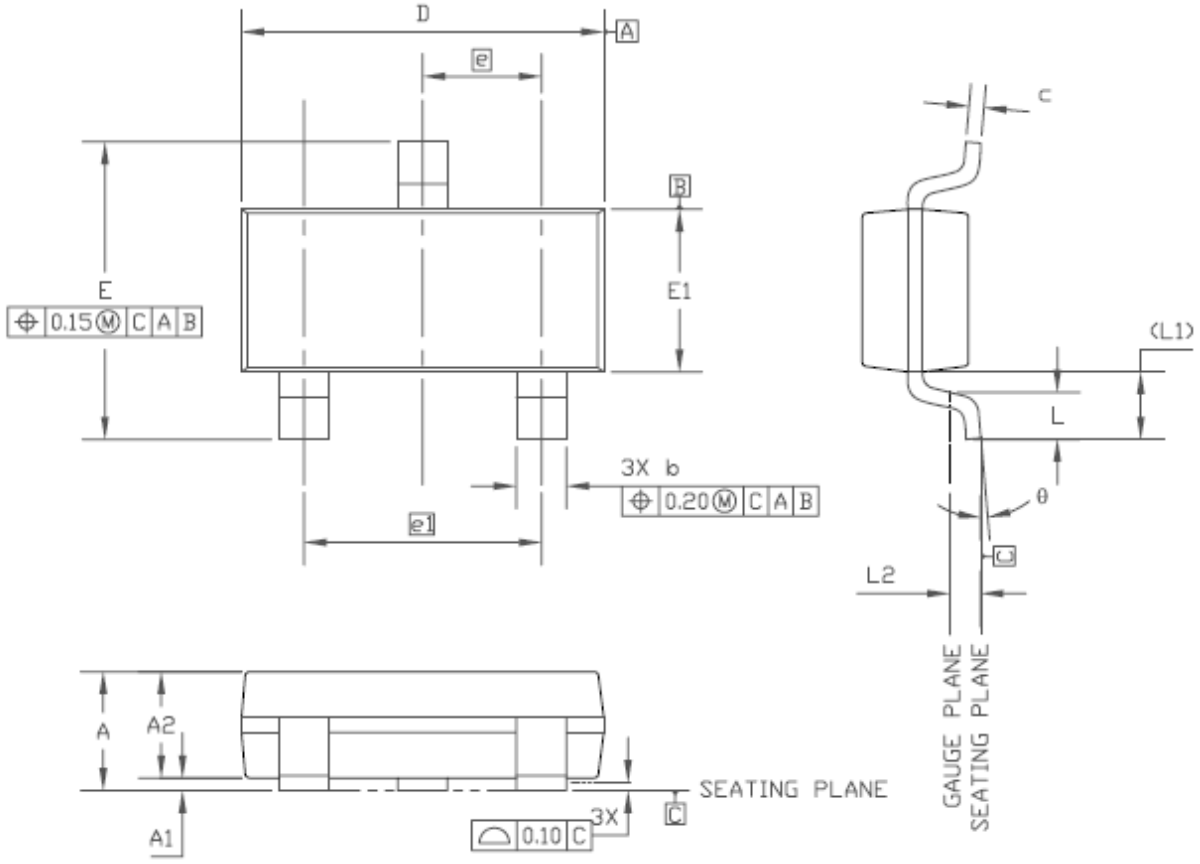
Diode Recovery Test Circuit & Waveforms



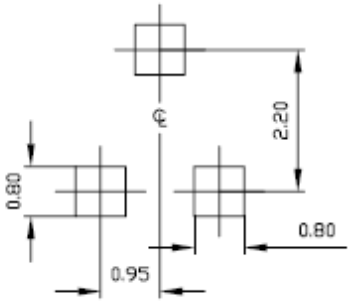


Package Information

SOT−23 STANDARD PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	1.17	0.030	—	0.046
A1	0.05	—	0.15	0.002	—	0.006
A2	0.70	0.85	1.02	0.028	0.033	0.040
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.20	0.003	—	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	2.10	—	2.64	0.083	—	0.104
E1	1.20	1.30	1.40	0.047	0.051	0.055
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.54 REF			0.021REF		
L2	0.25			0.010		
θ1	0°	—	8°	0°	—	8°