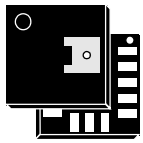
LPS001D

MEMS pressure sensor: 300 - 1100 mbar absolute digital output barometer

Preliminary data

Features

- Piezoresistive pressure sensor
- Very low power consumption
- 300 -1100 mbar absolute pressure range
- 0.1 mbar resolution
- Embedded offset and span temperature compensation
- Embedded 16-bit ADC
- SPI and I^2C interfaces
- Supply voltage: 2.2 V to 3.6 V
- 1.8 V compatible IOs
- High shock survivability (10000 *g*)
- Small, thin package
- ECOPACK® lead-free compliant



HLGA 5x5 16L

Applications

- Altimeter and barometer for portable devices
- GPS applications
- Weather station equipment
- Sport watches

Description

The LPS001D is an ultra-compact absolute piezoresistive pressure sensor. It includes a monolithic sensing element and an IC interface capable of taking information from the sensing element and providing a digital signal to external applications.

The sensing element consists of a suspended membrane within a single monosilicon substrate, manufactured using a dedicated process developed by STMicroelectronics called “VENSENS”.

The VENSENS process allows the construction of a monosilicon membrane above an air cavity with a controlled gap and defined pressure. The membrane is very small compared to traditional silicon micromachined membranes. Membrane breakage is prevented by intrinsic mechanical stoppers.

The IC interface is manufactured using a standard CMOS process that allows a high level of integration, to design a dedicated circuit which is trimmed to better match the sensing element characteristics. The LPS001D is available in a small plastic land grid array (LGA) package, and is guaranteed to operate over a temperature range extending from -40 °C to +85 °C. The package is holed to allow external pressure to reach the sensing element.

Table 1. Device summary

Order code	Temperature range [°C]	Package	Packing
LPS001DL	-40 to +85	HLGA 5x5 16L	Tray
LPS001DLTR	-40 to +85	HLGA 5x5 16L	Tape and reel

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1 Block diagram and pin information

Figure 1. Block diagram

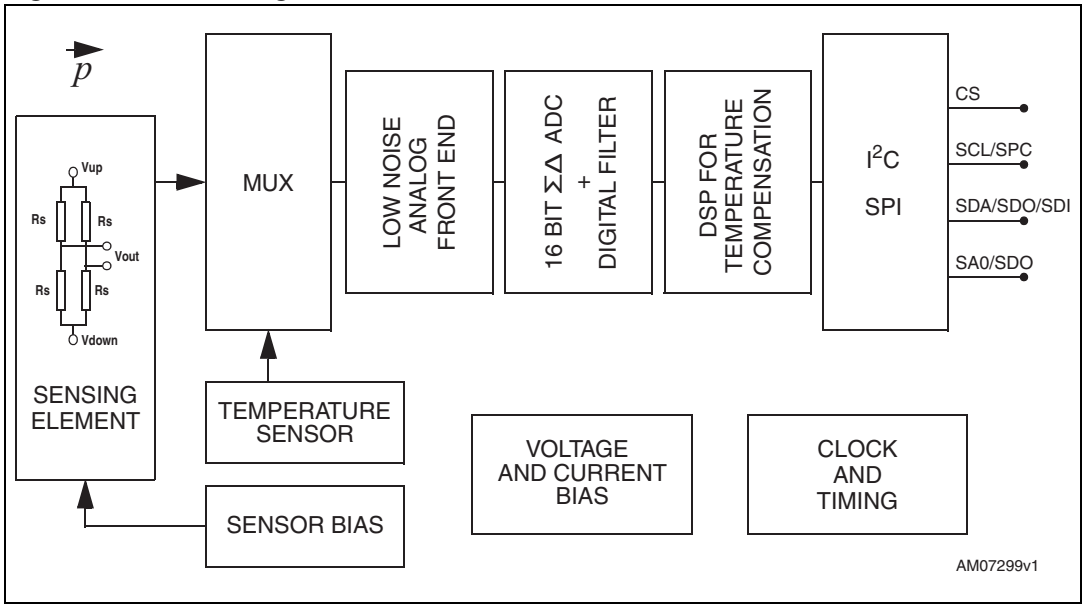


Figure 2. Pin connection

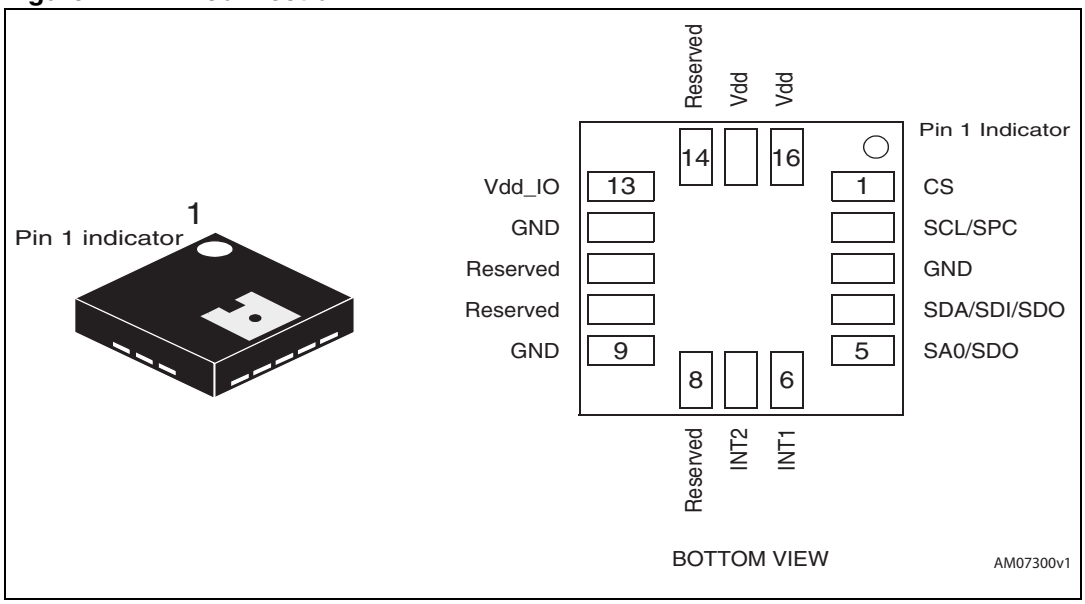


Table 2. Pin description

Pin #	Pin Name	Function
1	CS	SPI enable I^2C/SPI mode selection (logic 1: I^2C mode; logic 0: SPI enabled)
2	SCL/SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)

Table 2. Pin description (continued)

Pin #	Pin Name	Function
3	GND	0 V supply
4	SDA/ SDI/ SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	SA0/SDO	I^2C less significant bit of device slave address (SA0) SPI serial data output
6	INT1	Interrupt 1 (or data ready)
7	INT2	Interrupt 2 (or data ready)
8	Reserved	Leave unconnected
9	GND	0 V supply
10	Reserved	Connect to GND
11	Reserved	Connect to GND
12	GND	0 V supply
13	Vdd_IO	Power supply for I/O pads
14	Reserved	Connect to Vdd
15	Vdd	Power supply
16	Vdd	Power supply

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

Vdd = 2.5 V, T = 25 °C, unless otherwise noted.

Table 3. Mechanical characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
Pop	Operating pressure range		300		1100	mbar
Res(2)	Resolution in normal mode	P = 1013 mbar; T = 25 °C		0.1		mbar
	Resolution in low-power mode	P = 1013 mbar; T = 25 °C		0.13		
Acc	Accuracy	P = 300 to 1100 mbar; T = 25 °C		± 20		mbar
AccT	Accuracy over temperature range	P = 1013 mbar; T = 25 °C to +60 °C		±1.5(3)		mbar
		P = 1013 mbar; -40 °C < T < 25 °C or 60 °C < T < 85 °C		0.5		mbar/°C
PSo	Pressure sensitivity			16		LSb/mbar
TSo	Temperature sensitivity			64		LSb/°C

1. Typical specifications are not guaranteed.
2. Parameter given as standard deviation value.
3. Overall pressure drift in the range from 25 °C to 60 °C.

2.2 Electrical characteristics

Vdd = 2.5 V, T = 25 °C, unless otherwise noted.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		2.2		3.6	V
Vdd_IO	I/O supply voltage		1.7		Vdd+0.1	V
Idd	Supply current	Continous mode ODR_P = 7 Hz ODR_T = 1 Hz		190		µA
		During conversion		400		
IddLpr	Supply current in low-power mode	Continous mode ODR_P = 7 Hz ODR_T = 1 Hz		120		µA
IddPdn	Supply current in power-down mode			5		µA
ODR_P	Pressure output data rate(2)			7	12.5	Hz
ODR_T	Temperature output data rate(2)		1	7	12.5	Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. For pressure and temperature output data rate configurations, refer to *Table 17*.

3 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 6	V
Vdd_IO	I/O pins supply voltage	-0.3 to 6	V
Vin	Input voltage on any control pin	-0.3 to Vdd +0.3	V
P	Overpressure	12	bar
T_{STG}	Storage temperature range	-40 to +125	°C

This is a mechanical shock-sensitive device. Improper handling can cause permanent damage to the part.

This is an ESD sensitive device. Improper handling can cause permanent damage to the part.

4 Functionality

The LPS001D is a high-resolution, digital-output pressure sensor packaged in an LGA holed package. The complete device includes a sensing element based on a piezoresistive Wheatstone bridge approach, and an IC interface capable of providing information from the sensing element to external applications as a digital signal.

4.1 Sensing element

An ST proprietary process is used to obtain a monosilicon µ-sized membrane for MEMS pressure sensors, without requiring substrate-to-substrate bonding.

When pressure is applied, membrane deflection induces an imbalance in the Wheatstone bridge piezoresistors, whose output signal is converted by the IC interface.

Intrinsic mechanical stoppers prevent breakage in case of pressure overstress, ensuring measurement repeatability.

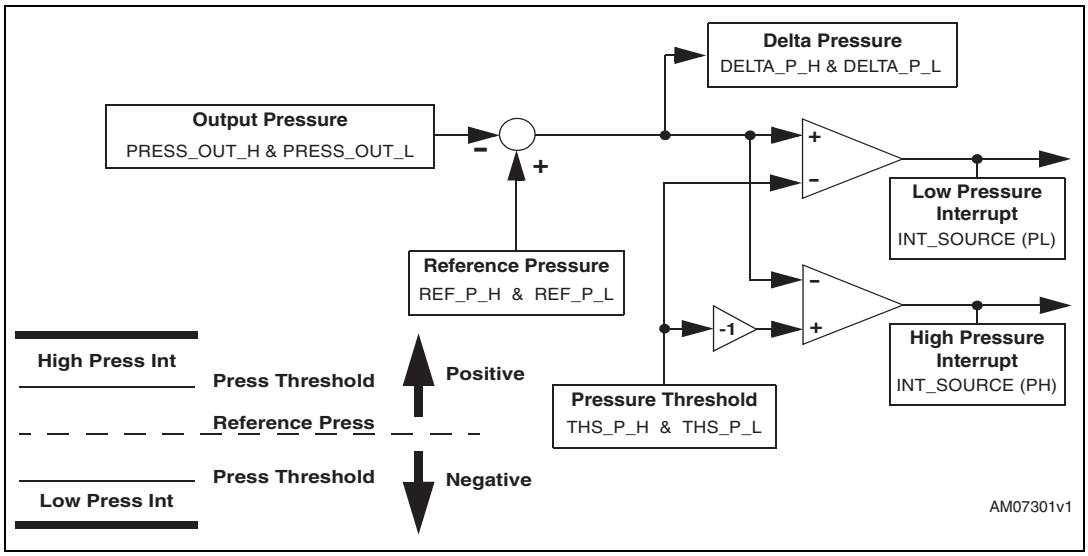
The pressure inside the buried cavity under the membrane is constant and controlled by process parameters.

To be compatible with traditional packaging technologies, a silicon holed cap is placed on top of the sensing element. During the moulding phase, this opening is covered by dedicated protection to avoid membrane blocking.

The package design leaves the holed cap exposed, allowing ambient pressure to reach the sensing element.

4.2 IC interface

Figure 3. Interrupt generation block and output pressure data.



The complete measurement chain consists of a low-noise capacitive amplifier, which converts the resistive imbalance of the MEMS sensor into an analog voltage signal, and an analog-to-digital converter, which translates the signal produced into a digital bitstream.

The converter is coupled with a dedicated reconstruction filter which removes the high frequency components of the quantization noise and provides low rate and high resolution digital words.

The pressure data can be accessed through an I^2C/SPI interface, thus making the device particularly suitable for direct interfacing with a microcontroller.

The device features two fully-programmable interrupt sources (*INT1* and *INT2*) which may be configured to trigger different pressure events. *Figure 3* shows the block diagram of the interrupt generation block and output pressure data.

The device may also be configured to generate, through interrupt pins, a Data Ready signal (*Drdy*) which indicates when new measured pressure data is available, thus simplifying data synchronization in digital systems.

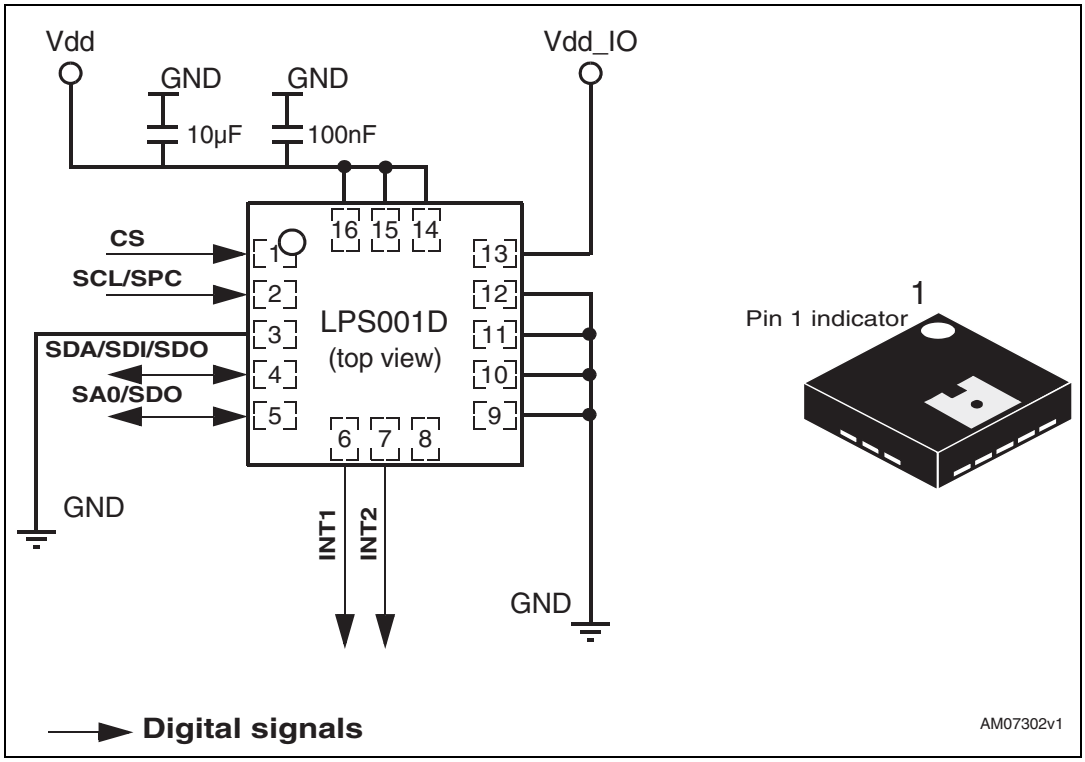
4.3 Factory calibration

The IC interface is factory-calibrated at two temperatures and two pressure levels for sensitivity and accuracy.

The trimming values are stored inside the device using a non-volatile structure. Each time the device is turned on, the trimming parameters are downloaded into the registers to be employed during normal operation. This allows the user to employ the device without requiring further calibration.

5 Application hints

Figure 4. LPS001D electrical connection



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to the supply pad of the device (common design practice).

All the voltage and ground supplies must be present at the same time to obtain proper behavior of the IC (refer to *Figure 4*). It is possible to remove the Vdd while maintaining Vdd_IO without blocking the communication busses. In this condition the measurement chain is powered off.

The functionality of the device and the measured data outputs are selectable and accessible through the I²C/SPI interface.When using the I²C, CS must be tied high.

The functions and the threshold of the two interrupt pins (INT 1 and INT 2) can be completely programmed by the user though the I²C/SPI interface.

5.1 Soldering information

The LGA package is compliant with the ECOPACK® standard. It is qualified for soldering heat resistance in accordance with JEDEC J-STD-020C.

Leave “Pin 1 indicator” unconnected during soldering.

6 Digital interfaces

The registers embedded in the LPS001D may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I^2C interface, the CS line must be tied high (i.e connected to Vdd_IO).

Table 6. Serial interface pin description

Pin name	Pin description
CS	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
SCL/SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI/SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SA0/SDO	I^2C less significant bit of device slave address (SA0) SPI serial data output (SDO)

6.1 I^2C serial interface

The LPS001D I^2C is a bus slave. The I^2C is employed to write the data into the registers whose content can also be read back.

The relevant I^2C terminology is provided in the table below:

Table 7. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines are connected to Vdd_IO through a pull-up resistor embedded inside the LPS001D. When the bus is free, both the lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards, as well as normal mode.

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the Master.

The Slave ADdress (SAD) associated with the LPS001D is 101110xb. The SDO pad can be used to modify the less significant bit of the device address. If the SDO pad is connected to the voltage supply, LSb is '1' (address 1011101b). Otherwise, if the SDO pad is connected to ground, the LSb value is '0' (address 1011100b). This solution permits the connection and addressing of two different LPS001D devices to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is required to generate an acknowledge after each byte of data has been received.

The I²C embedded in the LPS001D behaves as a slave device and the protocol which follows must be adhered to. After the start condition (ST) a slave address is sent (SAD + R/W). Once a slave acknowledge (SAK) has been returned, an 8-bit sub-address is transmitted (SUB): the 7 LSb represent the actual register address, while the MSB enables address auto-increment. If the MSb of the SUB field is '1', the SUB (register address) is automatically incremented to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (write) the Master transmits to the slave with direction unchanged. *Table 8* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 8. SAD+read/write patterns

Command	SAD[6:1]	SAD[0] = SDO	R/W	SAD+R/W
Read	101110	0	1	10111001 (39h)
Write	101110	0	0	10111000 (38h)
Read	101110	1	1	10111011 (3Bh)
Write	101110	1	0	10111010 (3Ah)

Table 9. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 10. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 11. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 12. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the clock line (SCL) LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The Master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, to increment the register address it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to read.

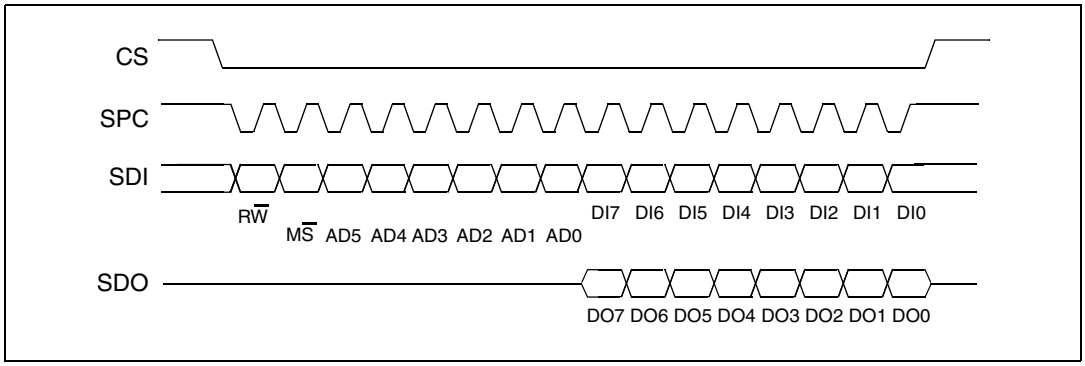
In the communication format presented, MAK is *master acknowledg*e and NMAK is *no master acknowledge*.

6.2 SPI bus interface

The LPS001D SPI is a bus slave. The SPI allows writing and reading of the registers of the device.

The serial interface interacts with external applications with 4 wires: CS, SPC, SDI and SDO.

Figure 5. Read and write protocol



CS is the serial port enable and is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. SPC is the serial port clock and is controlled by the SPI master. It is stopped high when CS is high (no transmission). SDI and SDO are respectively the serial port data input and output. These lines are driven at the falling edge of SPC and should be captured at the rising edge of SPC.

Both the read register and write register commands are completed in 16 clock pulses or in multiple of 8 in case of multiple byte read/write. Bit duration is the time between two falling edges of SPC. The first bit (bit 0) starts at the first falling edge of SPC after the falling edge of CS while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of CS.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives SDO at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address is auto-incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

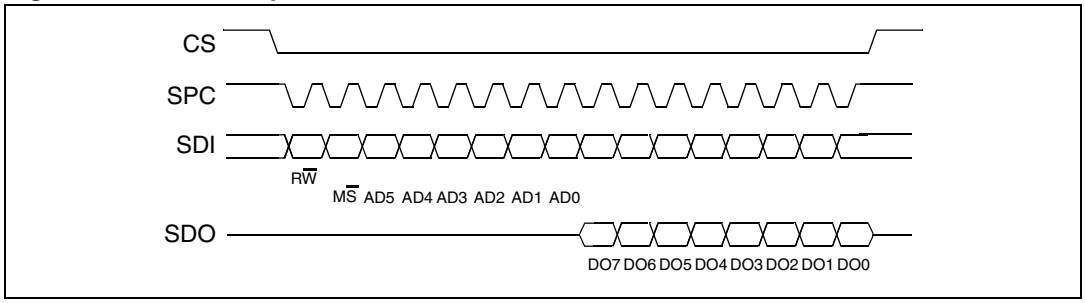
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods are added. When the M$\overline{S}$ bit is 0, the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is 1, the address used to read/write data is incremented at every block.

The function and the behavior of SDI and SDO remain unchanged.

6.2.1 SPI read

Figure 6. SPI read protocol



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: READ bit. The value is 1.

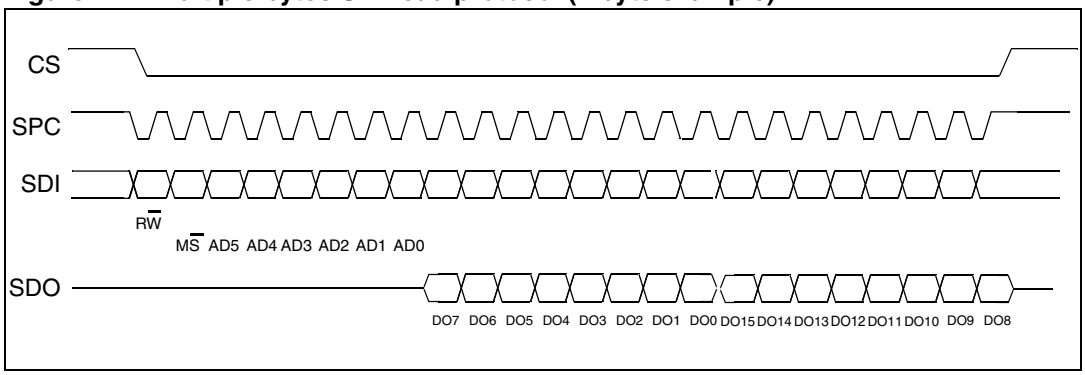
bit 1: MS bit. When 0, do not increment the address; when 1, increment the address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

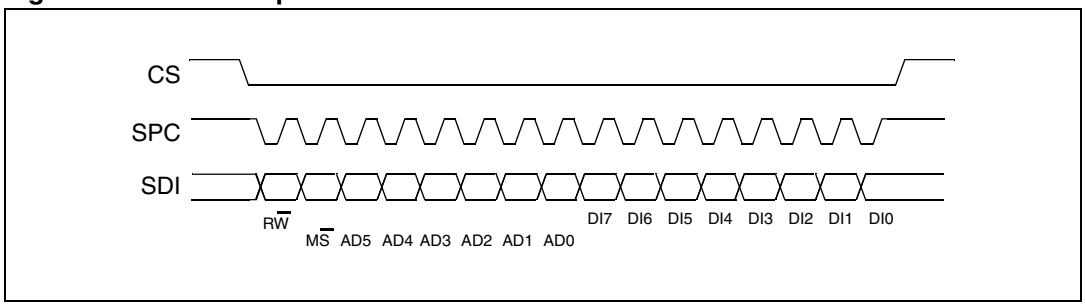
bit 16-... : data DO(...-8). Further data in multiple byte reading.

Figure 7. Multiple bytes SPI read protocol (2 byte example)



6.2.2 SPI write

Figure 8. SPI write protocol



The SPI write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

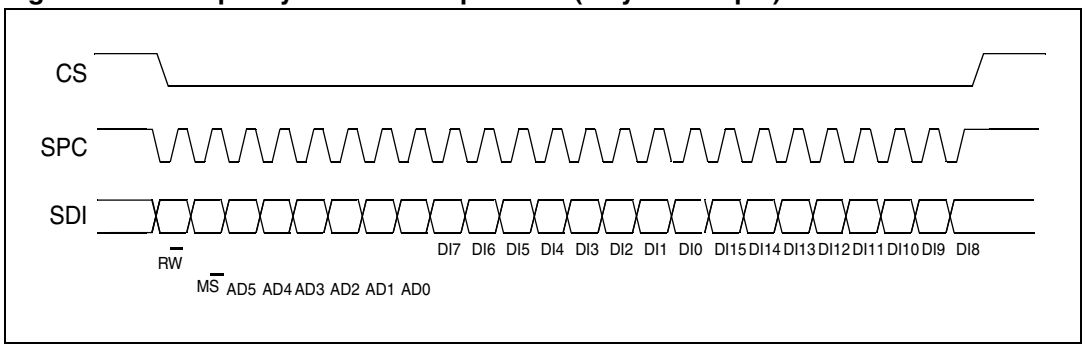
bit 1: MS bit. When 0, do not increment address; when 1, increment the address in multiple writing.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writing.

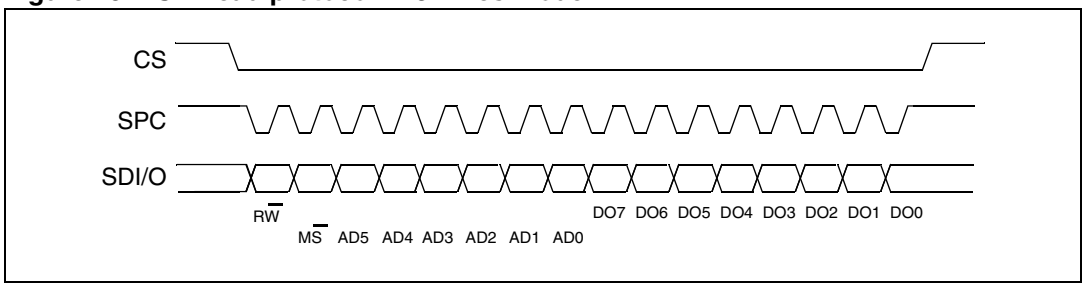
Figure 9. Multiple bytes SPI write protocol (2 byte example)



6.2.3 SPI read in 3-wires mode

3-wires mode is entered by setting to 1 the bit SIM (SPI serial interface mode selection) in the internal control register.

Figure 10. SPI read protocol in 3-wires mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: MS bit. When 0, do not increment the address; when 1, increment the address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

Multiple read command is also available in 3-wires mode.

7 Register mapping

Table 13 below provides a listing of the 8-bit registers embedded in the device, and the related addresses.

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Table 13. Register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved (do not modify)		00-0E			Reserved
WHO_AM_I	r	0F	000 1111	10111010	Dummy register
Reserved (do not modify)		10-1F			Reserved
CTRL_REG1	rw	20	010 0000	00000000	
CTRL_REG2	rw	21	010 0001	00000000	
CTRL_REG3	rw	22	010 0010	00000000	
Reserved (do not modify)		23-26			Reserved
Status_Reg	r	27	010 0111	00000000	
PRESS_OUT_L	r	28	010 1000	output	
PRESS_OUT_H	r	29	010 1001	output	
TEMP_OUT_L	r	2A	010 1010	output	
TEMP_OUT_H	r	2B	010 1011	output	
DELTA_P_L	r	2C	010 1100	output	
DELTA_P_H	r	2D	010 1101	output	
Reserved (do not modify)		2E-2F			Reserved
REF_P_L	rw	30	011 0000	00000000	
REF_P_H	rw	31	011 0001	00000000	
THS_P_L	rw	32	011 0010	00000000	
THS_P_H	rw	33	011 0011	00000000	
INTERRUPT_CFG	rw	34	011 0100	00000000	
INT_SOURCE	r	35	011 0101	output	
INT_ACK	r	36	011 0110		Dummy register
Reserved (do not modify)		37-3F			Reserved

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

8 Register description

The device contains a set of registers which are used to control its behavior and to retrieve pressure and temperature data. The register address, made up of 7 bits, is used to identify them and to read/write the data through the serial interface.

8.1 WHO_AM_I (0Fh)

Table 14. WHO_AM_I (0Fh) register

1	0	1	1	1	0	1	0

Device identification register.

This read-only register contains the device identifier that, for the LPS001D, is set to BAh.

8.2 CTRL_REG1 (20h)

Table 15. CTRL_REG1 (20h) register

LOWPWR	PD	ODR1	ODR0	DIFF_EN	BDU	BLE	SIM

Table 16. CTRL_REG1 (20h) register description

LOWPOW	Low power functionality. Default value: 0 (0: normal mode; 1: low-power activated)
PD	Power down control. Default value: 0 (0: power-down mode; 1: active mode)
ODR1 ODR0	Output data rate selection. Default value: 00 (see *Table 17*)
DIFF_EN	Interrupt circuit enable. Default value: 0 (0: interrupt generation disabled; 1: interrupt circuit enabled)
BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB reading)
BLE	Big/little endian selection. Default value: 0 (0: little endian; 1: big endian)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)

The **LOWPWR** bit is used to modify resolution and power consumption. In default mode this bit is ‘0’ and processing is done in normal mode with high resolution. When this bit is set to ‘1’ the device operates in low-power mode with lower resolution.

The **PD** bit is used to turn on the device. The device is in power-down mode when PD = '0' (default value after boot). The device is active when PD is set to '1'.

The **ODR1 - ODR0** bits change the output data rates of pressure and temperature samples. The default value is "00", which corresponds to a data rate of 7 Hz for pressure output and 1 Hz for temperature output. ODR1 and ODR2 bits can be configured as described in *Table 17*.

Table 17. Output data rate bit configurations

ODR1(1)	ODR0(1)	Pressure output data rate	Temperature output data rate
0	0	7 Hz	1 Hz
0	1	7 Hz	7 Hz
1	1	12.5 Hz	12.5 Hz

1. "10" bit configuration is not allowed and may cause incorrect device functionality.

The **DIFF_EN** bit is used to enable the circuitry for the computing of delta pressure output, DELTA_P. In default mode (DIFF_EN = '0'), this circuitry is turned off. It is recommended to turn on the circuitry only after the configuration of REF_P_L, REF_P_H, THS_P_L and THS_P_H registers, which are used by the circuitry.

The **BDU** bit is used to inhibit the update of output registers between the reading of upper and lower register parts. In default mode (BDU = '0'), the lower and upper register parts are updated continuously. If it is not certain that it can read faster than the output data rate, it is recommended to set the BDU bit to '1'. In this way, after the reading of the lower (upper) register part, the content of that output register is not updated until the upper (lower) part is read also. This feature prevents reading LSB and MSB related to different samples.

The **BLE** bit is used to select big endian or little endian representation for output registers. In the big endian representation, MSB values are located in PRESS_OUT_L (pressure), TEMP_OUT_L (temperature) and DELTA_P_L (delta pressure), while LSB values are located in PRESS_OUT_H, TEMP_OUT_H and DELTA_P_H. In little endian representation, the order is inverted (refer to data register description for more details).

The **SIM** bit selects the SPI serial interface mode. When SIM is '0' (default value), the 4-wire interface mode is selected and data coming from the device are sent to pin #4 (SDO). In 3-wire interface mode, output data are sent to pin #5 (SDI/SDO).

8.3 CTRL_REG2 (21h)

Table 18. CTRL_REG2 (21h) register

BOOT	X	X	X	X	X	X	0(1)

1. Bit to be kept to '0' for correct device functionality

Table 19. CTRL_REG2 (21h) register description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)

The **BOOT** bit is used to refresh the content of internal registers stored in the Flash memory block. At device power-up, the content of the Flash memory block is transferred to the internal registers related to trimming functions, to permit good behavior of the device. If for any reason the content of the trimming registers was changed, it is sufficient to use this bit to restore the correct values. When the BOOT bit is set to '1', the content of the internal Flash is copied within the corresponding internal registers and is used to calibrate the device. These values are factory trimmed and are different for every device. They permit good behavior of the device and normally do not need to be changed. At the end of the boot process, the BOOT bit is set again to '0'.

BOOT bit takes effect after one ODR clock cycle.

8.4 CTRL_REG3 [Interrupt CTRL register] (22h)

Table 20. CTRL_REG3 [Interrupt CTRL register] (22h) register

H_L active	PP_OD	Int2_cfg3	Int2_cfg2	Int2_cfg1	Int1_cfg3	Int1_cfg2	Int1_cfg1

Table 21. CTRL_REG3 [Interrupt CTRL register] (22h) register description

H_L active	Interrupt active high, low. Default value: 0 (0: active high; 1: active low)
PP_OD	Push-pull/open drain selection on interrupt pads. Default value: 0 (0: push-pull; 1: open drain)
Int2_cfg3 Int2_cfg2 Int2_cfg1	Data signal on INT2 pad control bits. Default value: 000 (see *Table 22*)
Int1_cfg3 Int1_cfg2 Int1_cfg1	Data signal on INT1 pad control bits. Default value: 000 (see *Table 22*)

Table 22. Data signal on INT1(2) pad control bits

Int1(2)_cfg3(1)	Int1(2)_cfg2(1)	Int1(2)_cfg1(1)	INT1(2) Pad
0	0	0	GND
0	0	1	Pressure High (P_high)
0	1	0	Pressure Low (P_low)
0	1	1	P_low OR P_high
1	0	0	Pressure Data Ready (Drdy)
1	1	1	Tri-state

1. These are the allowed bit configurations.

8.5 STATUS_REG (27h)

Table 23. STATUS_REG (27h) register

0	0	P_OR	T_OR	0	0	P_DA	T_DA

Table 24. STATUS_REG (27h) register description

P_OR	Pressure data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for pressure has overwritten the previous data)
T_OR	Temperature data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for temperature has overwritten the previous data)
P_DA	Pressure data available. Default value: 0 (0: new data for pressure is not yet available; 1: new data for pressure is available)
T_DA	Temperature data available. Default value: 0 (0: new data for temperature is not yet available; 1: new data for temperature is available)

The content of this register is updated every ODR cycle, regardless of the BDU value in CTRL_REG1.

P_DA is set to '1' whenever a new pressure sample is available. P_DA is cleared anytime PRESS_OUT_H (29h) register is read.

T_DA is set to '1' whenever a new temperature sample is available. T_DA is cleared anytime TEMP_OUT_H (2Bh) register is read.

The **P_OR** bit is set to '1' whenever new pressure data is available and P_DA was set in the previous ODR cycle and not cleared. P_OR is cleared anytime PRESS_OUT_H (29h) register is read.

T_OR is set to '1' whenever new temperature data is available and T_DA was set in the previous ODR cycle and not cleared. T_OR is cleared anytime TEMP_OUT_H (2Bh) register is read.

8.6 PRESS_OUT_L (28h)

Table 25. PRESS_OUT_L (28h) register

POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0

Table 26. PRESS_OUT_L (28h) register description

POUT7 - POUT0	Pressure data LSB (when BLE bit in CTRL_REG1 is set to '0', little endian)

Pressure data are expressed as absolute values. Values exceeding the operating pressure range (see *Table 3*) are clipped.

In big endian mode (BLE bit in CTRL_REG1 set to '1'), the content of this register is the MSB pressure data.

8.7 PRESS_OUT_H (29h)

Table 27. PRESS_OUT_H (29h) register

POUT15	POUT14	POUT13	POUT12	POUT11	POUT10	POUT9	POUT8

Table 28. PRESS_OUT_H (29h) register description

POUT15 - POUT8	Pressure data MSB (when BLE bit in CTRL_REG1 is set to '0')

In big endian mode (BLE bit in CTRL_REG1 set to '1') the content of this register is the LSB pressure data.

8.8 TEMP_OUT_L (2Ah)

Table 29. TEMP_OUT_L (2Ah) register

TOUT7	TOUT6	TOUT5	TOUT4	TOUT3	TOUT2	TOUT1	TOUT0

Table 30. TEMP_OUT_L (2Ah) register description

TOUT7 - TOUT0	Temperature data LSB (when BLE bit in CTRL_REG1 register is set to '0', little endian)

Temperature data are expressed as 2's complement numbers.

In big endian mode (BLE bit in CTRL_REG1 set to '1') the content of this register is the MSB temperature data.

8.9 TEMP_OUT_H (2Bh)

Table 31. TEMP_OUT_H (2Bh) register

TOUT15	TOUT14	TOUT13	TOUT12	TOUT11	TOUT10	TOUT9	TOUT8

Table 32. TEMP_OUT_H (2Bh) register description

TOUT8 - TOUT15	Temperature data MSB (when BLE bit in CTRL_REG1 register is set to '0')

Temperature data are expressed as 2's complement numbers.

In big endian mode (BLE bit in CTRL_REG1 set to '1') the content of this register is the LSB temperature data.

8.10 DELTA_P_L (2Ch)

Table 33. DELTA_P_L (2Ch) register

DP7	DP6	DP5	DP4	DP3	DP2	DP1	DP0

Table 34. DELTA_P_L (2Ch) register description

DP7 - DP0	Delta pressure data LSB (when BLE bit in CTRL_REG1 register is set to '0')

DELTA_P registers store a delta pressure representing the difference between a constant reference value, REF_P registers, and the actual pressure measured, PRESS_OUT registers.

In big endian mode (BLE bit in CTRL_REG1 set to '1') the content of this register is the MSB delta pressure data.

8.11 DELTA_P_H (2Dh)

Table 35. DELTA_P_H (2Dh) register

DP15	DP14	DP13	DP12	DP11	DP10	DP9	DP8

Table 36. DELTA_P_H (2Dh) register description

DP15 - DP8	Delta pressure data MSB (when BLE bit in CTRL_REG1 register is set to '0').

In big endian mode (BLE bit in CTRL_REG1 set to '1') the content of this register is the LSB delta pressure data.

8.12 REF_P_L (30h)

Table 37. REF_P_L (30h) register

REFL7	REFL6	REFL5	REFL4	REFL3	REFL2	REFL1	REFL0

Table 38. REF_P_L (30h) register description

REFL7 - REFL0	Reference pressure LSB data. Default value: 00h.

This register contains the lower part of the reference pressure for computing of delta pressure.

Full value is REF_P_H & REF_P_L and is represented as an unsigned number.

8.13 REF_P_H (31h)

Table 39. REF_P_H (31h) register

REFL15	REFL14	REFL13	REFL12	REFL11	REFL10	REFL9	REFL8

Table 40. REF_P_H (31h) register description

REFL15 - REFL8	Reference pressure MSB data. Default value: 00h.

This register contains the higher part of the reference pressure for computing of delta pressure.

Full value is REF_P_H & REF_P_L and is represented as an unsigned number.

8.14 THS_P_L (32h)

Table 41. THS_P_L (32h) register

THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 42. THS_P_L (32h) register description

THS7 - THS0	Threshold pressure LSB. Default value: 00h.

This register contains the low part of the threshold value for pressure interrupt generation. The complete threshold value is given by THS_P_H & THS_P_L and is expressed as an unsigned number.

8.15 THS_P_H (33h)

Table 43. THS_P_H (33h) register

THS15	THS14	THS13	THS12	THS11	THS10	THS9	THS8

Table 44. THS_P_H (33h) register description

THS15 - THS8	Threshold pressure MSB. Default value: 00h.

This register contains the high part of the threshold value for pressure interrupt generation. The complete threshold value is given by THS_P_H & THS_P_L and is expressed as an unsigned number.

8.16 INTERRUPT_CFG (34h)

Table 45. INTERRUPT_CFG (34h) register

X	X	X	X	X	LIR	PL_E	PH_E

Table 46. INTERRUPT_CFG (34h) register description

LIR	Latch interrupt request into INT_SOURCE register. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
PL_E	Enable interrupt generation on delta pressure low event. Default value: 0. (0: disable interrupt request; 1: enable interrupt request on measured delta pressure value lower than preset threshold)
PH_E	Enable interrupt generation on delta pressure high event. Default value: 0 (0: disable interrupt request; 1:enable interrupt request on measured delta pressure value higher than preset threshold)

Interrupt configuration register.

8.17 INT_SOURCE (35h)

Table 47. INT_SOURCE (35h) register

0	0	0	0	0	IA	PL	PH

Table 48. INT_SOURCE (35h) register description

IA	Interrupt active. (0: no interrupt has been generated; 1: one or more interrupt events have been generated).
PL	Delta pressure low. (0: no interrupt has been generated; 1: Low delta pressure event has occurred).
PH	Delta pressure high. (0: no interrupt has been generated; 1: High delta pressure event has occurred).

Interrupt source register. INT_SOURCE register is cleared by reading the INT_ACK register.

8.18 INT_ACK (36h)

Table 49. INT_ACK (36h) register

X	X	X	X	X	X	X	X

Dummy register. If the LIR bit in the INTERRUPT_CFG register is set to ‘1’, a reading at this address clears the INT_SOURCE register.

Read data are not significant.

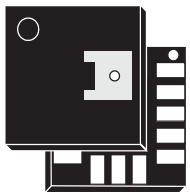
9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

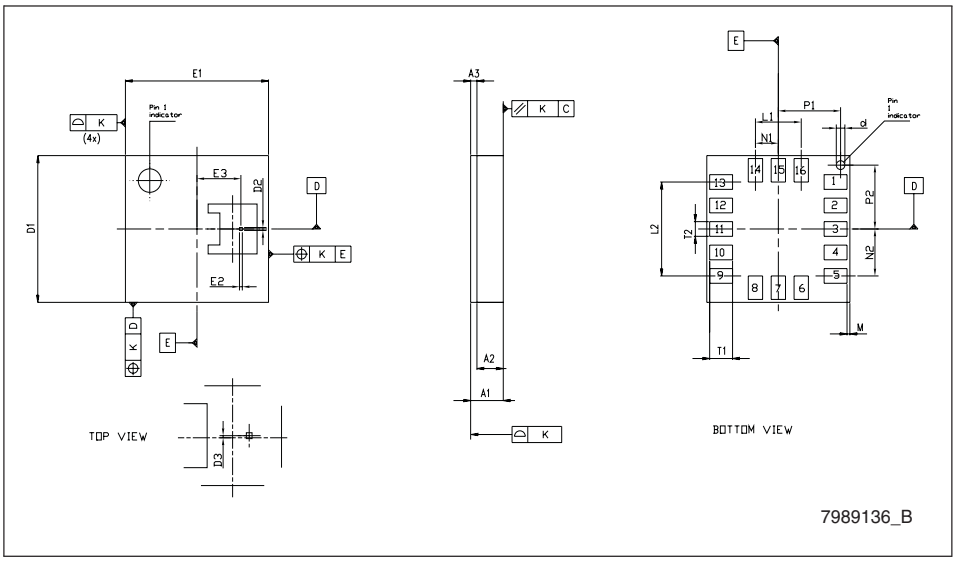
Figure 11. HLGA 5x5 16L: mechanical data and package dimensions

Dimensions			
Ref.	mm		
	Min.	Typ.	Max.
A1			1
A2		0.700	
A3		0.200	
D1	4.850	5.000	5.150
D2		0.100	
D3		0	
d		0.200	
E1	4.850	5.000	5.150
E2		0.100	
E3		1.530	
L1		1.600	
L2		3.200	
M		0.100	
N1		0.800	
N2		1.600	
P1		2.095	
P2		2.202	
T1		0.800	
T2		0.500	
K		0.050	

Outline and mechanical data



HLGA 5x5 16L
Land Grid Array Package



10 Revision history

Table 50. Document revision history

Date	Revision	Changes
17-Aug-2010	1	First release.

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