Product Specifications

Customer	**STANDARD**
Description	**3.45" TFT LCD Module**
Model Name	**LQ035WC115**
Date	**2005/02/09**
Doc. No.	
Revision	**02**

PRELIMINARY

Customer Approval	
Date	

The above signature represents that the product specifications, testing regulation, and warranty in the specifications are accepted

Approval		Design Engineering	
		Check	Design
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CONETNTS

RECORD OF REVISIONS

Revision No.	Revision Date	Page	Summary
02	2006/2/6	4	Modify the weight of general specifications from (350) to (32)
02	2006/2/6	4	Change Top and Tst
02	2006/2/6	18	Change viewing angle
02	2006/2/6	25	Add Quality Assurance

1. SUMMARY

This technical specification applies to 3.45“ color TFT-LCD panel. The 3.45“ color TFT-LCD panel is designed for camcorder, digital camera application and other electronic products which require high quality flat panel displays.

2. FEATURES

High Resolution :230,400 Dots (320 RGB x 240) . Image Reversion: Up/Down and Left/Right.

3. GENERAL SPECIFICATIONS

Parameter		Specifications	Unit
Screen size		3.45(Diagonal)	inch
Display Format		320 RGB x 240	Dot
Active area		70.08(H) x 52.56(V)	mm
Dot pitch		0.073(H) x 0.219(V)	mm
Surface treatment		Anti-glare	
Pixel Configuration		RGB-Stripe	
Outline dimension		76.9(W) x 63.9(H) x 3.3(D)	mm
Weight		(32)	g
View Angle direction		6 o’clock	
Temperature Range	Operation	-20~60	℃
	Storage	-30~70	℃

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power Voltage	V_{DD},V_{CC}	GND=0	-0.3	7.0	V	
	V_{GH}	GND=0	-0.3	32.0	V	
	V_{GL}	GND=0	-22.0	0.3	V	
	V_{GH} –V_{GL}	GND=0	-0.3	+45.0	V	
Input Signal Voltage	V_{in}	GND=0	-0.3	V_{DD}+0.3	V	
Logic Output Voltage	V_{OUT}	GND=0	-0.3	+0.7	V	

Note : Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

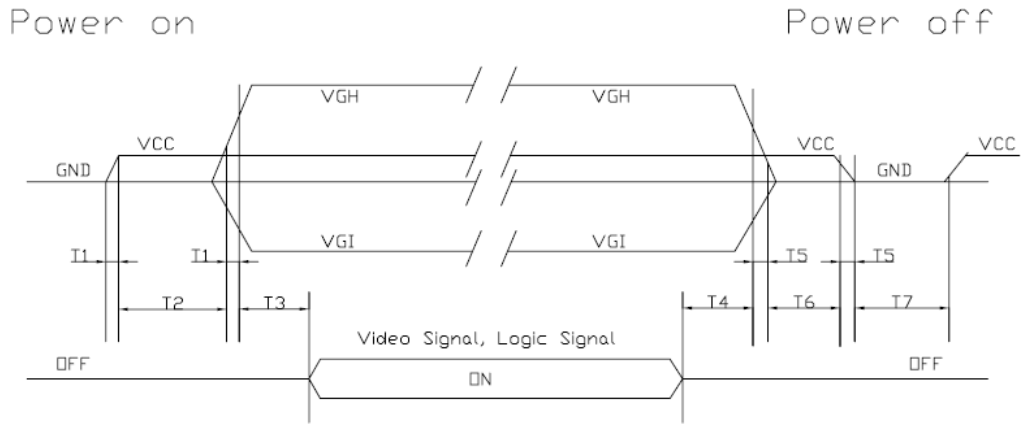
5. ELECTRICAL CHARACTERISTICS

5.1. Operating conditions :

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Power Voltage	VCC	3.0	3.3	3.6	V	
	VDD	3.8	5	5.5	V	
	VGH	10	-	30	V	
	VGL	-17	-	-5	V	
Low level input voltage	V_{IL}	0	-	0.3 VDD	V	SCL, SDI,UD,LRC,IF1,IF2
Hight level input voltage	V_{IH}	0.7 VDD	-	VDD	V	
Analog operating current	I_{VDD}	-	-	TBD	mA	f_{CLKIN}=27MHz,f_{OEH}=15.7KHz, VDDA=5V

5.2 Power Sequence

Sequence for power on/off and Signal on/off



T1≤ 15ms(From 10% VCC to 90%*VCC, when VCC is Low to High) ;
T2 ≤10ms(From 90% VCC to 10%*VCC, when VCC is Low to High) ;
T3 ≤10ms(From 90% VGH to Video signal, when VGH is Low to High) ;
T4 ≤10ms(From Video signal to 90%*VGH,, when VGH is High to Low) ;
T5 ≤20ms(From 90% VCC to 10%*VCC, when VCC is High to Low) ;
T6≤10ms(From 10% VGH to 90%*VCC, when VCC is Low to High) ;
T7≤0.4s(From 10% VCC is H→Lto 10%*VCC is L→H)

To prevent the device from damage due to latch-up, the power ON/OFF sequence shown below must be followed.

Power ON : VDD, VCC → VGL → Input Signals → VGH

Power OFF : VGH → Input Signals → VGL → VDD, VCC

5.3 LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current			20	30	mA	
LED voltage	V_{LED1},V_{LED2}	9.2	10.2	11.2	V	Note 1
LED Life Time	-	(10000)	-	-	Hr	Note 2,3

Note 1 : There are 2 Groups LED , each of FB = 0.6V , $V_{LED1,2}$=10.2V (typ.)
Note 2 : Ta = 25℃ ,
Note 3 : Brightess to be decreased to 50% of the initial value

6. AC Characteristics

6.1. Input signal characteristics

6.1.1. CCIR601/656 Interface

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
CLK period	T_{OSC}	-	37	-	ns
Data setup time	T_{SU}	12	-	-	ns
Data hold time	T_{HD}	12	-	-	ns

6.1.2 Hardware reset timing

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
RESET low pulse width	T_{RSB}	10	-	-	μs

6.2. Output signal characteristics for Digital input signal

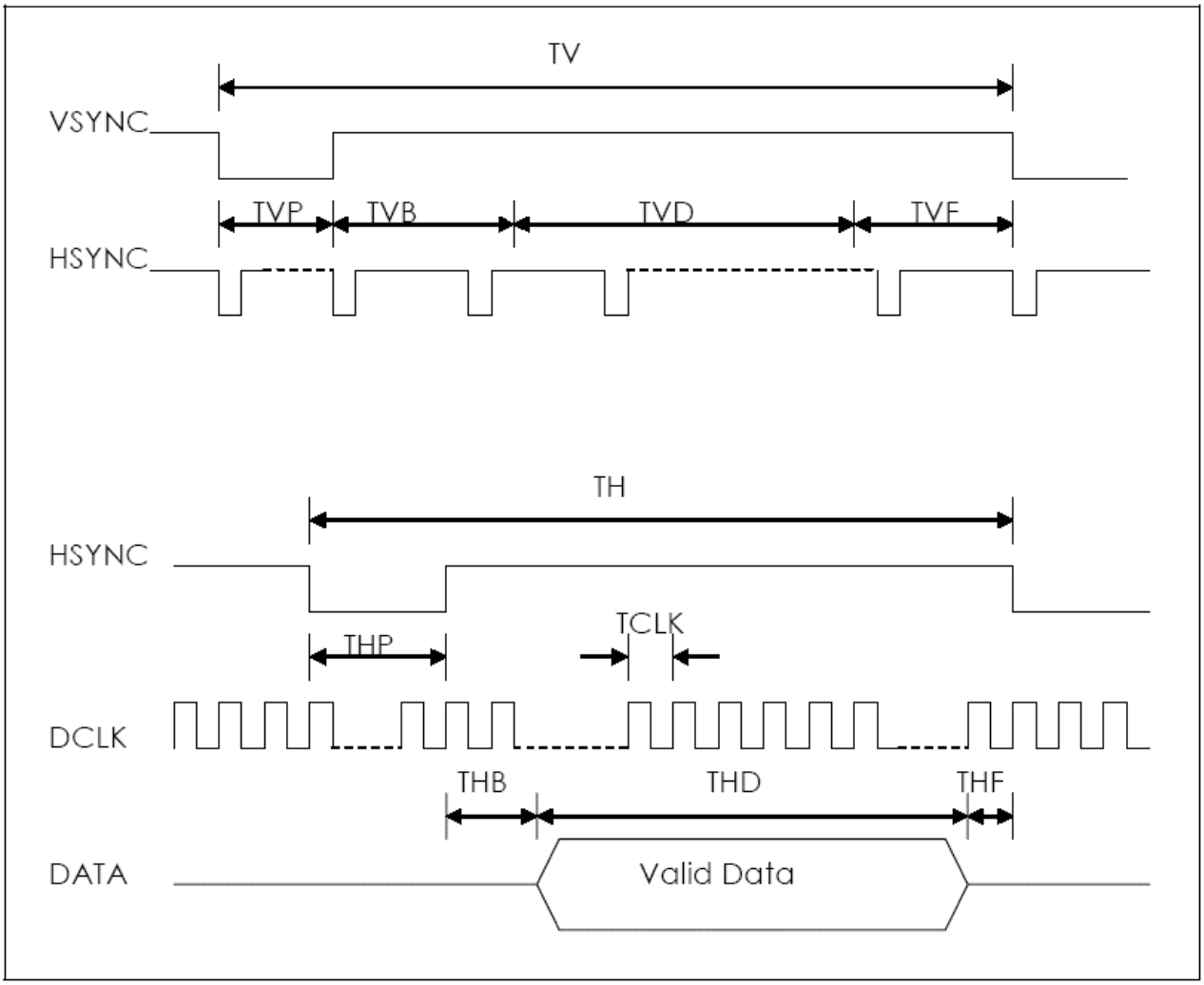
PARAMETER		Symbol	Min.	Typ.	Max.	Unit
Rising time		T_r	-	-	10	ns
Falling time		T_f	-	-	10	ns
Internal STH setup time		T_{SUS}	12	-	-	ns
Internal STH hold time		T_{HDS}	12	-	-	ns
Internal data setup time		T_{SUD}	60	-	-	ns
Internal data hold time		T_{HDD}	40	-	-	ns
OEH pulse width		T_{OEH}	-	1248	-	ns
OEV pulse width		T_{OEV}	-	4992	-	ns
CKV pulse width		T_{CKV}	-	3744	-	ns
Hsync – DEH time		T_1	-	4368	-	ns
Hsync – CKV time		T_2	-	2496	-	ns
Hsync – OEV time		T_3	-	624	-	ns
Vsync – setup time		T_{SUV}		1872	-	ns
Vsync – pulse time		T_{STV}		1	-	T_H
Vsync – STV time	NTSC	T_{VS1}	-	19	-	T_H
	PAL	T_{VS1}	-	27	-	T_H
OEH – STV time		T_{HE}	-	2	-	T_H
Output settling time		T_{OES}	-	12	20	μs

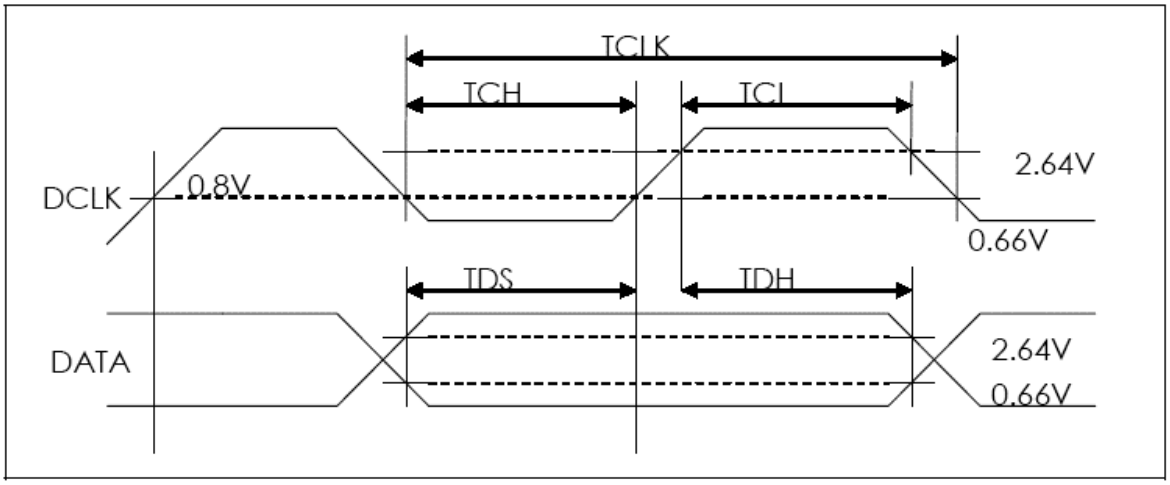
6.2. 24-bits parallel RGB Interface

6.2.1. AC Timing characteristics

Signal	Item		Symbol	Min	Typ	Max	Unit
Dclk	Frequency		Dclk	-	6.4	-	MHZ
	High Time		Tch	-	78	-	ns
	Low Time		Tcl	-	78	-	ns
Data	Setup Time		Tds	12	-	-	ns
	Hold Time		Tdh	12	-	-	ns
Hsync	Period		TH	-	408	-	DCLK
	Pulse Width		Thp	-	30	-	DCLK
	Back-Porch		Thb	-	38	-	DCLK
	Display Period		Thd	-	320	-	DCLK
	Front-Porch		Thf	-	20	-	DCLK
Vsync	Period	NTSC	Tv	-	262.5	-	TH
		PAL			312.5		
	Pulse Width		Tvp	1	3	5	TH
	Back-Porch	NTSC	Tvb	-	15	-	TH
		PAL			23		
	Display Period		Tvd	-	240	-	TH
	Front-Porch	NTSC	Tvf	-	4.5	-	TH
		PAL			46.5		

6.1.2.2 AC Timing Diagrams



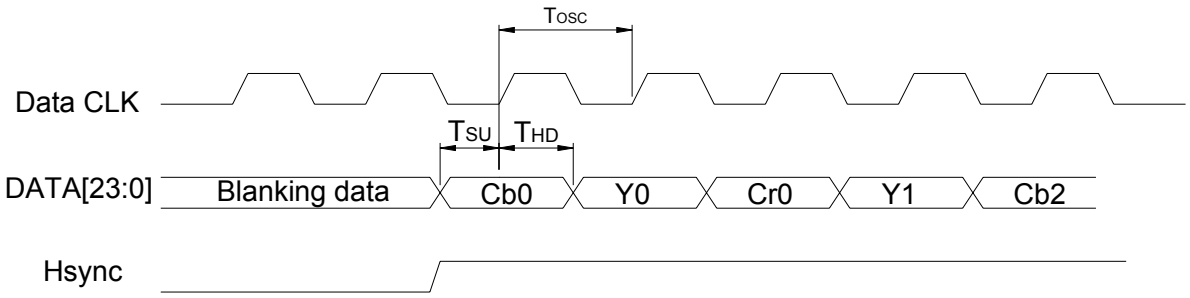


7. Waveform

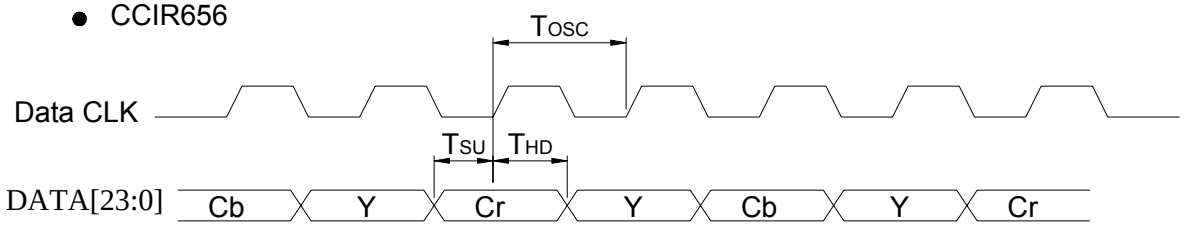
7.1. Timing Controller Timing Chart

7.1.1. Clock and Data waveform

- CCIR601(HS_POL="L" in Register R2)



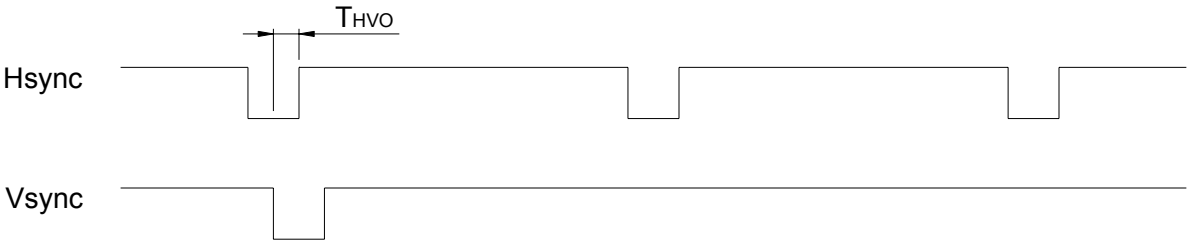
- CCIR656



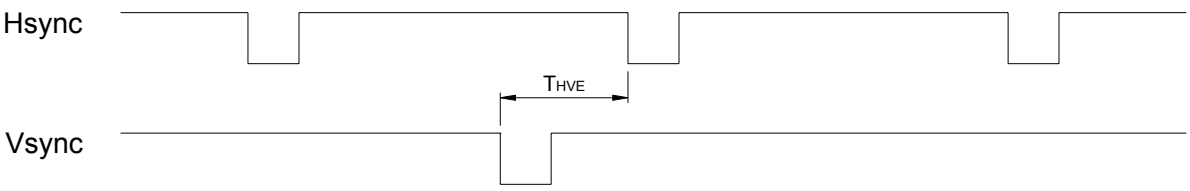
7.1.2 Digital / Analog RGB timing waveform

7.1.2.1 Hsync and Vsync timing

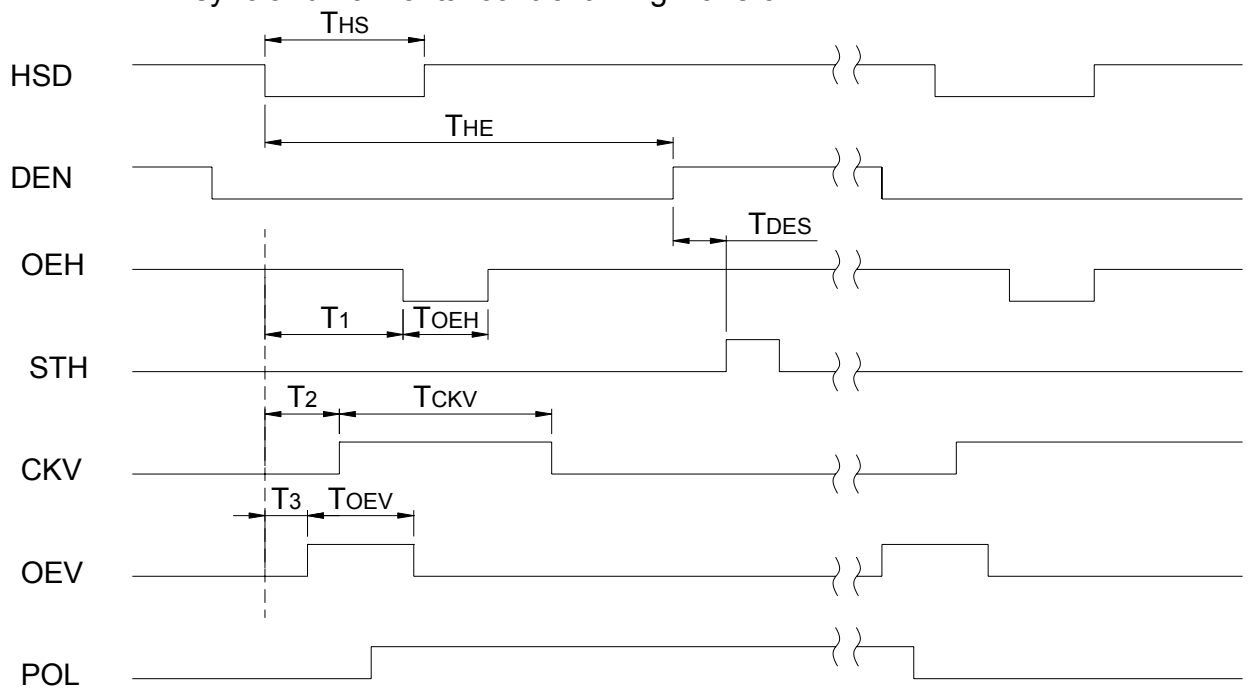
- Odd field



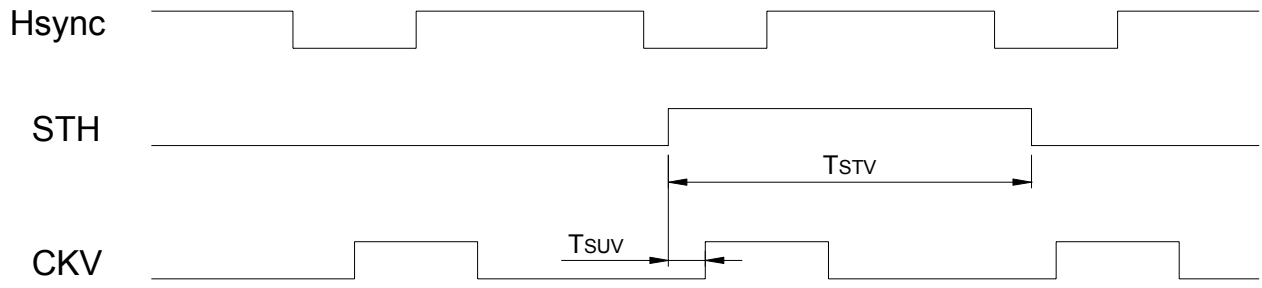
- Even field



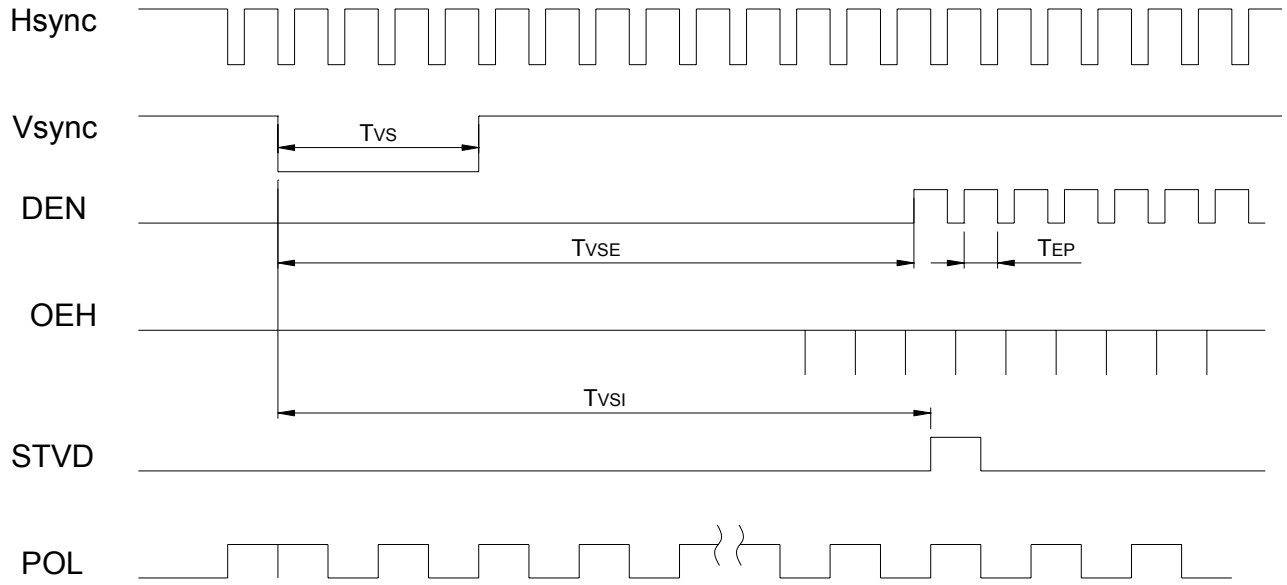
7.1.2.2 Hsync and horizontal control timing waveform



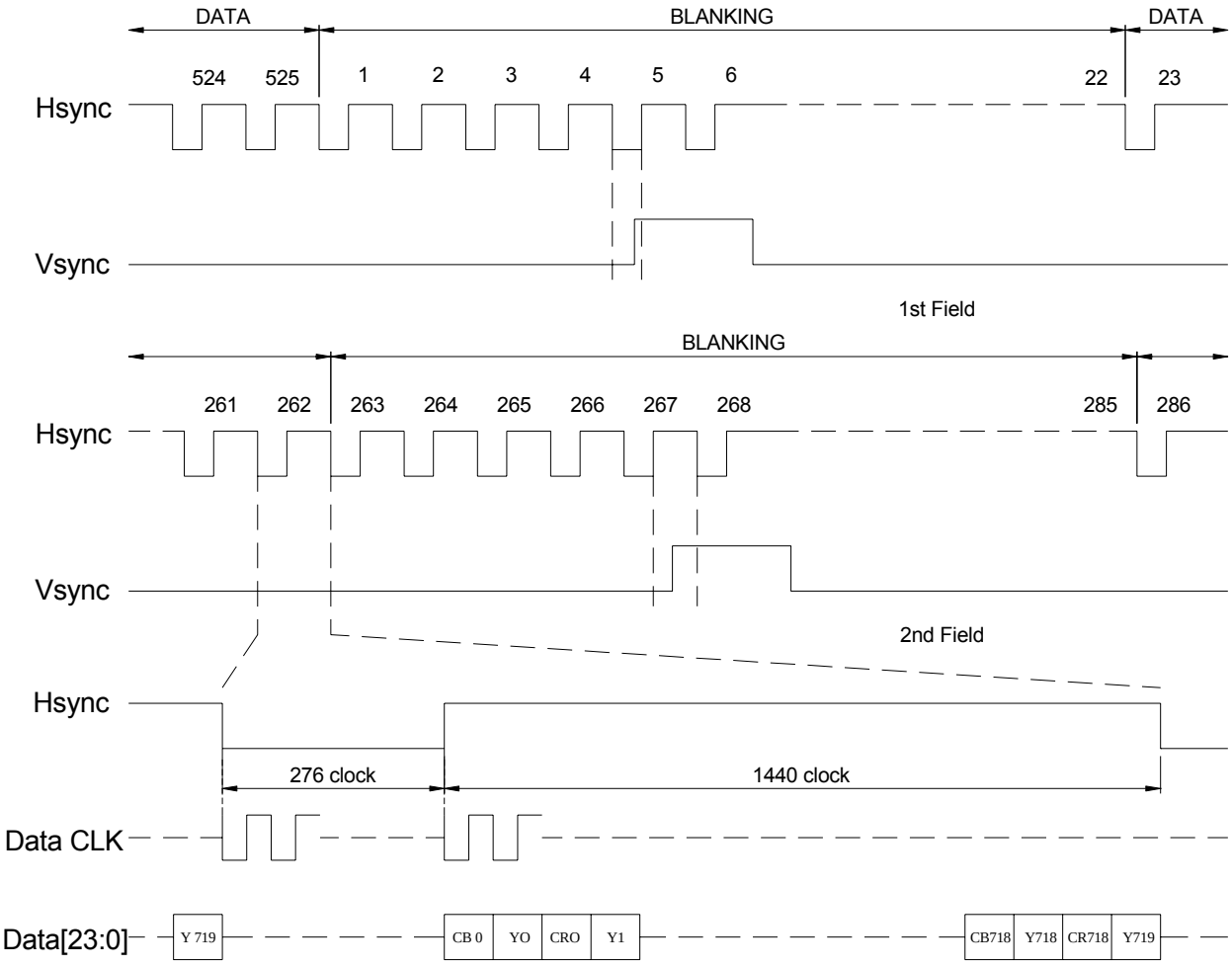
7.1.2.3 Hsync and vertical shift clock timing waveform



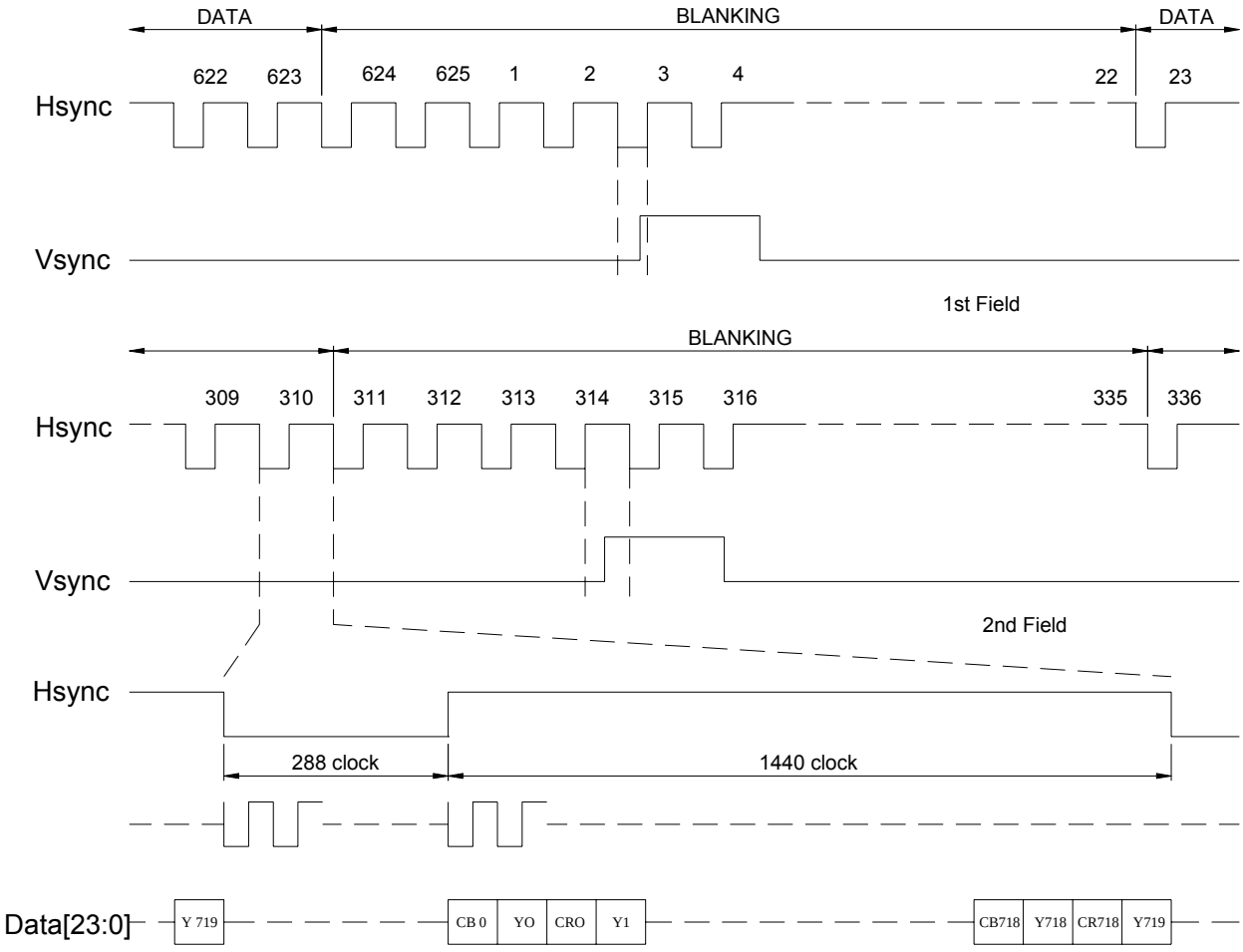
7.1.2.4 Hsync and vertical control timing waveform



7.1.3 CCIR601 timing waveform (VS_POL="H" , HS_POL="L" in Register R2)



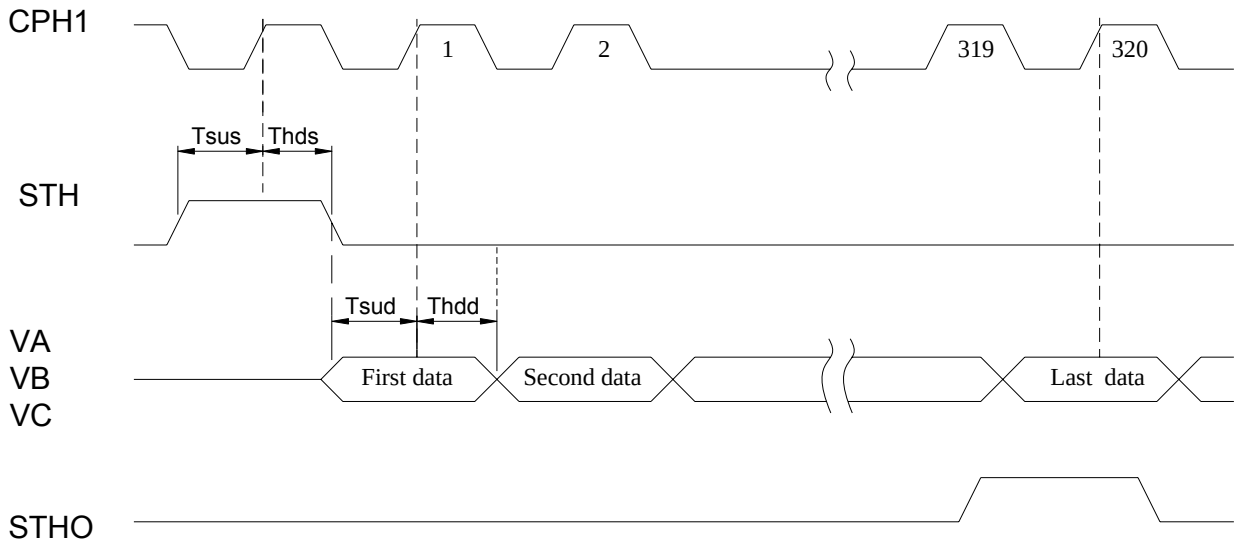
ITU-BT.601 NTSC Input Timing



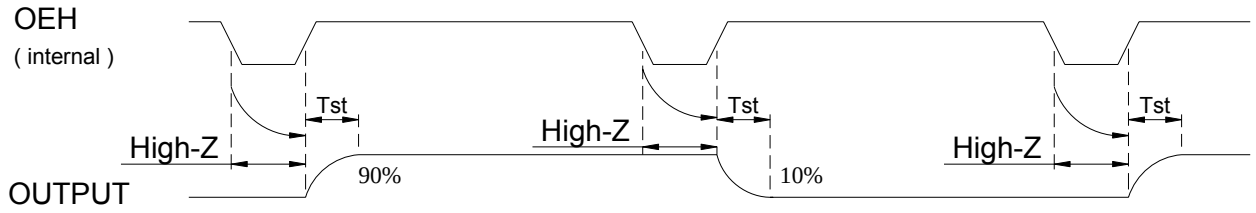
ITU-BT.601 PAL Input Timing

7.2 Source Driver Timing Chart

7.2.1 Clock and Start Pulse timing waveform



7.2.2 OEH and Data Output timing waveform



7.3 Analog video signal characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
Video signal amplitude (VA, VB, VC)	V_{IAC}	-	3.81	-	V
	V_{IDC}	-	2.385	-	V

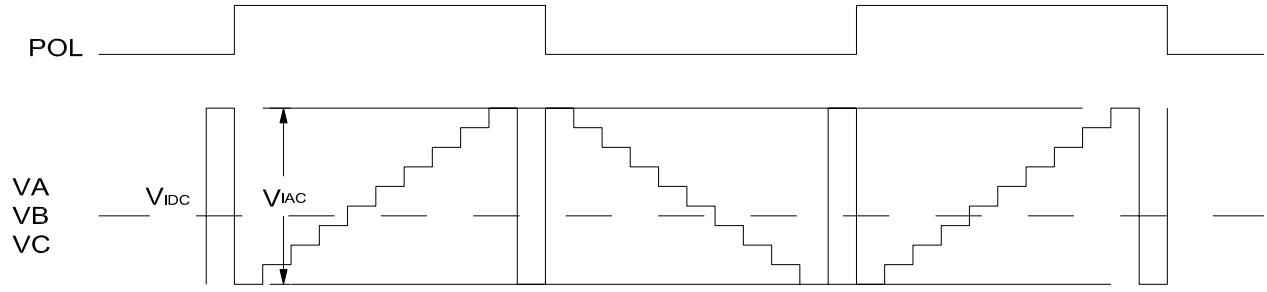
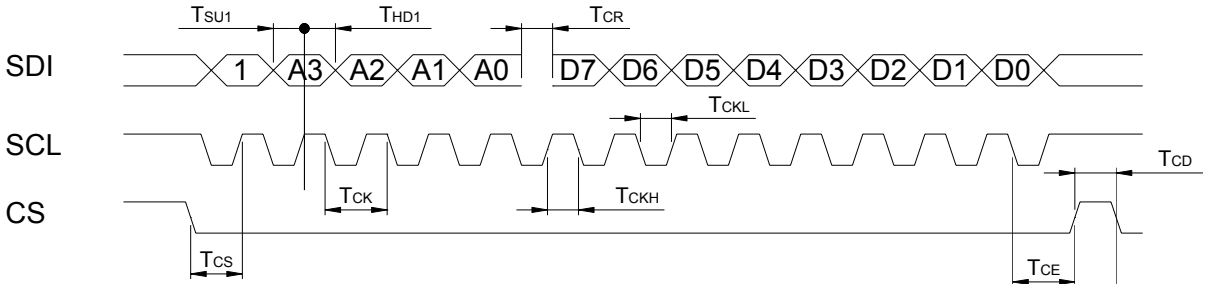


Fig. 4-(a) Horizontal timing

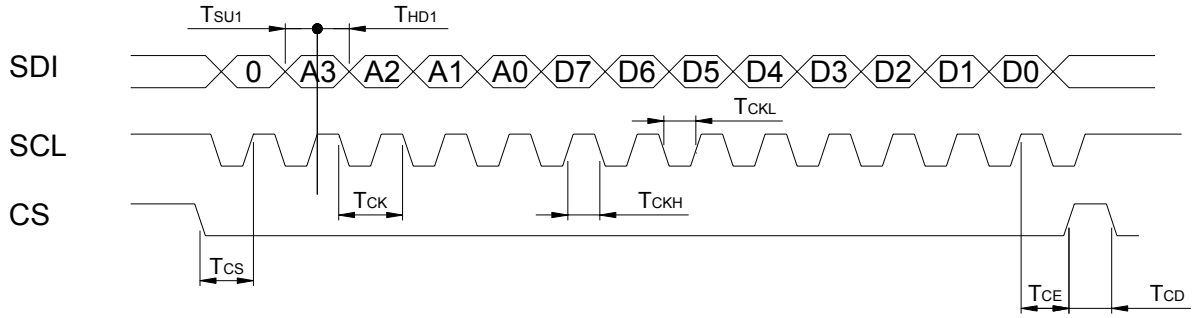
7.4 SPI timing characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SCL period	T_{CK}	60	-	-	ns
SCL high width	T_{CKH}	30	-	-	ns
SCL low width	T_{CKL}	30	-	-	ns
Data setup time	T_{SU1}	12	-	-	ns
Data hold time	T_{HD1}	12	-	-	ns
CS to SPCK setup time	T_{CS}	20	-	-	ns
CS to SPDA hold time	T_{CE}	20	-	-	ns
CS high pulse width	T_{CD}	50	-	-	ns
SDI output latency	T_{CR}		1/2	-	T_{CK}

- SPI "read" timing

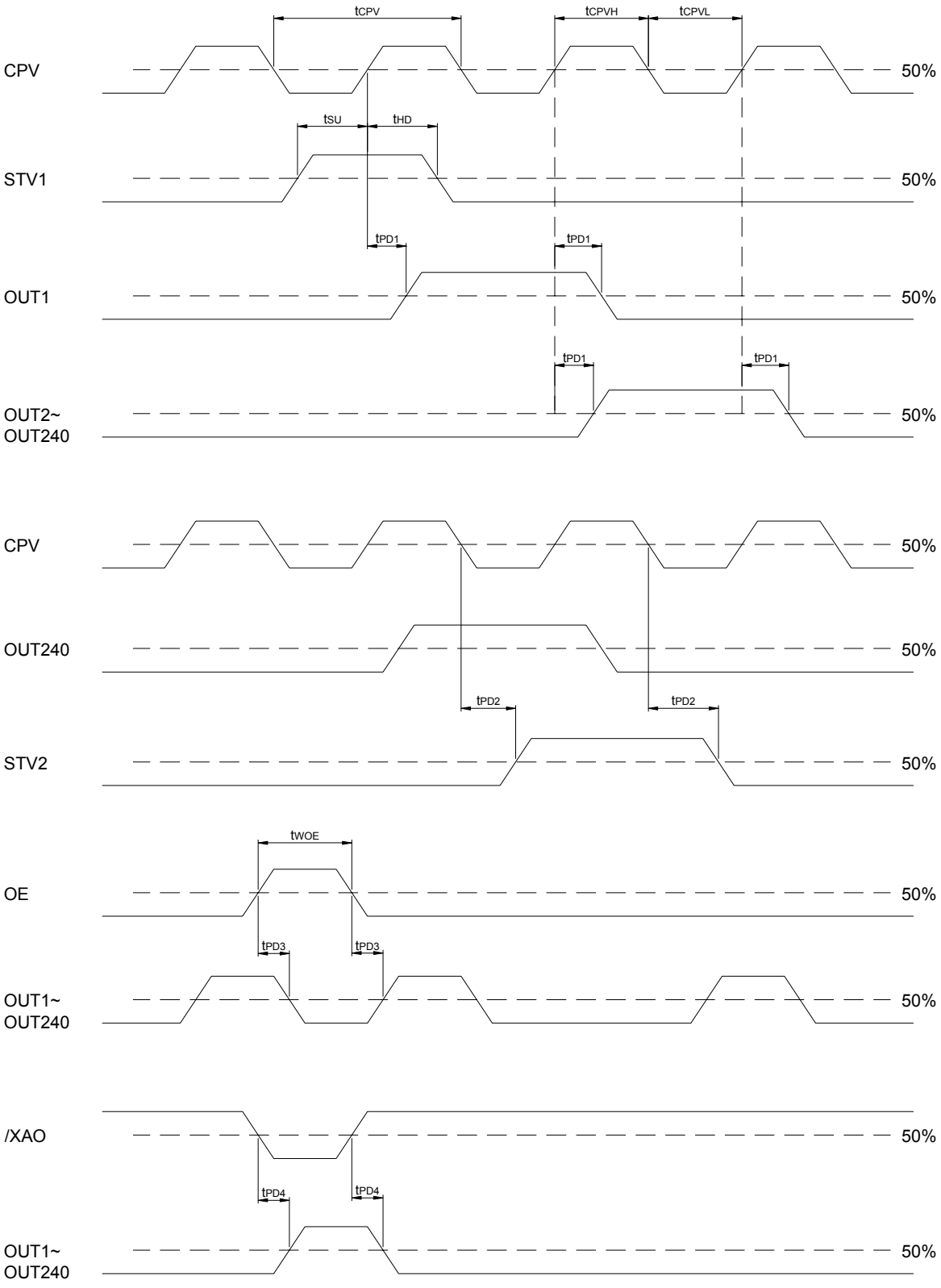


- SPI "write" timing



7.5 Gate Driver Timing Chart

Parameter	Symbol	Condition	Spec		Unit
			Min.	Max.	
Operation frequency	tCPV		5	-	μs
CPV pulse width	tCPVH,tCPVL	50%duty cycle	2.5	-	
OE pulse width	twOE		1	-	
Data setup time	tsu		0.4	-	us
Data hold time	thd		0.7	-	
Output delay time	tpd1	CL=300pF	-	1	
Output delay time	tpd2	CL=300pF	-	0.8	
Output delay time	tpd3	CL=300pF	-	0.8	
Output delay time	tpd4	CL=300pF	-	10	


tCPV
tCPVH
tCPVL
CPV
50%
tSU
tHD
STV1
50%
tPD1
tPD1
OUT1
50%
tPD1
tPD1
OUT2~
OUT240
50%
CPV
50%
OUT240
50%
tPD2
tPD2
STV2
50%
tWOE
OE
50%
tPD3
tPD3
OUT1~
OUT240
50%
/XAO
50%
tPD4
tPD4
OUT1~
OUT240
50%

8. Optical Characteristics

Ta=25±2℃, ILED=20mA

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr	θ=0°	-	15	30	ms	Note 3,5
		Tf		-	35	50	ms	
Contrast ratio		CR	At optimized viewing angle	150	200			Note 4,5
Color Chromaticity	White	Wx	θ=0°	(0.25)	(0.30)	(0.35)		Note 2,6,7
		Wy		(0.27)	(0.32)	(0.37)		
Viewing angle	Hor.	ΘR	CR≥10	(40)	(60)	-	Deg.	Note 1
		ΘL		(40)	(60)	-		
	Ver.	ΘT		(10)	(35)	-		
		ΘB		(30)	(55)	-		
Uniformity		U	-	(75)	(80)	-	%	Note 8
Brightness		-	-	(200)	(250)	-	cd/m^2	Center of display

Note 1: Definition of viewing angle range

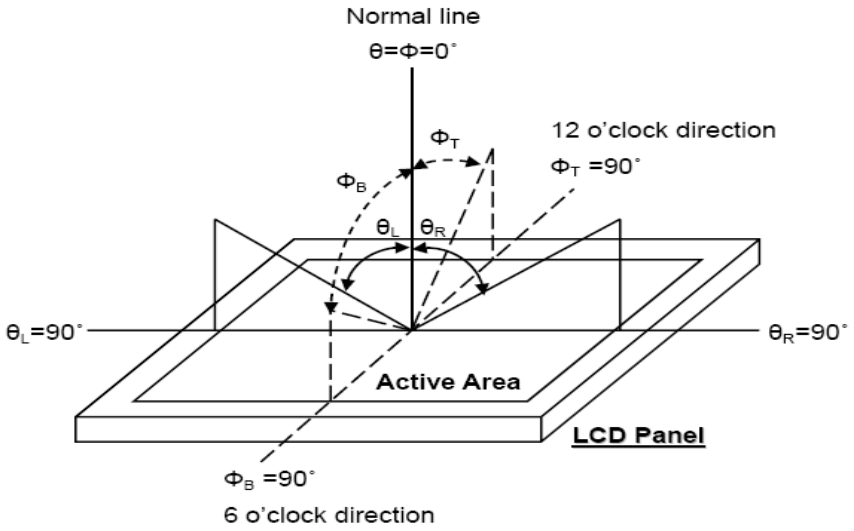


Fig. 8-1 Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

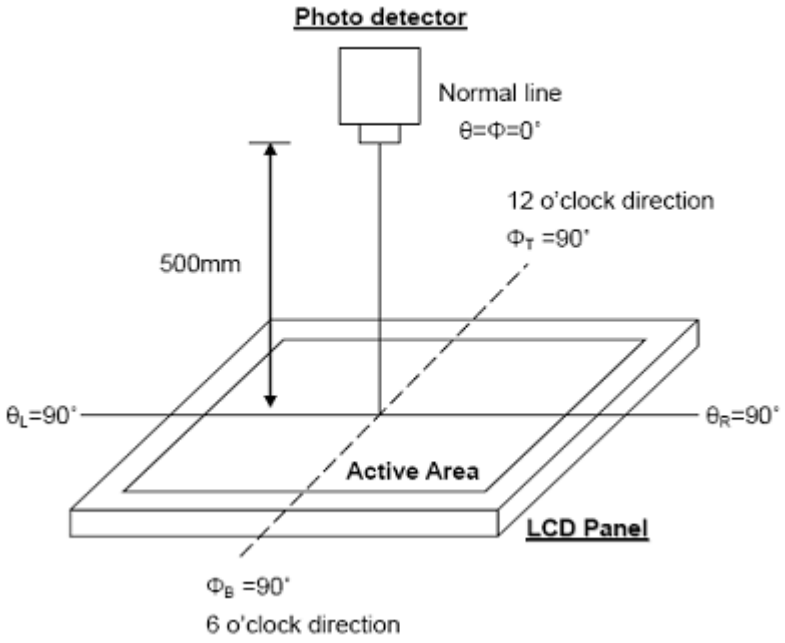


Fig. 8-2 Optical measurement system setup

Note 3: Definition of Response time:

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time, Tr, is the time between photo detector output intensity changed from 90% to 10% . And fall time, Tf, is the time between photo detector output intensity changed from 10% to 90% .

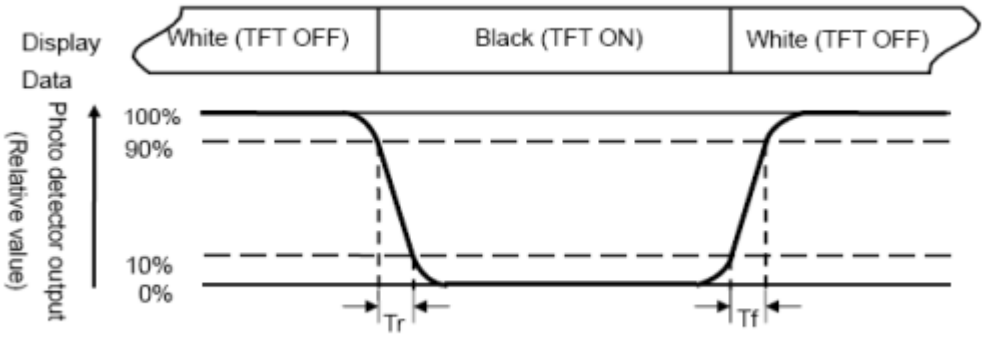


Fig. 3-3 Definition of response time

Note 4: Definition of contrast ratio:
The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

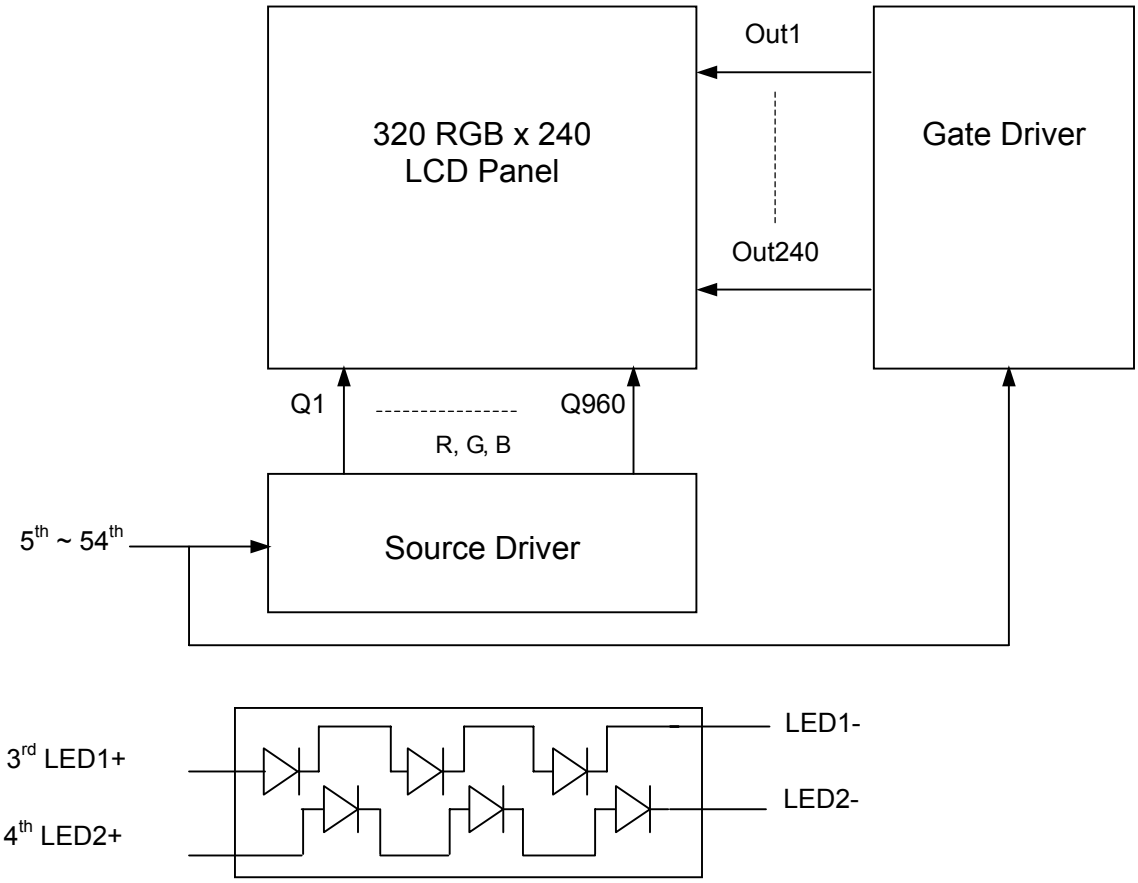
Note 5: White Vi = $V_{i50} \pm 1.5V$
Black Vi = $V_{i50} \pm 2.0V$
“±” means that the analog input signal swings in phase with VCOM signal.
“±” means that the analog input signal swings out of phase with VCOM signal.
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 6: Definition of color chromaticity (CIE 1931)
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

$$\text{Note 8 : Uniformity (U)} = \frac{\text{Brightness (min)}}{\text{Brightness (max)}} \times 100\%$$

9. BLOCK DIAGRAM



10. Input / Output Terminals

10.1. PIN Definition

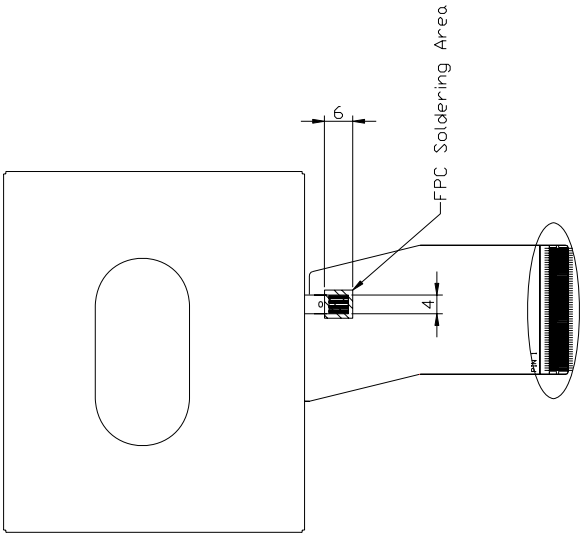
Pin No.	Symbol	I/O	Description
1	LED 1-	I	LED_Cathode
2	LED 2-	I	LED_Anode
3	LED 1+	I	LED_Cathode
4	LED 2+	I	LED_Anode
5	IF1	I	Input data format control (Note1)
6	IF2	I	Input data format control (Note1)
7	POL	O	Polarity Signal connect to VCOM driving circuit.
8	RESET	I	Hardware reset.
9	CS	I	Chip select
10	SCL	I	Serial Clock
11	SDI	I/O	Serial Data
12	B0	I	Blue Data bit (LSB)
13	B1	I	Blue Data bit
14	B2	I	Blue Data bit
15	B3	I	Blue Data bit
16	B4	I	Blue Data bit
17	B5	I	Blue Data bit
18	B6	I	Blue Data bit
19	B7	I	Blue Data bit (MSB)
20	G0	I	Green Data bit (LSB)
21	G1	I	Green Data bit
22	G2	I	Green Data bit
23	G3	I	Green Data bit
24	G4	I	Green Data bit
25	G5	I	Green Data bit
26	G6	I	Green Data bit
27	G7	I	Green Data bit (MSB)
28	R0	I	Red Data bit (LSB)
29	R1	I	Red Data bit
30	R2	I	Red Data bit
31	R3	I	Red Data bit
32	R4	I	Red Data bit
33	R5	I	Red Data bit
34	R6	I	Red Data bit
35	R7	I	Red Data bit (MSB)

36	Hsync	I	Horizontal synchronous signal
37	Vsync	I	Vertical synchronous signal
38	Data CLK	I	Dot data clock
39	AVDD(analog)	I	Analog power: 4.5V~5.5V
40	AVDD(analog)	I	Analog power: 4.5V~5.5V
41	VDD(Digital)	I	Digital power: 3V~3.6V
42	VDD(Digital)	I	Digital power: 3V~3.6V
43	NPC	O	NTSC/PAL mode Auto detection result H:NTSC/L:PAL
44	VGL	I	Gate off power
45	VGL	I	Gate off power
46	UD	I	Up/Down scan setting. H: Reverse scan / L: Normal scan
47	VGH	I	Gate on power
48	LRC	I	Shift direction of device internal shift register control.
49	GND	I	GROUND
50	VCOM	I	VCOM driving input
51	VCOM	I	VCOM driving input
52	Dnable	I	Data enable input.Normally pull low.
53	GND	I	GROUND
54	GND	I	GROUND

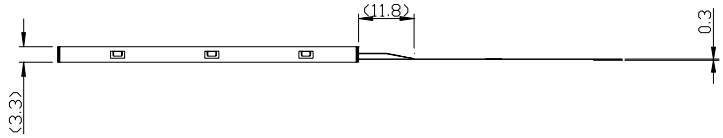
Note 1. Control the input data format.

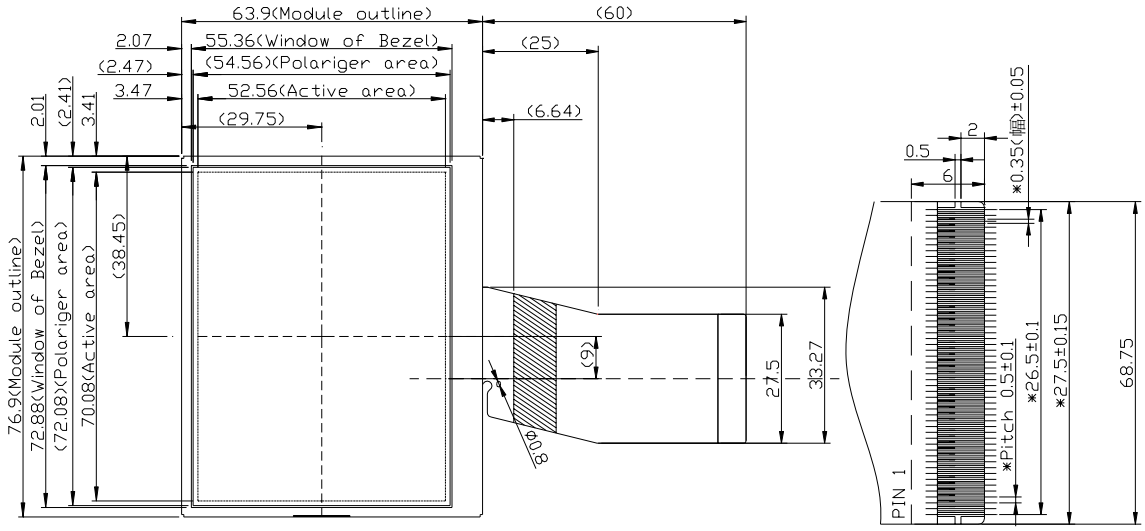
IF2, IF1	Input data format
L, L (default)	Serial RGB
L, H	Parallel RGB
H, L	CCIR601
H, H	CCIR656

11. Outline Drawing



NOTE:
1.Unmark tolerance : ± 0.5 mm
2.Suitable connector : Kyocera elco 6240 series or equivalent





12. QUALITY ASSURANCE

12.1 Test Condition

12.1.1 Temperature and Humidity(Ambient Temperature)

Temperature : 20 ± 5°C
Humidity : 65 ± 5%

12.1.2 Operation

Unless specified otherwise, test will be conducted under function state.

12.1.3 Container

Unless specified otherwise, vibration test will be conducted to the product itself without putting it in a container.

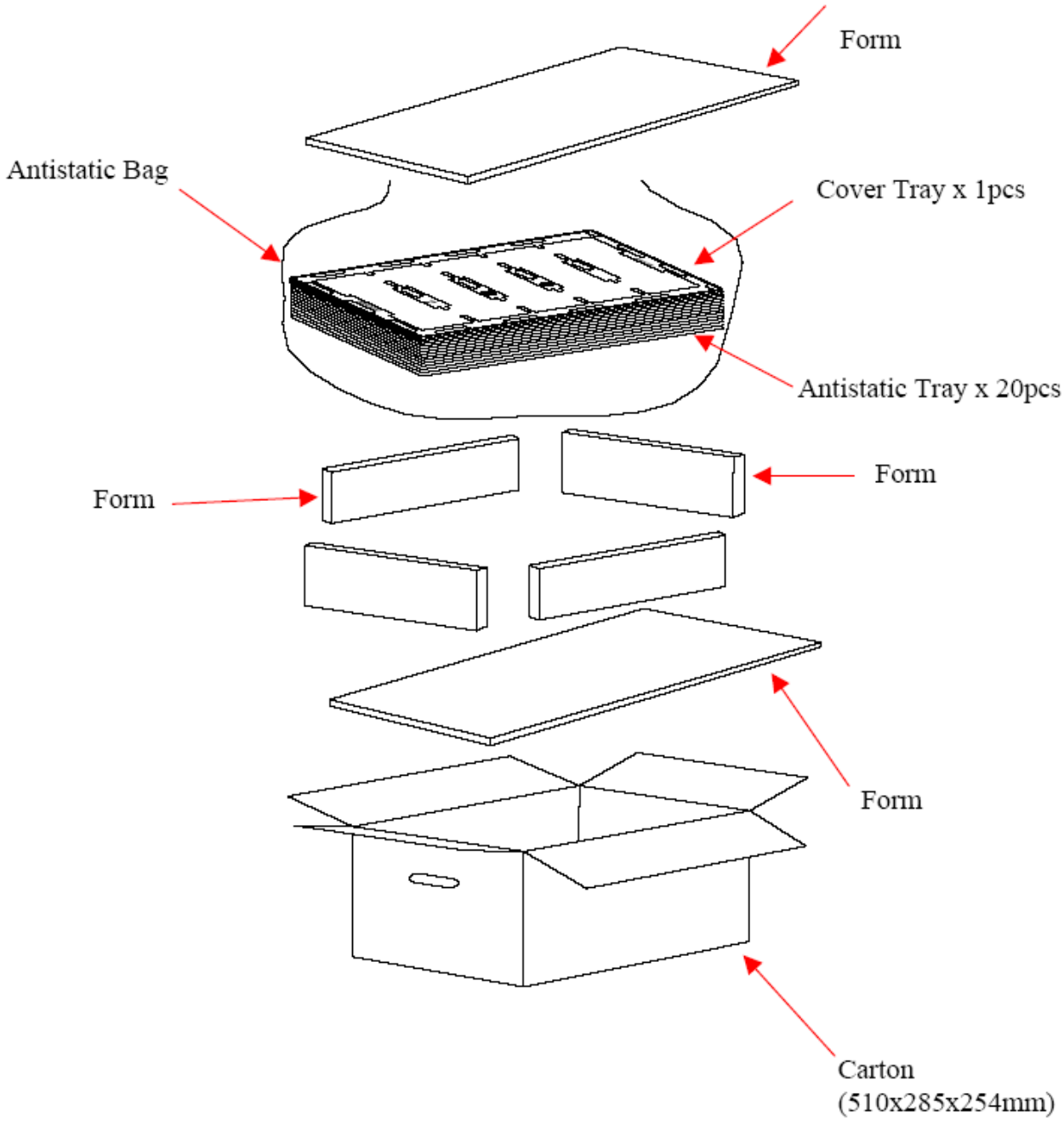
12.1.4 Test Frequency

In case of related to deterioration such as shock test. It will be conducted only once.

12.1.5 Test Method

No.	Reliability Test Item & Level	Test Level
1	High Temperature Storage Test	T=70°C,240hrs
2	Low Temperature Storage Test	T=-20°C,240hrs
3	High Temperature Operation Test	T=70°C,240hrs
4	Low Temperature Operation Test	T=-10°C,240hrs
5	High Temperature and High Humidity Operation Test	T=60°C,90% RH,240hrs
6	Thermal Cycling Test (No operation)	-20C → +25°C → +70°C,100 Cycles 30 min 5min 30 min
7	Vibration Test (No operation)	Frequency:10~ 55 Hz Amplitude:1.0mm Sweep Time:1min Test Period:6 Cycles for each Direction of X,Y,Z
8	Electrostatic Discharge Test (No operation)	150pF,330Ω Air:± 15KV;Contact: ± 8KV 10 times/point;4 points/panel face

13. Package



1 Antistatic tray = 10 pcs
1 Carton = 10(pcs/Layer) x 20(Layer) = 200 pcs
Total Weight = (9.0) kgw
Remove display protective film before use it.