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	SPECIFICATION	APPLICABLE GROUP LIQUID CRYSTAL DISPLAY GROUP

DEVICE SPECIFICATION FOR

TFT - LCD module

MODEL No. LQ080Y5DR02

CUSTOMER'S APPROVAL

DATE

BY

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1. General

This TFT-LCD module is a color active matrix LCD (Liquid Crystal Display) module of transmissive type incorporating amorphous silicon TFT (Thin Film Transistor). General specification of the module is shown in the Table 3-1.

It is composed of a color TFT-LCD panel, driver ICs, control-PWB, FPC, frame, shielding front case, shielding back case and backlight unit. (The DC / AC inverter circuit to drive the backlight is not contained in the module.)

2. Features

- Utilizes a panel with a 15:9 aspect ratio, which makes the module suitable for use in wide-screen systems.
- The 8 screen produces a high resolution image that is composed of 384,000 pixels elements in a stripe arrangement.
- Possible to indicate 262,144 colors by 18 bits (6 bits x RBG) data signal.
- Wide viewing field angle technology is employed. (The most suitable viewing angle is the 6 o'clock direction.)
- By adopting an active matrix drive, a picture with high contrast is realized.
- Reduced reflection as a result of low reflection black matrix and an antiglare (AG) and low-reflection (LR) polarizer being adopted.
- By COG method, realized a slim, lightweight, and compact module.
- Realized a high quality picture of the natural color appearance by adopting the TN-Normally White Mode which is superior to the color appearance.
- An inverted video display in the vertical and horizontal directions is possible.
- Built-in backlight with the high performance of start-up in the low temperature.
- The followings are possible to control by I2C−Bus communication:
  1) Brightness, Contrast and γ adjustment function
  2) RGB signal offset adjustment function
  3) Horizontal and Vertical display position adjustment function
  4) Switching function of the display direction
  5) Switching function of the test pattern indication
- Caution : Driving is possible without I²C-Bus control and default image is shown on the display this case.

3. Mechanical specifications (Dot Composition)

General Specification of the Module Table 3-1

Parameter	Specifications	Units	Remarks
Display format	384,000	pixels	
	2400(W)×480(H)	dots	
Active area	174.0 (W) × 104.4 (H)	mm	
Screen size (Diagonal)	20.3[8 “]	cm	
Dot pitch	0.0725 (W) × 0.2175 (H)	mm	
Pixel configuration	R,G,B Stripe configuration		
Outline dimension	190 (W) × 120 (H) × 13.0 (D)	mm	[Note 3-1]
Mass	385(Typ.)	g	

[Note 3-1]

Typical values are given. For detailed measurements and tolerances, refer to Fig. 8, Outline Dimension of the Module.

4. Input terminal and its function

4-1 TFT-LCD panel driving part

Connector used: 40FLZ-RSM1-R (JST Co., Ltd.)

Table 4-1

Pin No.	Symbol	Description	Remarks
1	GND	Ground	
2	DCLK	Clock signal for sampling each data signal	
3	GND	Ground	
4	R0	RED data signal(LSB)	
5	R1	RED data signal	
6	R2	RED data signal	
7	R3	RED data signal	
8	R4	RED data signal	
9	R5	RED data signal(MSB)	
10	GND	Ground	
11	G0	GREEN data signal(LSB)	
12	G1	GREEN data signal	
13	G2	GREEN data signal	
14	G3	GREEN data signal	
15	G4	GREEN data signal	
16	G5	GREEN data signal(MSB)	
17	GND	Ground	
18	B0	BLUE data signal(LSB)	
19	B1	BLUE data signal	
20	B2	BLUE data signal	
21	B3	BLUE data signal	
22	B4	BLUE data signal	
23	B5	BLUE data signa(MSB)l	
24	GND	Ground	
25	Hsync	Horizontal Sync	[Note4-1]
26	DataEn	Horizontal Data Enable (Fixed to Lo when the internal register value is used.)	[Note4-3]
27	Vsync	Vertical Sync	[Note4-1]
28	GND	Ground	
29	SCK	Clock signal for serial interface	[Note4-4]
30	SDI	Data signal for serial interface	[Note4-4]
31	WC	EEPROM write protect signal for serial interface	[Note4-4]
32	SCS	Chip select signal for serial interface	[Note4-4]
33	GND	Ground	
34	HVR	Horizontally and Vertically inverted	[Note4-2]
35	RST	Compulsive Reset signal	[Note4-5]
36	VCC	+3.3V power supply	
37	VCC	+3.3V power supply	
38	VCC	+3.3V power supply	
39	GND	Ground	
40	GND	Ground	

[Note4-1]

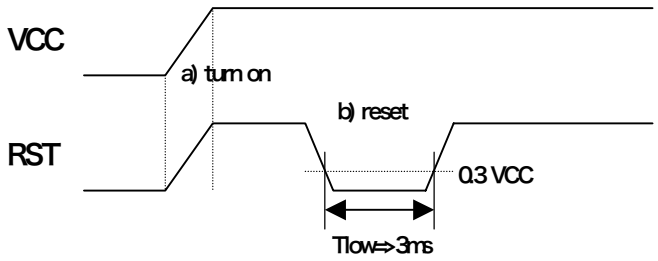
Hsync	Negative polarity
Vsync	Negative polarity

[Note4-2] HVR = " High " : Regular video
HVR = " Low ": Horizontally and Vertically inverted video

[Note4-3] The horizontal display starting position is settled in accordance with a rising timing of DataEn signal. (Refer to P.9,Fig. 2)
In case DataEn is fixed to “Low”, the horizontal display starting position is determined as described in P.10,Fig. 3.(Don’t keep DataEn “High” during operation..)

[Note4-4] In the case that I2C-Busis not used, keep the below terminals as follows,
SCK=Low
SDI=Low
WC=High
SCS= Low

[Note4-5] The purpose of this terminal (No.35 Pin) is to provide reset for controlled IC in this module.
a) When the input power (VCC) is turn on, RST is to turn on at the same timing.
b) When RST is reset (High to Low), the resetting (Low) duration should be more than 3msec.
(See below Fig.)



4-2) Backlight fluorescent tube driving part
Connector used :(BHR-04(4.0)VS-1N (JST Co.,Ltd.))
Fitting connector : (SM04(4.0)B-BHS-1-TB (JST Co.,Ltd.) or the equivalent.)

Table 4-2

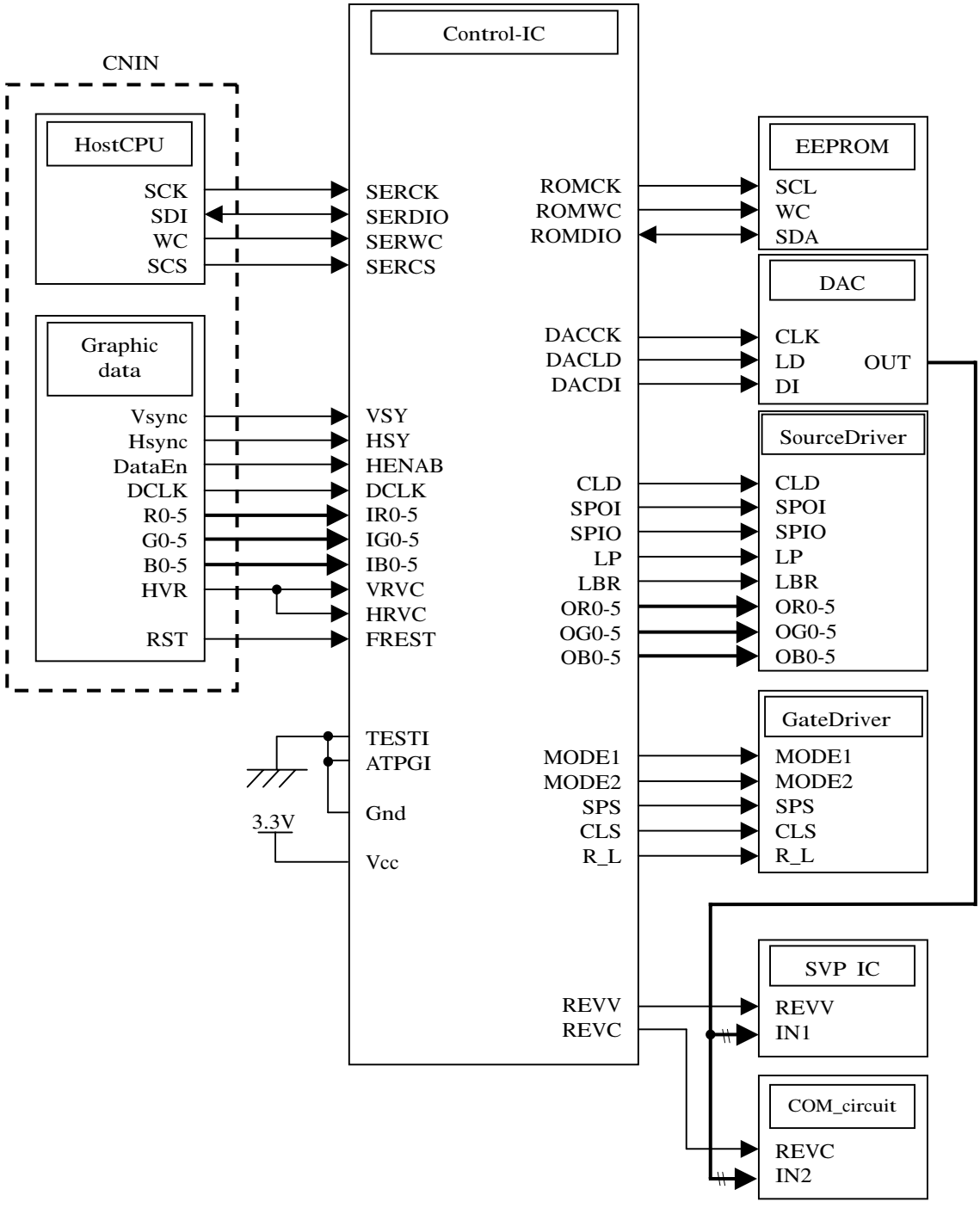
No.	Symbol	Function
1	VL1	Input terminal 1(Hi voltage side)
2	VL2	Input terminal 2(Hi voltage side)
3	VL3	Input terminal 3(open)
4	VL4	Input terminal 4 (Low voltage side)

5. General function of the Control PWB

As this system has EEPROM, DAC, SVP_IC (IC for standard voltage production) and COM_circuit (Common power supply production circuit) on the peripherals of the control PWB, it is possible to have the variety of functions about picture by inputting the 2 line type serial data (I^2Cbus type) which is supplied from the Graphic Data and the Host CPU to the input terminal (CNIN: 40 Pin).

This system is so designed that the data written in the designated address of the EEPROM is written to the internal register in the control IC (hereinafter called C-IC) of this system by applying 3.3V to the power supply terminal Vcc, therefore, it is possible to store the display settings as users wish.
Furthermore, as the data at the designated address in EEPROM or C-IC can be changed or written, it is possible to realize the display of the picture as users wish.

・The Block Diagram of this system is shown in the P.6　Fig. 1.
・AC characteristics of the serial interface is shown in P. 11～12.
・The timing chart at the power ON (when initialing the internal register of C-IC) between the control IC and the EEPROM is shown in P.13.
・The timing chart when re-writing the internal register of C-IC by the serial communication is shown in　P. 14.
・The control timing of SCS and WC (signal timing of the serial interface) is shown in P. 15.



ADC ：A/D Converter (output:8bit Digital Data)
DAC ：D/A Converter (output: Analog Data)
SVP_IC ：IC for standard voltage production
COM_circuit ：Common power supply production circuit

Fig. 1. Block Diagram of the System

6. Timing Characteristics of input signals

6 - 1 When operating under 60Hz

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Clock [DCLK]	Frequency	1/Tc	31.95	33.26	34.60	MHz	Frequency：1/(THa/THb)
	Hi_Time	Tch	8	—	—	ns	
	Lo_Time	Tcl	8	—	—	ns	
Data [I* 0-5]	Setup time	Tds	5	—	—	ns	
	Hold time	Tdh	5	—	—	ns	
Horizontal sync.signal [HSY]	Cycle	THa	31.45	31.75	32.05	μs	
		THb	1024	1056	1088	ck	
	Pulse width	THp	5	—	THb-5	ck	
Vertical sync. Signal [VSY]	Cycle	TV	520	525	530	line	
	Pulse width	TVp	2	—	TV-2	line	
Horizontal display period		THd	—	800	—	ck	
HSY_DCLK phase difference		THc	A-8	0	A+8	ns	※ A=Tch(1/2DCLK)
HSY_VSY phase difference		TVh	-10	0	10	ck	
Vertical display invalid line		TVs	10	—	35	line	Default is 35 Lines.
Vertical display period		TVd	—	480	—	line	
Enable signal [HENAB]	Setup time	Tes	5	—	—	ns	
	Hold time	Teh	5	—	—	ns	
	Pulse width	Tep	5	800	800	ck	
Horizontal display starting position		THe	188	—	244	ck	Note 1

6 - 2 When operating under 50Hz

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Clock [DCLK]	Frequency	1/Tc	26.62	33.00	34.54	MHz	Frequency：1/(THa/THb)
	Hi_Time	Tch	8	—	—	ns	
	Lo_Time	Tcl	8	—	—	ns	
Data [I* 0-5]	Setup time	Tds	5	—	—	ns	
	Hold time	Tdh	5	—	—	ns	
Horizontal sync.signal [HSY]	Cycle	THa	31.50	32.00	38.46	μs	When operating under 50Hz, if THa becomes less than 31.50μs, the display quality may be deteriorated.
		THb	1024	1056	1088	ck	
	Pulse width	THp	5	—	THb-5	ck	
Vertical sync. Signal [VSY]	Cycle	TV	520	525	635	line	Recommend Max.635 Lines.
	Pulse width	TVp	2	—	TV-2	line	
Horizontal display period		THd	—	800	—	ck	
HSY_DCLK phase difference		THc	A-8	0	A+8	ns	※ A=Tch(1/2DCLK)
HSY_VSY phase difference		TVh	-10	0	10	ck	
Vertical display invalid line		TVs	10	—	35	line	Default is 35 Lines.
Vertical display period		TVd	—	480	—	line	
Enable signal [HENAB]	Setup time	Tes	5	—	—	ns	
	Hold time	Teh	5	—	—	ns	
	Pulse width	Tep	5	800	800	ck	
Horizontal display starting position		THe	188	—	244	ck	Note 1

・Refer to P.9 Fig.2 and P.10 Fig. 3 for the input timing chart.

Note 1: Note for setting the Horizontal display starting position (THe: phase difference between HSY falling and HENAB rising)

- In case of setting the Horizontal display starting position by entering DataEn signal from outside:

  When the rising timing of DataEn signal is out of the specification range (188-244ck), the display starting position, THe, becomes the value set as the Horizontal display starting position in the internal register of C-IC. As the defaultvalue of the internal register of C-IC is 244, if the display starting position is not set by the serial communication, the display starting position, THe, begins from the data of 244ck.
  Although, DataEn signal is recommended to input actively at every Horizontal period in the Vertical period, it has no problem to fix to Lo for the Vertical returning period and to input actively at every Horizontal period in the Vertical display period. (Refer to P.9 Fig. 2)

- In case of setting the Horizontal display starting position by re-writing the internal register value of C-IC by the serial communication:
  Set the DataEn input terminal to Lo in order to give the priority to the setting of the display starting position by the serial signals（SCS, WC, SCK and SDIO）.
  (Refer to P.10 Fig. 3)
  When the setting of the display starting position in the internal register of C-IC is set as THe≦188, the register setting value becomes to THe=188 and when set as THe≧244, the register setting value becomes to THe=244.

  (Do not set the display starting position by serial communication when DataEn signal i s assumed to use in the active condition.)

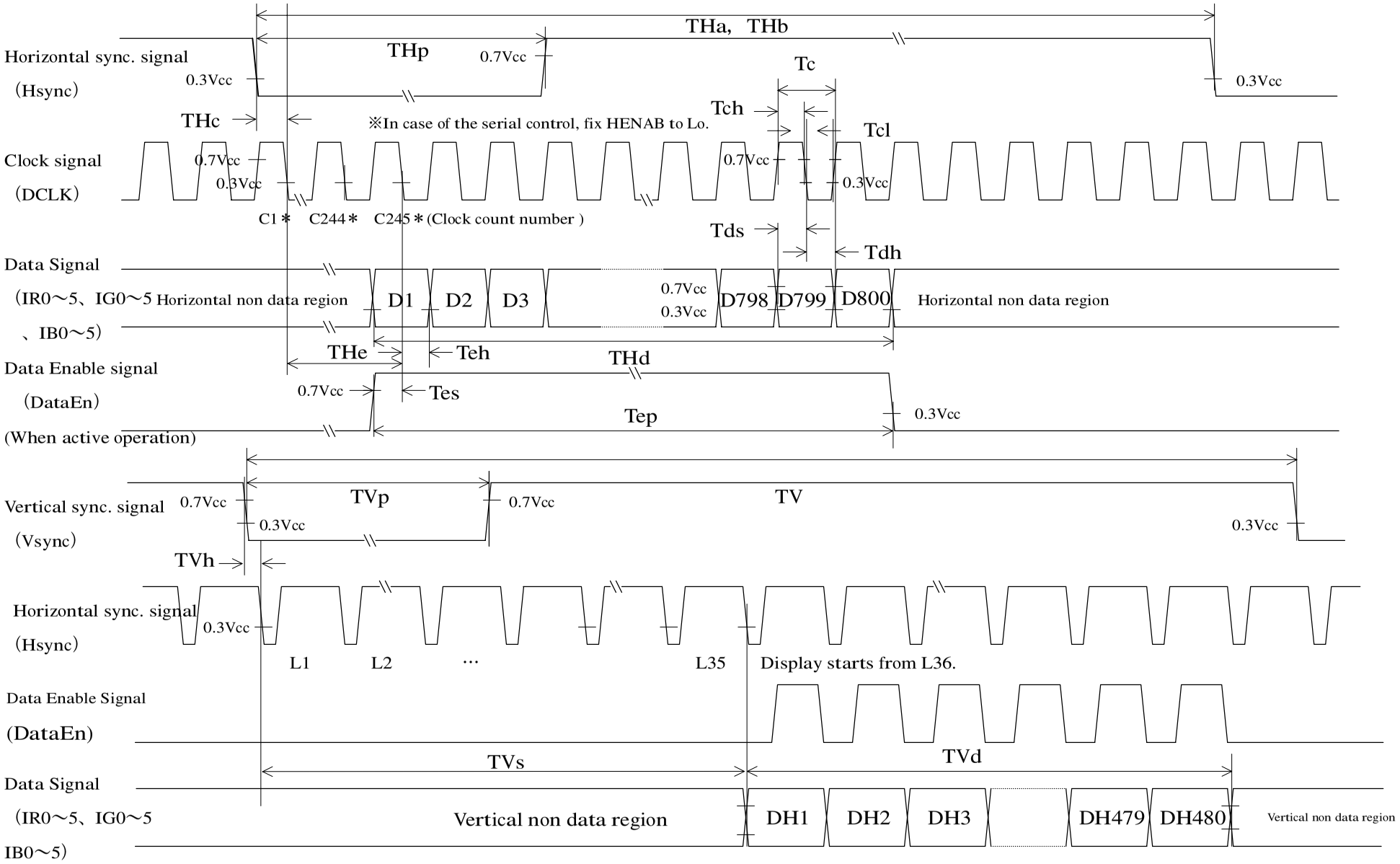


Fig. 2: Input timing chart when setting the Horizontal display starting position by entering DataEn signal

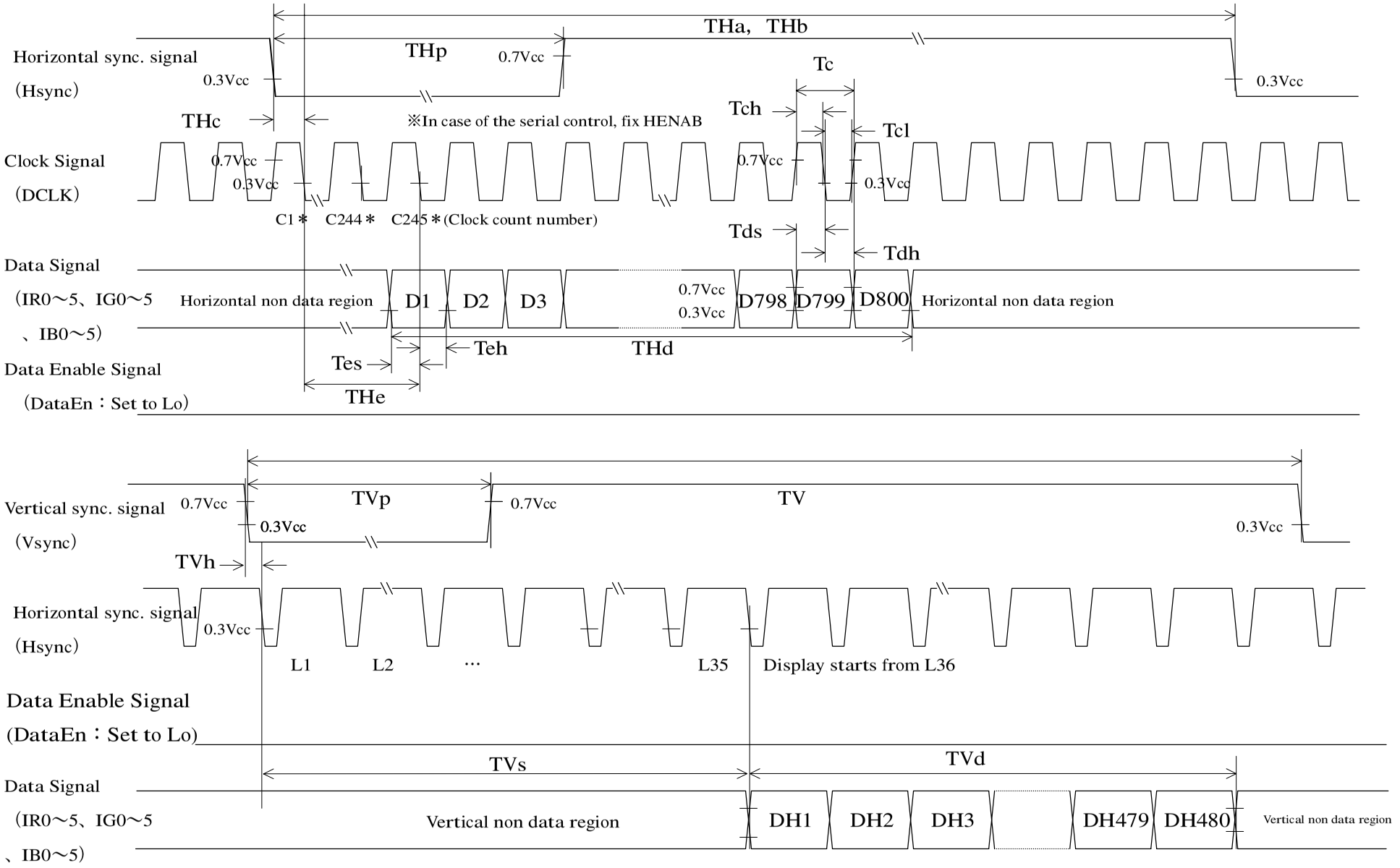
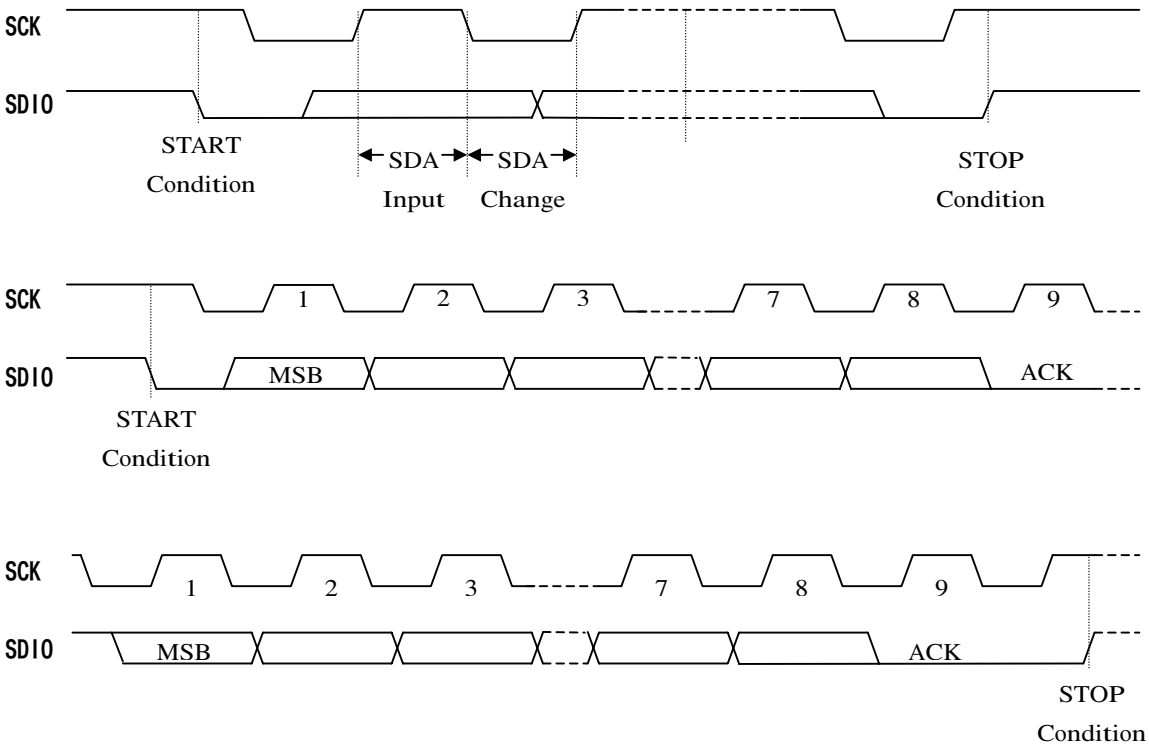


Fig. 3: Input timing chart when setting the Horizontal display starting position by serial communication

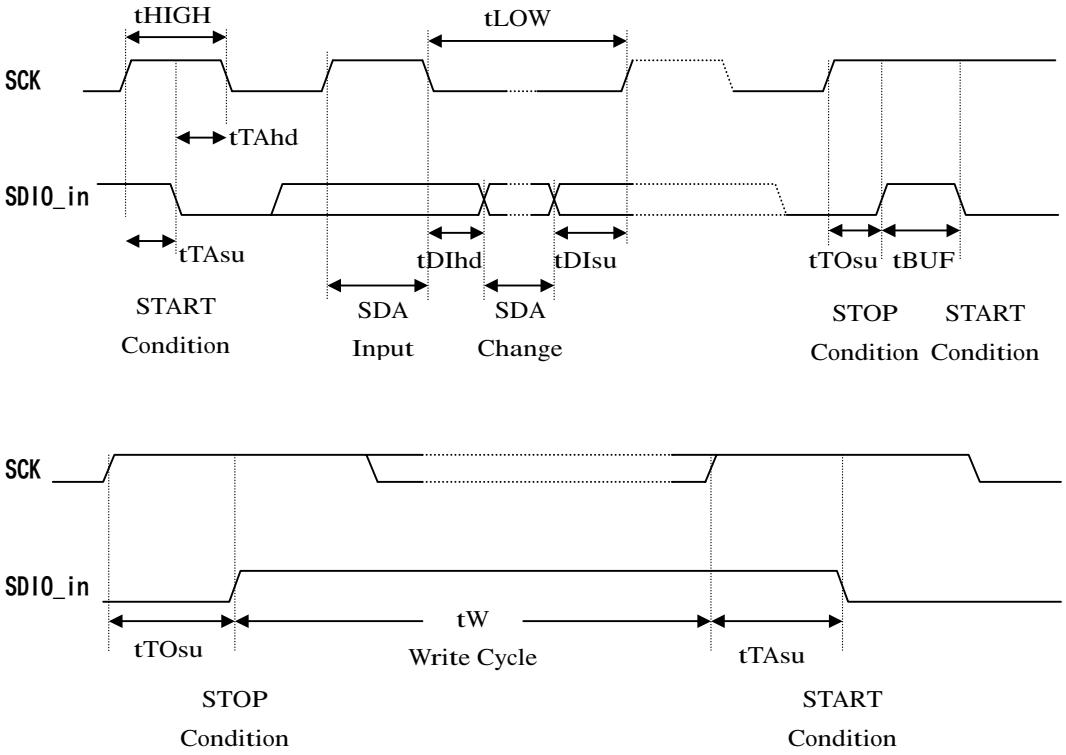
7. Input of the Serial Data

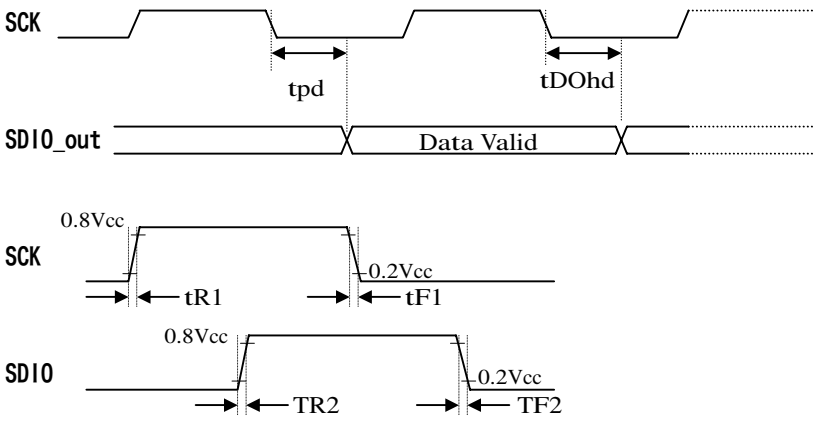
7 - 1 I²C Protocol



Read / Write from or to the internal register of C-IC and EEPROM is to be done using the dual line type (I²C – Bus type) serial communication.

7-2 AC characteristics of the serial interface

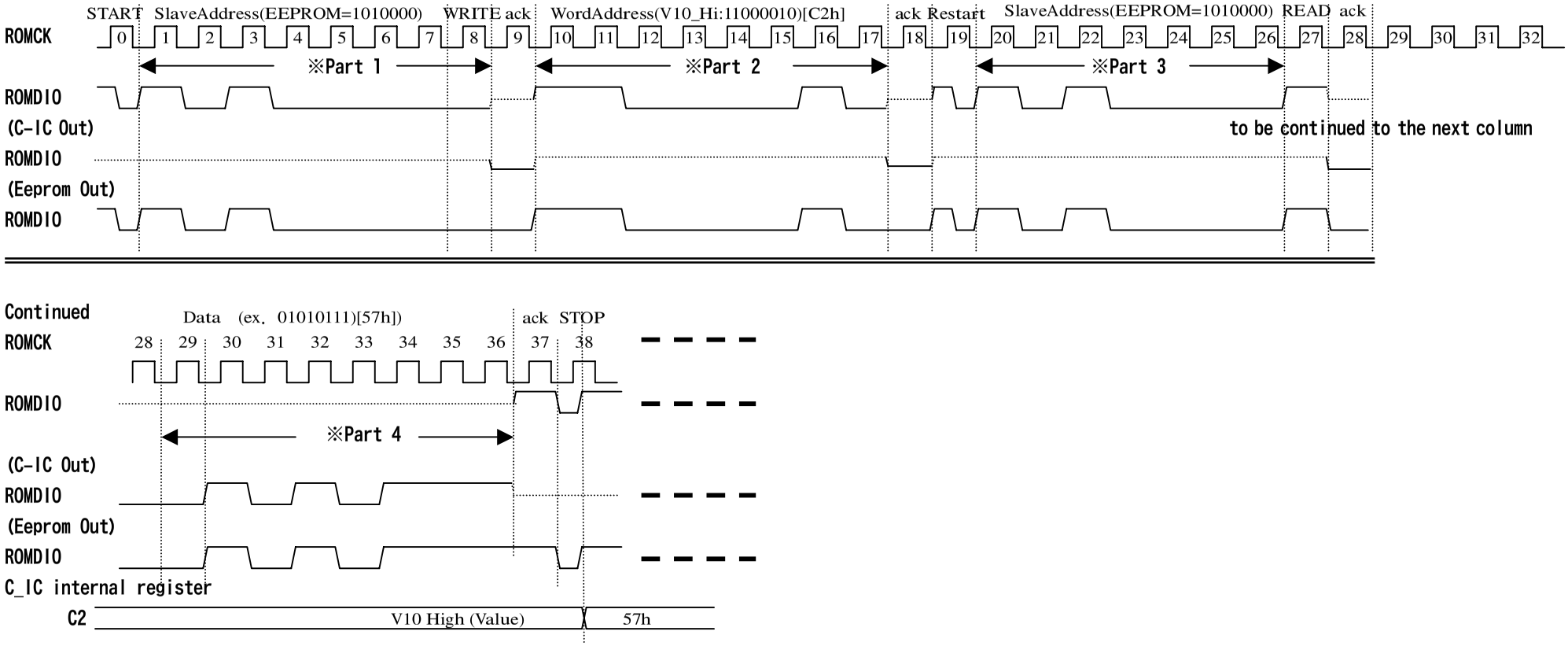




Operation Timing　Vcc:3.0～3.6V　Ta:－40～85ºC

Item	Symbol	Min.	Max.	Unit
Clock Frequency	fSCK		400	kHz
Data clock “Hi” period	tHIGH	600		ns
Data clock “Lo” period	tLOW	1200		ns
Clock rising time	tR1		300	ns
Clock falling time	tF1		300	ns
Data rising time	tR2	20	300	ns
Data falling time	tF2	20	300	ns
Input data set-up time	tDIsu	100		ns
Input data hold time	tDIhd	0		ns
Output data hold time	tDOhd	200		ns
Output data delay time	tpd	200	900	ns
Start condition set-up time	tTAsu	600		ns
Start condition hold time	tTAhd	600		ns
Stop condition set-up time	tTOsu	600		ns
Bus open timing before transfer	tBUF	1300		ns
Writing time	tW		10	ms

7-3 Example for EEPROM read out timing at the initialization of C-IC (for 1 WORD)



● Flow at the initialization of C-IC (under the condition that the original clock is input to C-IC other than serial input, at the initialization)

① The device ID signal is output from C-IC in order to access to EEPROM. Slave setting '1010000' (Chip Enable '000') (※Part 1)

② Following to the above, the command is output (from C-IC) to instruct the internal address C2h in EEPROM. (※Part 2)

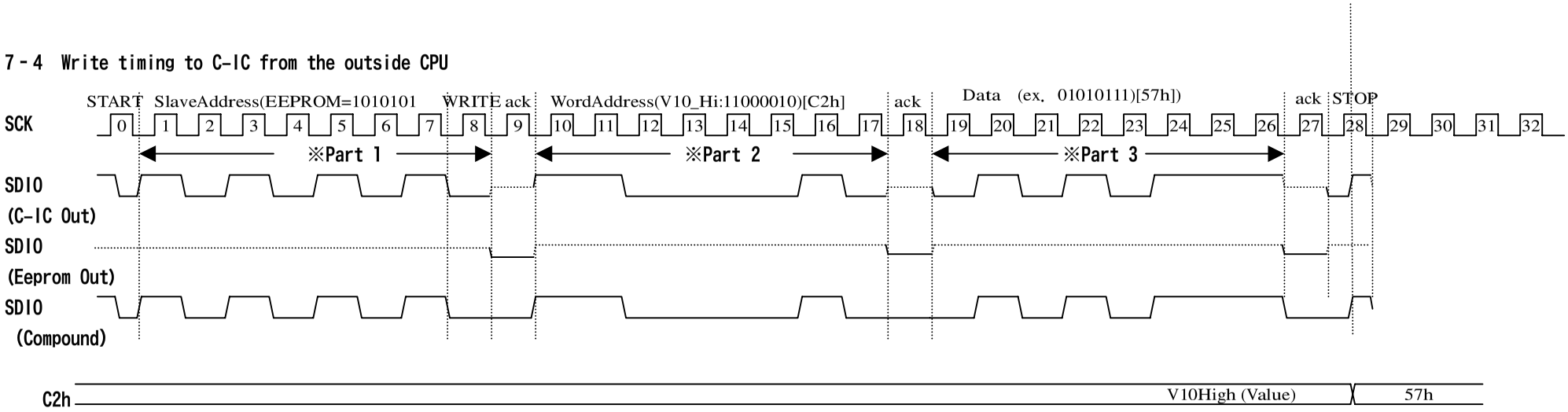
③ Next, the command to read the data in the address (C2h) of EEPROM. (It is for 'slave address' + 'R/W', and does not transmit the address for the C-IC internal register.) (※Part 3)

④ When EEPROM receives the above command, EEPROM outputs the data stored in the C2h address of EEPROM (Here it is designated as 57h.) to C-IC. (※Part 4)

⑤ After C-IC internal register receives the above data, and after STOP condition, the data to designate the V10_High (57h : data to write to DAC) is output from C-IC, and the series of the EEPROM internal data are written to the C-IC internal register, and thus the operation to finish the DAC adjustment is completed.

By repeating the steps of ①～⑤, the initialization of the C-IC internal register is carried out. Therefore, the address designation of EEPROM is to be (C2h, C4h, C6h…E0h).

7 - 4 Write timing to C-IC from the outside CPU



● Flow of the command from the external CPU to C-IC (under the condition that the original clock is input to C-IC other than serial input)

① The device ID signal to access to C-IC is output from the outer CPU. Slave setting '1010101' (Chip Enable '101') (※Part 1)

② Following to the above, the command is output to instruct the internal address C2h in C-IC. (※Part 2)

③ The data is transferred to the designated C-IC internal register address. (The data and the address designation is to be done by the host CPU.)
After the C-IC internal register receives the above data and after the STOP condition, C-IC outputs the data to designate the V10_High (57h : data to write to DAC) and set the data which is completed to write to DAC, and thus the series of the operation is completed.

By repeating the steps of above ①～③, the C-IC internal register is initialized. Therefore the designation of the C-IC internal register address is to be (C2h, C4h, C6h…E0h).

7 - 5 Timing of the serial transmission

1. Regarding the polarity of SERCS and SERWC and the possibility to read / write of the EEPROM / C-IC internal register

SCS	WC	ROM_Write	ROM_Read	C-IC_Write	C-IC_Read
0	1	×	○	○	○
1	0	○	○	×	○
0	0	○	○	○	○
1	1	×	○	×	○

※ 1：In case the change of the address value designated by C-IC internal register is not desired, SERCS is to be fixed to Hi. When desired to change, it is to be fixed to Lo for the period designated below.

※ 2：In case the change of the address value designated by EEPROM is not desired, SERWS is to be fixed to Hi. When desired to change, it is to be fixed to Lo for the period designated below.

2. Timing of the SERCS and SERWC signals when writing to the designated address in the C-IC internal register and in EEPROM

※ T1, T2 ≧ 5μs

100kHz：1CK=10μs

400kHz：1CK=2.5μs

7-6 Functions of C-IC internal register (Slave address1010101) ※ Chip Enable = '101'

Command List

	Address	Data address								Initial value		
Command	[HEX]	D7	D6	D5	D4	D3	D2	D1	D0	[HEX]	Variable range	Note
V10 P/S High set	C2h	Dac4ch (Contrast) adjustable amount (0-255 Scale)								3Bh	00h-FFh	→7-6-1
V10 P/S Low set	C4h	Dac3ch (Contrast) adjustable amount (0-255 Scale)								EDh	00h-FFh	
V3 P/S High set	C6h	Dac2ch (Gamma) adjustable amount (0-255 Scale)								A1h	00h-FFh	→7-6-2
V3 P/S Low set	C8h	Dac1ch (Gamma) adjustable amount (0-255 Scale)								65h	00h-FFh	
COM amplitude High set	CAh	Dac7ch (Bright) adjustable amount (0-255 Scale)								11h	00h-FFh	→7-6-3
COM amplitude Low set	CCh	Dac6ch (Bright) adjustable amount (0-255 Scale)								EFh	00h-FFh	
Red data offset	CEh	POL	*	Red data offset amount (0-63 scale)						00h	00h-3Fh 80h-BFh	→7-6-4
Green data offset	D0h	POL	*	Green data offset amount (0-63 scale)						00h		
Blue data offset	D2h	POL	*	Blue data offset amount (0-63 scale)						00h		
Horizontal display starting position	D4h	Horizontal display starting position adjustable amount (188-244ck)								FFh	BCh-F4h	→7-6-5
Vertical display starting position	D6h	*	*	Vertical display starting position adjustable amount (10-35L)						23h	0Ah-23h	→7-6-6
Switching instruction of scanning direction	D8h	*	*	*	*	*	RSEL	VRVC	HRVC	00h	00h-07h	→7-6-7
Setting of display test pattern	DEh	TEN	*	*	P4	P3	P2	P1	P0	00h	80-88h, 98-9Fh	→7-6-8
COMDC adjust	E0h	Dac5ch (COMDC) adjustable amount (0-255 scale)								78h	00h-FFh	→7-6-9

※① The 3 bits of the Chip Enable are for the selection of the devises and can be set Max. 8 selections on the same Bus. In this ASIC, either one of the 2 devises, namely C-IC internal register or EEPROM, can be selected. (The Chip Enable of EEPROM is '000'.) 「Chip Enable」 corresponds to the lower 3 bits of the slave address.

7-6-1 V10 amplitude [Whiteness] adjustment [C-IC internal register address: C2h, C4h]

Command	Data adjustable amount 255 scales	Data address value (D7-D0)								
		Low	←←←			Typ.	→→→			High
V10 P/S amplitude High set	[00h-FFh]	7Dh	←		←	43h	→		→	38h
V10 P/S amplitude Low set	[00h-FFh]	94h	←		←	E1h	→		→	F5h
Initial setting at SHARP shipment						○				

"[V10 P/S amplitude High set]-[V10 P/S amplitude Low set]" can be used for the contrast adjustment.

【Note】 V10 power supply amplitude adjustment has to be done within the range of the discrete value which will be submitted separately. In case it is not adjusted by the recommended value, degrading of the display (flicker, etc.) may be occurred.

7-6-2 V3 amplitude [Middle tone] adjustment [C-IC internal register address: C6h, C8h]

Command	Data adjustable amount 255 scales	Data address value (D7-D0)								
		Bright	←←←			Typ.	→→→			Dark
V3 P/S amplitude High set	[00h-FFh]	90h	←		←	9Dh	→		→	DCh
V3 P/S amplitude Low set	[00h-FFh]	7Bh	←		←	67h	→		→	21h
Initial setting at SHARP shipment						○				

"[V3 P/S amplitude High set]-[V3 P/S amplitude Low set]" can be used for the contrast adjustment.

【Note】 V10 power supply amplitude adjustment has to be done within the range of the discrete value which will be submitted separately. In case it is not adjusted by the recommended value, degrading of the display (flicker, etc.) may be occurred.

7-6-3 COM amplitude adjustment [C-IC internal register address: CAh, CCh]

Command	Data adjustable amount 255 scales	Data address value (D7-D0)								
		Bright	←←←			Typ.	→→→			Dark
COM signal amplitude High set	[00h-FFh]	42h	←		←	0Eh	→		→	00h
COM signal amplitude Low set	[00h-FFh]	BEh	←		←	F2h	→		→	FFh
Initial setting at SHARP shipment						○				

"[COM signal amplitude High set]-[COM signal amplitude Low set]" can be used for the adjustment of Brightness.

7-6-4 White Balance adjustment [C-IC internal register address: CEh, D0h, D2h]

Command	Data adjustable amount 64 scales	Data address value (D7-D0)				
		Bright	←	Typical	→	Dark
Red data offset amount Green data offset amount Blue data offset amount	"0*000000" ～ "0*111111" [00h-3Fh]	"0*111111" [3Fh] or [7Fh]	←	"**000000" [00h] or [80h], etc.	—	—
Red data offset amount Green data offset amount Blue data offset amount	"1*000000" ～ "1*111111" [00h-3Fh]	—	—		→	"1*111111" [BFh] or [FFh]
Initial setting at SHARP shipment				○ [00h]		

Example: When desired to brighten green by 3 scales, by setting the C-IC internal register address D0h to "D7-D0：03h(POL：0)", the output data becomes to 28 scales at the input data of 25 scales.
When desired to darken blue by 34 scales, by setting the C-IC internal register address D2h to "D7-D0：A2h(POL：1)", the output data becomes to 0 scale at the input data of 25 scales.
(When the data offset amount is big, the lower limit of the output data becomes to 0 scales and the upper limit becomes to 63 scales.)
*：This can be either 0 or 1.

7-6-5 Horizontal display starting position adjustment [C-IC internal register address: D4h]

Command	Data adjustable amount 57 pixels	Data address value (D7-D0)				
		Min.	※Display shifts to right	※Display at center	※Display shifts to left	Max.
Horizontal display starting position adjustment	[BCh-F4h]	[BCh]	←	[D8h]	→	【Note】[F4h]
Initial setting at SHARP shipment						○ [FFh]

※ This table shows the display status when the horizontal display starting position is set to THe=216(ck), correctly.

"THe" is defined as the ck numbers from the fall time of Hsync signal to the rise time of the DataEn signal. (Refer to P.9 Fig.2 and P.10 Fig.3)
When the setting of the horizontal display starting position "THe" is 188[BCh]ck, the 189th picture data from the Hsync signal becomes the data for the first pixel of the display of the module.
【Note】 As the initial setting at SHARP shipment, the data value FFh is written in the D4h address of EEPROM, but when this data is read by C-IC, it is so designed that the Horizontal display starting position "THe" becomes to F4h.

- In case the Horizontal display starting position (THe) is set by the serial communication:
  DataEn signal has to be set to 'Lo'. If not 'Lo', there is a case that the display may become improper or other functions may not be used.
  When 'THe' is set to the lower number than 188ck, the data value is set to 188[BCh] in the C-IC, and when it is bigger than 244ck, it is set to 244[F4h].
  【Note】 Input data value [BCh-F4h] to the EEPROM_D4h address corresponding to the displayed signal.
- In case the Horizontal display starting position (THe) is set by the rise time of the DataEn signal:
  Control the signal as 'THe' value becomes 188～244[BCh-F4h]ck. If the signal other than this range is input, the display may not be proper.
  【Note】 Input the data value of [FFh] to the EEPROM_D4h address.

7-6-6 Vertical display starting position adjustment [C-IC internal register address: D6h]

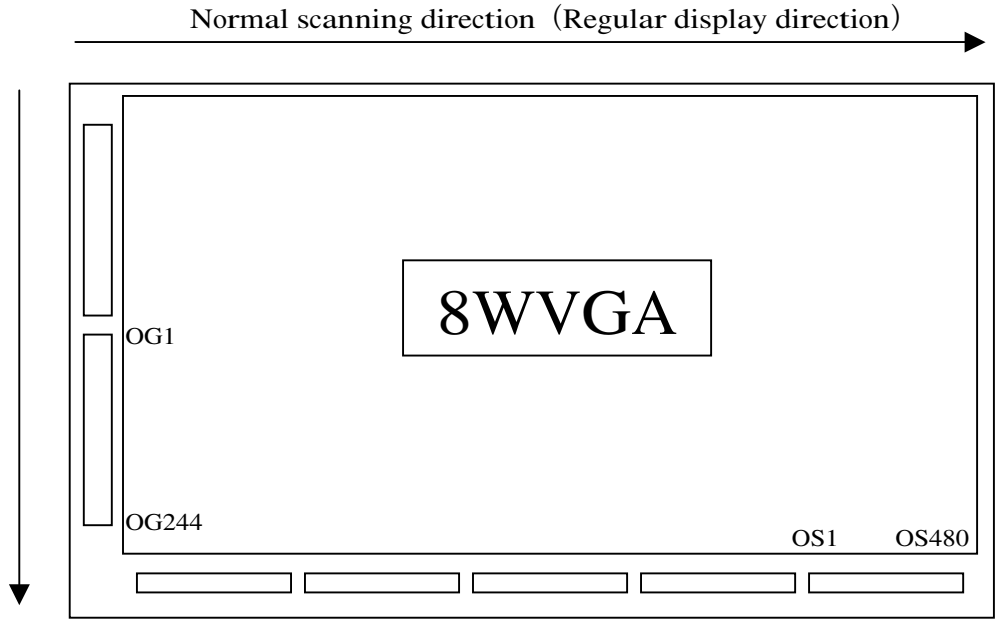
Command	Data adjustable amount 26Line	Data address value (D7-D0)				
		Min.	※Display shifts to lower	※Display at center	※Display shifts to upper	Max.
Vertical display starting position adjustment	[0Ah-23h]	[0Ah]	←	[17h]	→	[23h]
Initial setting at SHARP shipment						○

※ This table shows the display status when the vertical display starting position is set to TVs=23(Line), correctly.
"TVs" is defined as the line number from the fall time of Vsync signal to the Vertical display starting position. (Refer to P.9 Fig.2 and P.10 Fig.3)When the Vertical display starting position "TVs" is 10[0Ah]Line, the picture data from 11th line is displayed.

7-6-7 Horizontal / Vertical scanning direction switching [C-IC internal register address: D8h]

Panel display status	RSEL[D2]	VRVC[D1]	HRVC[D0]	Priority	Initial setting at SHARP shipment
Regular Video	0	—	—	Setting of PWB circuit	○
Horizontally / Vertically inverted video	1	0	0	Setting of serial communication input	
Vertically inverted video	1	0	1	Setting of serial communication input	
Horizontally inverted video	1	1	0	Setting of serial communication input	
Regular Video	1	1	1	Setting of serial communication input	

※ As the data address value uses only lower 3 bits, it is indicated by the binary code.



When RSEL=0, the setting of the PWB circuit has the priority. When RSEL=1, the input of the serial communication has the priority.
When VRVC=0, the gate driver is in the reverse scan mode and when VRVC=1, the gate driver is in the normal scan mode. When HRVC=0, the source driver is in the reverse scan mode and when HRVC=1, the source driver is in the normal scan mode.

7-6-8 Display test pattern setting [C-IC internal register address: DEh]

Pattern Name	Data address lower 5 bits						Data address value	Explanation of the test pattern
	TEN	P4	P3	P2	P1	P0		
Whole red	1	0	0	0	0	0	80h	Whole red 800dot×480Line (63 Scales)
Whole green		0	0	0	0	1	81h	Whole green 800dot×480Line (63 Scales)
Whole blue		0	0	0	1	0	82h	Whole blue 800dot×480Line (63 Scales)
Whole black		0	0	0	1	1	83h	Whole black 800dot×480Line (0 Scales)
Cross hatch 1		0	0	1	0	0	84h	1 square 40Lines×40dots Black background & white lines (Line width: 2 dots×2 Lines)
8 Scales gray bar		0	0	1	0	1	85h	Display 0,9,18,27,36,45,54,63 Scales at every 100 dots from left
8 Scales color bar		0	0	1	1	0	86h	Display white, yellow, cyan, green, magenta, red, blue and black at every 100 dots from left
Check		0	0	1	1	1	87h	5 Columns×5 Rows (160pixels×96Lines) Check Black and white pattern
Whole white		0	1	0	0	0	88h	Whole white 800dot×480Line。 (63 Scales)
Sweep		1	1	0	0	0	98h	Display black and white vertical lines at the interval of 128,64,32,16,8,4,2,1 pixels from left
Cross hatch 2		1	1	0	0	1	99h	1 square 40Lines×40dots white background & black lines (Line width: 2 dots×2 Lines)
64 Scales horizontal		1	1	0	1	0	9Ah	Gray pattern degrading by 64 scales in the horizontal direction
64 Scales vertical		1	1	0	1	1	9Bh	Gray pattern degrading by 64 scales in the vertical direction
Flicker		1	1	1	0	0	9Ch	Display pattern to be able to detect flickers at every 8 scales
Outer frame display		1	1	1	0	1	9Dh	Display judge mark of the outer frame (2dots×2Lines) and the scanning direction. Judge mark: LEFT
Shadow check		1	1	1	1	0	9Eh	Display rectangles of gray scale (V21) against the background of (V42). 1:2:1
Current consumption		1	1	1	1	1	9Fh	Pattern that the black and white of 18 bits video is inverted at every 1H1V

- When TEN=0, displays the video input from the RGB input terminal at the normal display mode.
- When TEN=1, displays the test pattern designated by the lower 5 bits of the data address. The test pattern is generated by the internal signal which is made by C-IC internal counter and it is not made based on the external signals such as Hsync, Vsync, DataEn, etc. (DCLK signal has to be input.)

When back to the normal display mode from the test pattern display, input TEN=0 again by the serial communication. When display the test pattern, it is not possible to adjust RGB data offset. (Possible to adjust Horizontal display starting position, V10 power supply High set and other items.)

7-6-9 COMDC adjustment [C-IC internal register address: E0h]

Command	Data adjust amount 256 scales	Data address value (D7-D0)				
		Min.	Flickering	No flicker	Flickering	Max.
COMDC adjustment	[00h-FFh]	[00h]	←	Typ. [78h]	→	[FFh]
Initial setting of SHARP shipment				○【Note】		

【Note】 This COMDC adjustment is set to the best value at the shipment of the module. As this value is different to each panel, do not change the value at the shipment from SHARP. (The set value is written to EEPROM_E0 address.) Furthermore, when this set value is changed, it may create the degrading of the display .(happenings of flicker)

7-6-10 Others

- Write mode to C-IC：「Byte Write」
- Read mode from C-IC：「RANDOM ADDRESS READ」(Only one data at a time)
- Even if the EEPROM data is not read, the initial value of the internal register is reflected after the release of FREST signal.
- When write to C-IC, set the slave address to 1010101.
- The designated address of EEPROM is set as the address of the C-IC internal register.
- When rewriting the C-IC internal register value, it does not operate without the input of DCLK signal other than the input of the serial signal.

7-7 EEPROM register functions (Slave address 1010101) ※ Chip Enable = '101'

7-7-1 EEPROM register table

Data block	Address	Byte no.	Explanation	Type	Action
Data structure	00h	1	EDID structure Version / Revision	Binary	R
Data for recognition	01h	1-2	ID maker name (EISA 3)	Binary	R
	03h	1-2	ID product code(Specifications number)	※	R
	05h	1	week of Manufacture	Binary	R
	06h	1-2	year of Manufacture	Binary	R
	08h	1-21	Maker / Model part number	ASCII	R
	1Dh	1-8	SHARP process control number registration	Binary	R
	25h	1-27	RB coefficient for Grafic Controller LUT	Binary	R
Display interface parameter	40h	1	Physical Interface Type	Binary	R
	41h	1	Video Interface Type	Binary	R
	42h	1-8	Interface Data Format	Binary	R
	4Ah	1-5	Interface Color/Luminance Encoding	Binary	R
Description of the display devises	4Fh	1	Display technology type / sub-type	Binary	R
	50h	1	Major Display Characteristics	Binary	R
	51h	1-3	Features Support	Binary	R
	54h	1-2	Display Response Time	Binary	R
Description of color / brightness	56h	1-4	Display Transfer Characteristic /γ	Binary	R/W
	5Ah	1-4	Maximum Luminance and Offset	Binary	R
	5Eh	1-10	Colorimetry / White Points (63 gray scale)	Binary	R/W
	68h	1-10	SHARP process control number registration	Binary	R/W
Display Spatial Description	72h	1-4	Max. Image Size (mm)	Binary	R
	76h	1-4	Max. Addressibility (pixels)	Binary	R
	7Ah	1-2	Dot / Pixel Pitch (mm×100)	Binary	R
	7Ch	1	Unused (Reserved)	Binary	R
	7Dh	1	GTF Support Information	Binary	R
	7Eh	1-2	Map Of Timing Information	Binary	R
Luminance Table	80h	1-65	Luminance Table	Binary	R/W
C-IC Address Map°	C1h	1-32	Initial Data Input Space For C-IC	Binary	R/W
Timing description	E1h	1-27	Range limit	Binary	R
	FCh	1-3	Unused	Binary	R
Check Sum	FFh	1	Check sum of all "256 bytes = 0" / Total	Binary	R/W

※ 03h: Binary, 04h: ASCII

7-7-2 EEPROM initial value setting table

Address		EEPROM Data value (binary)								hex	Description of the register address
Deci	hex	E7	E6	E5	E4	E3	E2	E1	E0		
0	00h	0	0	1	0	0	0	0	0	20h	EDID Structure 2 Revision 0
1	01h	0	1	0	0	1	1	0	1	4Dh	EISA manufacturer Code (Low Byte)
2	02h	0	0	0	0	0	0	0	0	00h	(High Byte)
3	03h	0	0	0	1	1	0	0	0	18h	Product code=Sharp Product/Version Number (Product)
4	04h	0	1	0	0	0	0	0	1	41h	(Version) [Product : binary, Version : ASCII] [default]
5	05h	0	0	0	1	0	1	1	0	16h	Week of manufacture (ex. 2004/6/28)
6	06h	1	1	0	1	0	1	0	0	D4h	Year of manufacture (low Byte)
7	07h	0	0	0	0	0	1	1	1	07h	(high Byte) [TBD, default]
8	08h	0	1	0	1	0	0	1	1	53h	1st character of ID String [S] Maker Name :
9	09h	0	1	0	0	1	0	0	0	48h	2nd character of ID String [H] 【SHARP】
10	0Ah	0	1	0	0	0	0	0	1	41h	3rd character of ID String [A]
11	0Bh	0	1	0	1	0	0	1	0	52h	4th character of ID String [R]
12	0Ch	0	1	0	1	0	0	0	0	50h	5th character of ID String [P]
13	0Dh	0	0	0	0	1	0	0	1	09h	6th character of ID String [<Tab>]
14	0Eh	0	1	0	0	1	1	0	0	4Ch	7th character of ID String [L] Model part number
15	0Fh	0	1	0	1	0	0	0	1	51h	8th character of ID String [Q] 【LQ080Y5DR02】
16	10h	0	0	1	1	0	0	0	0	30h	9th character of ID String [0]
17	11h	0	0	1	1	1	0	0	0	38h	10th character of ID String [8]
18	12h	0	0	1	1	0	0	0	0	30h	11th character of ID String [0]
19	13h	0	1	0	1	1	0	0	1	59h	12th character of ID String [Y]
20	14h	0	0	1	1	0	1	0	1	35h	13th character of ID String [5]
21	15h	0	1	0	0	0	1	0	0	44h	14th character of ID String [D]
22	16h	0	1	0	1	0	0	1	0	52h	15th character of ID String [R]
23	17h	0	0	1	1	0	0	0	0	30h	16th character of ID String [0]
24	18h	0	0	1	1	0	0	1	0	32h	17th character of ID String [2]
25	19h	0	0	1	0	0	0	0	0	20h	18th character of ID String [ ]
26	1Ah	0	0	1	0	0	0	0	0	20h	19th character of ID String [ ]
27	1Bh	0	0	1	0	0	0	0	0	20h	20th character of ID String [ ]
28	1Ch	0	0	1	0	0	0	0	0	20h	21th character of ID String [ ] [TBD, default]
29	1Dh	-	-	-	-	-	-	-	-	--h	Sharp Internal Check up registers for Mass Production
30	1Eh	-	-	-	-	-	-	-	-	--h	Sharp Internal Check up registers for Mass Production
31	1Fh	-	-	-	-	-	-	-	-	--h	Sharp Internal Check up registers for Mass Production
32	20h	0	0	0	0	1	1	1	1	0Fh	Sharp Internal Check up registers for Mass Production
33	21h	0	0	0	1	0	0	0	1	11h	Sharp Internal Check up registers for Mass Production
34	22h	-	-	-	-	-	-	-	-	--h	Sharp Internal Check up registers for Mass Production
35	23h	-	-	-	-	-	-	-	-	--h	Sharp Internal Check up registers for Mass Production
36	24h	1	1	1	1	1	1	1	1	FFh	Sharp Internal Check up registers for Mass Production
37	25h	0	0	0	0	0	0	0	0	00h	RB coefficient for Grafic Controller LUT Red0
38	26h	0	0	0	0	1	0	0	0	08h	RB coefficient for Grafic Controller LUT Red1
39	27h	0	0	0	1	0	0	0	0	10h	RB coefficient for Grafic Controller LUT Red2
40	28h	0	0	0	1	1	0	0	0	18h	RB coefficient for Grafic Controller LUT Red3
41	29h	0	0	1	0	0	0	0	0	20h	RB coefficient for Grafic Controller LUT Red4
42	2Ah	0	0	1	0	1	0	0	0	28h	RB coefficient for Grafic Controller LUT Red5
43	2Bh	0	0	1	1	0	0	0	0	30h	RB coefficient for Grafic Controller LUT Red6
44	2Ch	0	0	1	1	1	0	0	0	38h	RB coefficient for Grafic Controller LUT Red7
45	2Dh	0	1	0	0	0	0	0	0	40h	RB coefficient for Grafic Controller LUT Red8
46	2Eh	0	0	0	0	0	0	0	0	00h	RB coefficient for Grafic Controller LUT Green0
47	2Fh	0	0	0	0	1	0	0	0	08h	RB coefficient for Grafic Controller LUT Green1
48	30h	0	0	0	1	0	0	0	0	10h	RB coefficient for Grafic Controller LUT Green2
49	31h	0	0	0	1	1	0	0	0	18h	RB coefficient for Grafic Controller LUT Green3
50	32h	0	0	1	0	0	0	0	0	20h	RB coefficient for Grafic Controller LUT Green4
51	33h	0	0	1	0	1	0	0	0	28h	RB coefficient for Grafic Controller LUT Green5
52	34h	0	0	1	1	0	0	0	0	30h	RB coefficient for Grafic Controller LUT Green6
53	35h	0	0	1	1	1	0	0	0	38h	RB coefficient for Grafic Controller LUT Green7
54	36h	0	1	0	0	0	0	0	0	40h	RB coefficient for Grafic Controller LUT Green8

Address		EEPROM Data value (binary)								hex	Description of the register address
Deci	hex	E7	E6	E5	E4	E3	E2	E1	E0		
55	37h	0	0	0	0	0	0	0	0	00h	RB coefficient for Grafic Controller LUT Blue0
56	38h	0	0	0	0	1	0	0	0	08h	RB coefficient for Grafic Controller LUT Blue1
57	39h	0	0	0	1	0	0	0	0	10h	RB coefficient for Grafic Controller LUT Blue2
58	3Ah	0	0	0	1	1	0	0	0	18h	RB coefficient for Grafic Controller LUT Blue3
59	3Bh	0	0	1	0	0	0	0	0	20h	RB coefficient for Grafic Controller LUT Blue4
60	3Ch	0	0	1	0	1	0	0	0	28h	RB coefficient for Grafic Controller LUT Blue5
61	3Dh	0	0	1	1	0	0	0	0	30h	RB coefficient for Grafic Controller LUT Blue6
62	3Eh	0	0	1	1	1	0	0	0	38h	RB coefficient for Grafic Controller LUT Blue7
63	3Fh	0	1	0	0	0	0	0	0	40h	RB coefficient for Grafic Controller LUT Blue8
64	40h	1	1	1	1	0	0	0	0	F0h	Default physical interface
65	41h	0	1	1	0	0	0	0	0	60h	Default Video Interface=6+no secondary Interface
66	42h	1	0	0	1	0	0	0	0	90h	Interface Speed and polarity
67	43h	0	0	0	1	1	0	1	0	1Ah	Minimum Speed:26MHz
68	44h	0	0	1	0	0	0	1	1	23h	Maximum Speed:35MHz
69	45h	0	0	1	0	0	0	0	0	20h	Digital Interface Data = pseudo 18 bit MSB aligned TFT
70	46h	0	0	0	0	0	0	0	0	00h	Reserved for opt.secondary Interface
71	47h	0	0	0	0	0	0	0	0	00h	Reserved for opt.secondary Interface
72	48h	0	0	0	0	0	0	0	0	00h	Reserved for opt.secondary Interface
73	49h	0	0	0	0	0	0	0	0	00h	Reserved for opt.secondary Interface
74	4Ah	0	0	0	1	0	0	0	1	11h	Color Space used = RGB
75	4Bh	0	1	1	0	0	1	1	0	66h	Color Depth Red/Green Primary Interface
76	4Ch	0	1	1	0	0	0	0	0	60h	Color Depth Blue Primary Interface
77	4Dh	0	0	0	0	0	0	0	0	00h	Color Depth Red/Green Secondary Interface
78	4Eh	0	0	0	0	0	0	0	0	00h	Color Depth Blue Secondary Interface
79	4Fh	0	0	0	1	0	0	1	1	13h	Display Technology Type
80	50h	1	0	0	0	1	0	1	1	8Bh	Display Major Charactersitics
81	51h	0	0	0	0	0	0	0	0	00h	Display Feature Support (Power modes)
82	52h	0	0	0	0	0	0	0	0	00h	Display Feature Support (Audio/Video Inputs)
83	53h	0	0	1	0	0	0	0	0	20h	Display Feature Support (additional Features)
84	54h	0	0	0	1	1	1	1	0	1Eh	Display Response Time (Rise Time) Tamb.25° : Typ.30ms
85	55h	0	0	1	1	0	0	1	0	32h	Display Response Time (Fall Time) Tamb.25° : Typ.50ms
86	56h	0	1	1	1	1	0	0	0	78h	White Gamma (C sample γ=2.2±20%) [2.2×100-100→hex]
87	57h	0	1	1	0	0	1	0	0	64h	Color 0 (Red) Gamma (optional)
88	58h	0	1	1	0	0	1	0	0	64h	Color 1 (green) Gamma (Optional)
89	59h	0	1	1	0	0	1	0	0	64h	Color 3 (blue) Gamma (Optional)
90	5Ah	1	0	0	0	1	0	0	0	88h	Min.Luminance (white) (Low Byte) [500cd×10=1388h]
91	5Bh	0	0	0	1	0	0	1	1	13h	(High Byte)
92	5Ch	1	1	0	0	0	0	0	0	C0h	Standard RGB+Adjustable Gamma
93	5Dh	0	0	0	0	0	0	0	0	00h	Offset Value
94	5Eh	1	0	0	0	1	0	0	1	49h	Chromaticity Red/Green (Low 2 bits) [60-63h address]
95	5Fh	1	1	1	1	0	1	0	1	F5h	Chromaticity Blue/White (Low 2 bits) [64-67h address]
96	60h	1	0	0	1	0	1	1	0	96h	Chromaticity coordinate Red x (63 gray scale)
97	61h	0	1	0	1	0	1	1	0	56h	Chromaticity coordinate Red y (63 gray scale)
98	62h	0	1	0	0	1	1	0	1	4Dh	Chromaticity coordinate Green x (63 gray scale)
99	63h	1	0	0	0	1	1	0	0	8Ch	Chromaticity coordinate Green y (63 gray scale)
100	64h	0	0	1	0	0	1	1	0	26h	Chromaticity coordinate Blue x (63 gray scale)
101	65h	0	0	1	0	0	0	0	0	20h	Chromaticity coordinate Blue y (63 gray scale)
102	66h	0	1	0	1	0	0	0	0	50h	Chromaticity coordinate White x (63 gray scale)
103	67h	0	1	0	1	0	0	0	0	50h	Chromaticity coordinate White y (63 gray scale)

Chromaticity coordinate ・・・
Average value

	Red	Green	Blue	White
X	0.587	0.303	0.152	0.313
Y	0.336	0.548	0.128	0.329

Address		EEPROM Data value (binary)								hex	Description of the register address
Deci	hex	E7	E6	E5	E4	E3	E2	E1	E0		
104	68h	0	0	0	0	0	0	0	0	00h	Sharp Internal Check up registers for Mass Production
105	69h	0	0	0	0	0	0	0	0	00h	[00h]
106	6Ah	0	0	0	0	0	0	0	0	00h	Sharp Internal Check up registers for Mass Production
107	6Bh	0	0	0	0	0	0	0	0	00h	Sharp Internal Check up registers for Mass Production
108	6Ch	0	0	0	0	0	0	0	0	00h	[00h]
109	6Dh	0	0	0	0	0	0	0	0	00h	Sharp Internal Check up registers for Mass Production
110	6Eh	0	0	0	0	0	0	0	0	00h	Sharp Internal Check up registers for Mass Production
111	6Fh	0	0	0	0	0	0	0	0	00h	Sharp Internal Check up registers for Mass Production
112	70h	0	0	0	0	0	0	0	0	00h	Sharp Internal Check up registers for Mass Production
113	71h	0	0	0	0	0	0	0	0	00h	Sharp Internal Check up registers for Mass Production
114	72h	1	0	1	0	1	1	1	0	AE	Max. Image Size Horizontal (Low Byte) [174mm→00AEh]
115	73h	0	0	0	0	0	0	0	0	00	(High byte)
116	74h	0	1	1	0	1	0	0	0	68	Max. Image Size Vertical (Low Byte) [104mm→0068h]
117	75h	0	0	0	0	0	0	0	0	00	(High byte)
118	76h	0	0	1	0	0	0	0	0	20h	Max. Horizontal Addressibility (Low Byte)
119	77h	0	0	0	0	0	0	1	1	03h	(High byte) [800 pixels→0320h]
120	78h	1	1	1	0	0	0	0	0	E0h	Max. Vertical Addressibility (Low Byte)
121	79h	0	0	0	0	0	0	0	1	01h	(High byte) [480 pixels→01E0h]
122	7Ah	0	0	0	1	0	1	1	0	16h	Horizontal Pixel Pitch [0.2175 mm→0.22×100→16h]
123	7Bh	0	0	0	1	0	1	1	0	16h	Vertical Pixel Pitch [0.2175 mm→0.22×100→16h]
124	7Ch	0	0	0	0	0	0	0	0	00h	Unused (Reserved by EDID)
125	7Dh	0	0	0	0	0	0	0	0	00h	GTF Support (Generalized Timing Formula) support
126	7Eh	1	1	1	0	0	0	0	1	E1h	Map of Timing Information (2 Byte Information)
127	7Fh	0	0	0	0	0	0	0	0	00h	X*A+8*B+27*C+4*D+18*E (A=1, B=0, C=1, D=0, E=0)
128	80h	0	0	1	1	1	1	1	1	3Fh	Lumimance / Entries and Channels
129	81h	0	0	0	0	0	0	0	0	00h	0 gray scale Luminance Value (White) (V0level)
130	82h	0	0	0	0	0	0	0	0	00h	1 gray scale Luminance Value (White) [255×2/625=0=00h]
131	83h	0	0	0	0	0	0	0	0	00h	2 gray scale Luminance Value (White)
132	84h	0	0	0	0	0	0	0	0	00h	3 gray scale Luminance Value (White)
133	85h	0	0	0	0	0	0	0	1	01h	4 gray scale Luminance Value (White)
134	86h	0	0	0	0	0	0	0	1	01h	5 gray scale Luminance Value (White)
135	87h	0	0	0	0	0	0	0	1	01h	6 gray scale Luminance Value (White)
136	88h	0	0	0	0	0	0	1	0	02h	7 gray scale Luminance Value (White) (V2 level)
137	89h	0	0	0	0	0	0	1	1	03h	8 gray scale Luminance Value (White)
138	8Ah	0	0	0	0	0	1	0	0	04h	9 gray scale Luminance Value (White)
139	8Bh	0	0	0	0	0	1	0	0	04h	10 gray scale Luminance Value (White)
140	8Ch	0	0	0	0	0	1	0	1	05h	11 gray scale Luminance Value (White)
141	8Dh	0	0	0	0	0	1	1	1	07h	12 gray scale Luminance Value (White)
142	8Eh	0	0	0	0	1	0	0	0	08h	13 gray scale Luminance Value (White)
143	8Fh	0	0	0	0	1	0	0	1	09h	14 gray scale Luminance Value (White)
144	90h	0	0	0	0	1	0	1	1	0Bh	15 gray scale Luminance Value (White) (V3 level)
145	91h	0	0	0	0	1	1	0	1	0Dh	16 gray scale Luminance Value (White)
146	92h	0	0	0	0	1	1	1	0	0Eh	17 gray scale Luminance Value (White)
147	93h	0	0	0	1	0	0	0	0	10h	18 gray scale Luminance Value (White)
148	94h	0	0	0	1	0	0	1	0	12h	19 gray scale Luminance Value (White)
149	95h	0	0	0	1	0	1	0	0	14h	20 gray scale Luminance Value (White)
150	96h	0	0	0	1	0	1	1	1	17h	21 gray scale Luminance Value (White)
151	97h	0	0	0	1	1	0	0	1	19h	22 gray scale Luminance Value (White)
152	98h	0	0	0	1	1	1	0	0	1Ch	23 gray scale Luminance Value (White) (V4 level)
153	99h	0	0	1	0	1	1	1	1	1Fh	24 gray scale Luminance Value (White)
154	9Ah	0	0	1	0	0	0	0	1	21h	25 gray scale Luminance Value (White)
155	9Bh	0	0	1	0	0	1	0	0	24h	26 gray scale Luminance Value (White)
156	9Ch	0	0	1	0	1	0	0	0	28h	27 gray scale Luminance Value (White)
157	9Dh	0	0	1	0	1	0	1	1	2Bh	28 gray scale Luminance Value (White)
158	9Eh	0	0	1	0	1	1	1	0	2Eh	29 gray scale Luminance Value (White)

※ Luminance values are theoretical value at the time of γ = 2.2 (C sample)

Address		EEPROM Data value (binary)								hex	Description of the register address
Deci	hex	E7	E6	E5	E4	E3	E2	E1	E0		
159	9Fh	0	0	1	1	0	0	1	0	32h	30 gray scale Luminance Value (White)
160	A0h	0	0	1	1	0	1	1	0	36h	31 gray scale Luminance Value (White) (V5 level)
161	A1h	0	0	1	1	1	0	0	1	39h	32 gray scale Luminance Value (White)
162	A2h	0	0	1	1	1	1	0	1	3Dh	33 gray scale Luminance Value (White)
163	A3h	0	1	0	0	0	0	1	0	42h	34 gray scale Luminance Value (White)
164	A4h	0	1	0	0	0	1	1	0	46h	35 gray scale Luminance Value (White)
165	A5h	0	1	0	0	1	0	1	0	4Ah	36 gray scale Luminance Value (White)
166	A6h	0	1	0	0	1	1	1	1	4Fh	37 gray scale Luminance Value (White)
167	A7h	0	1	0	1	0	1	0	0	54h	38 gray scale Luminance Value (White)
168	A8h	0	1	0	1	1	0	0	1	59h	39 gray scale Luminance Value (White) (V6 level)
169	A9h	0	1	0	1	1	1	1	0	5Eh	40 gray scale Luminance Value (White)
170	AAh	0	1	1	0	0	0	1	1	63h	41 gray scale Luminance Value (White)
171	ABh	0	1	1	0	1	0	0	1	69h	42 gray scale Luminance Value (White)
172	ACh	0	1	1	0	1	1	1	0	6Eh	43 gray scale Luminance Value (White)
173	ADh	0	1	1	1	0	1	0	0	74h	44 gray scale Luminance Value (White)
174	AEh	0	1	1	1	1	0	1	0	7Ah	45 gray scale Luminance Value (White)
175	AFh	1	0	0	0	0	0	0	0	80h	46 gray scale Luminance Value (White)
176	B0h	1	0	0	0	0	1	1	0	86h	47 gray scale Luminance Value (White) (V7 level)
177	B1h	1	0	0	0	1	1	0	0	8Ch	48 gray scale Luminance Value (White)
178	B2h	1	0	0	1	0	0	1	1	93h	49 gray scale Luminance Value (White)
179	B3h	1	0	0	1	1	0	0	1	99h	50 gray scale Luminance Value (White)
180	B4h	1	0	1	0	0	0	0	0	A0h	51 gray scale Luminance Value (White)
181	B5h	1	0	1	0	0	1	1	1	A7h	52 gray scale Luminance Value (White)
182	B6h	1	0	1	0	1	1	1	0	AEh	53 gray scale Luminance Value (White)
183	B7h	1	0	1	1	0	1	1	0	B6h	54 gray scale Luminance Value (White)
184	B8h	1	0	1	1	1	1	0	1	BDh	55 gray scale Luminance Value (White) (V8 level)
185	B9h	1	1	0	0	0	1	0	1	C5h	56 gray scale Luminance Value (White)
186	BAh	1	1	0	0	1	1	0	1	CDh	57 gray scale Luminance Value (White)
187	BBh	1	1	0	1	0	1	0	1	D5h	58 gray scale Luminance Value (White)
188	BCh	1	1	0	1	1	1	0	1	DDh	59 gray scale Luminance Value (White)
189	BDh	1	1	1	0	0	1	0	1	E5h	60 gray scale Luminance Value (White)
190	BEh	1	1	1	0	1	1	1	0	EEh	61 gray scale Luminance Value (White)
191	BFh	1	1	1	1	0	1	1	0	F6h	62 gray scale Luminance Value (White)
192	C0h	1	1	1	1	1	1	1	1	FFh	63 gray scale Luminance Value (White) (V10 level)
193	C1h	0	1	0	0	0	0	1	1	43h	Set of V10-AC High Voltage (Word Address) / Contrast
194	C2h	0	1	0	0	0	0	1	1	43h	V10-AC High Voltage (C-IC set Value) / Contrast
195	C3h	1	1	1	0	0	0	0	1	E1h	Set of V10-AC Low Voltage (Word Address) / Contrast
196	C4h	1	1	1	0	0	0	0	1	E1h	V10-AC Low Voltage (C-IC set Value) / Contrast
197	C5h	1	0	0	1	1	1	0	1	9Dh	Set of V3 -AC High Voltage (Word Address) / Neutral Scale
198	C6h	1	0	0	1	1	1	0	1	9Dh	V3-AC High Voltage (C-IC set Value) / Neutral Scale
199	C7h	0	1	1	0	0	1	1	1	67h	Set of V3 -AC Low Voltage (Word Address) / Neutral Scale
200	C8h	0	1	1	0	0	1	1	1	67h	V3-AC Low Voltage (C-IC set Value) / Neutral Scale
201	C9h	0	0	0	0	1	1	1	0	0Eh	COM Adjustment High (Word Address) / Brightness
202	CAh	0	0	0	0	1	1	1	0	0Eh	COM Adjustment High Voltage (C-IC set Value) / Brightness
203	CBh	1	1	1	1	0	0	1	0	F2h	COM Adjustment Low (Word Address) / Brightness
204	CCh	1	1	1	1	0	0	1	0	F2h	COM Adjustment Low Voltage (C-IC set Value) / Brightness
205	CDh	0	0	0	0	0	0	0	0	00h	Red data offset (word address)
206	CEh	0	0	0	0	0	0	0	0	00h	Red color shift value (C-IC set Value)
207	CFh	0	0	0	0	0	0	0	0	00h	Green data offset (word address)
208	D0h	0	0	0	0	0	0	0	0	00h	Green color shift value (C-IC set Value)
209	D1h	0	0	0	0	0	0	0	0	00h	Blue data offset (word address)
210	D2h	0	0	0	0	0	0	0	0	00h	Blue color shift value (C-IC set Value)
211	D3h	1	1	1	1	1	1	1	1	FFh	Horizontal Indication Start Point (word address)
212	D4h	1	1	1	1	1	1	1	1	FFh	Horizontal Shift value (C-IC set Value)

※ Luminance values are theoretical value at the time of γ = 2.2 (C sample)

Address		EEPROM Data value (binary)								hex	Description of the register address
Deci	hex	E7	E6	E5	E4	E3	E2	E1	E0		
213	D5h	0	0	1	0	0	0	1	1	23h	Vertical Indication Start Point (word address)
214	D6h	0	0	1	0	0	0	1	1	23h	Vertical Shift value (C-IC set Value)
215	D7h	0	0	0	0	0	0	0	0	00h	Scan Direction switching (word address)
216	D8h	0	0	0	0	0	0	0	0	00h	Scan Direction data (C-IC set Value)
217	D9h	0	0	0	0	0	0	0	0	00h	Sharp Internal Check up registers for Mass Production
218	DAh	1	1	1	1	1	1	1	1	FFh	Sharp Internal Check up registers for Mass Production
219	DBh	0	0	0	0	0	0	0	0	00h	Sharp Internal Check up registers for Mass Production
220	DCh	1	1	1	1	1	1	1	1	FFh	Sharp Internal Check up registers for Mass Production
221	DDh	0	0	0	0	0	0	0	0	00h	Test Picture (word address)
222	DEh	0	0	0	0	0	0	0	0	00h	Test Picture Enable+Select Value/Picture(C-IC set Value)
223	DRh	1	1	1	1	1	1	1	1	FFh	Input signal error judgement (read only)
224	E0h	-	-	-	-	-	-	-	-	--h	COMDC adjustment (C-IC set Value)
225	E1h	0	1	1	0	0	1	1	0	66h	Min Pixel Clock/10000 (Low Byte)
226	E2h	0	0	0	0	1	0	1	0	0Ah	(High Byte) [26.62MHz→2662→0A66h]
227	E3h	1	1	1	0	0	0	0	0	E0h	Min. Horizontal Blanking (Low Byte) [224pixel=0E0h]
228	E4h	0	0	1	0	1	1	1	1	28h	Min. Vertical Blanking (Low Byte) [40Lines=028h]
229	E5h	0	0	0	0	0	0	0	0	00h	Min. Horizontal /Vertical Blanking (upper nibble)
230	E6h	1	0	1	1	1	1	0	0	BCh	Min. Horizontal Sync. Offset (Low Byte) [188pixel=0BCh]
231	E7h	0	0	0	0	0	1	0	1	05h	Min. Horizintal Sync Pulse width (Low Byte) [5pixel=005h]
232	E8h	1	0	1	0	0	0	1	0	A2h	Min. Vertical Sync Offset/Puls Width (lower nibble)
233	E9h	0	0	0	0	0	0	0	0	00h	Min. Horizontal Sync Offset (<7,6> upper 2 bits) Min. Horizontal Sync Punls Width (<5,4> upper 2 bits) Min. Vertical Sync Offset (<3,2> upper 2 bits) Min. Vertical Sync Pulse Width (<1,0> upper 2 bits)
234	EAh	1	0	0	0	0	1	0	0	84h	Max. Pixel clock / 10000 (Low Byte) [34.60MHz→0D84h]
235	EBh	0	0	0	0	1	1	0	1	0Dh	(High Byte)
236	ECh	0	0	1	0	0	0	0	0	20h	Max. Horizontal Blanking (Low Byte) [288pixel=120h]
237	EDh	1	0	0	1	0	1	1	0	96h	Max. Vertical Blanking (Low Byte) [155Lines=096h]
238	EEh	0	0	0	1	0	0	0	0	10h	Max. Horizontal / Vertical Blanking (upper nibble)
239	EFh	1	1	1	1	0	1	0	0	F4h	Max. Horizontal Sync Offset (Low Byte) [244pixel=0F4]
240	F0h	1	1	0	0	1	0	0	0	C8h	Max. Horizontal Sync pulse Width(Low Byte) [200pixel=0C8h]
241	F1h	0	0	1	1	0	0	0	0	30h	Max. Vertical Sync Offset 35Line /pulse width 48Line (lower nibble) [ex. 35Line=' 100011' , 48Line=' 110000']
242	F2h	0	0	0	0	1	0	1	1	0Bh	Max. Horizontal Sync Offset (<7,6> upper 2 bits) Max. Horizontal Sync Puls Width (<5,4> upper 2 bits) Max. Vertical Sync Offset (<3,2> upper 2 bits) Max. Vertical Sync Pulse Width (<1,0> upper 2 bits)
243	F3h	1	0	1	0	1	1	1	0	AEh	Horizontal Image Size (Low Byte) [174mm→0AEh]
244	F4h	0	1	1	0	1	0	0	0	68h	Vertical Image Size (Low Byte) [104mm→068h]
245	F5h	0	0	0	0	0	0	0	0	00h	Horizontal Image Size (upper nibble)
246	F6h	0	0	1	0	0	0	0	0	20h	Horizontal Active pixel (Low Byte) [800pixel=320h]
247	F7h	1	1	1	0	0	0	0	0	E0h	Vertical Active pixel (Low Byte) [480pixel=1E0h]
248	F8h	0	0	1	1	0	0	0	1	31h	Horizontal /Vertical Active pixel (upper nibble)
249	F9h	0	0	0	0	0	0	0	0	00h	Horizontal Border period [0pixcel=00h]
250	FAh	0	0	0	0	0	0	0	0	00h	Vertical Border period [0pixcel=00h]
251	FBh	0	0	0	0	0	0	0	0	00h	Flags /Sync polarities Function : non interface<7> : 0 , <6, 5> : 0, 0 Reference<4, 3, 2, 1> : 0, 0, 0, 0 , <0> : 0
252	FCh	0	0	0	0	0	0	0	0	00h	Not used therefore filled with 00h
253	FDh	0	0	0	0	0	0	0	0	00h	Not used therefore filled with 00h
254	FEh	0	0	0	0	0	0	0	0	00h	Not used therefore filled with 00h
255	FFh	-	-	-	-	-	-	-	-	--h	Checksum (Sum of all 256 bytes = 00h)

7-7-3 Others

EEPROM write operation mode
・Byte write (BYTE WRITE)
・Page write (PAGE WRITE)
EEPROM read out operation mode
・Current address read (CURRENT ADDRESS READ)
・Random address read (RANDOM ADDRESS READ)
・Sequential current read (SEQUENTIAL CURRENT READ)
・Sequential random read (SEQUENTIAL RANDOM READ)

When write to EEPROM, set the slave address to 1010000.

The address number about a display setup of your company is E0h from C1h.

8. Absolute maximum ratings

Table 8-1 GND=0V

Parameter	Symbol	MIN	MAX	Unit	Note
Input voltage	V_I	-0.3	Vcc+0.3	V	[Note 8-1]
+3.3V power supply	Vcc	-0.3	+4.6	V	
Storage temperature	Tstg	-40	85	℃	[Note 8-2,3]
Operating temperature (panel surface)	Topr1	-30	85	℃	[Note 8-2,3,4]
Operating temperature (Ambient temperature)	Topr2	-30	60	℃	[Note 8-5]

[Note 8-1] DCLK,R0～R5,G0～G5,B0～B5,Hsync,Vsync,DataEn,HVR,SCS,SCK,SDI ,RST

[Note 8-2] This rating applies to all parts of the module and should not be exceeded.

The specified temperature provides the maximum value within 5mm around the module.

[Note 8-3] Maximum wet-bulb temperature is to be less than 58℃. Condensation of dew must be avoided as electrical current leaks will occur, causing a degradation of performance specifications.

[Note 8-4] The operating temperature only guarantees operation of the circuit. For contrast, speed response, and other factors related to display quality, determine operating temperature using the formula Ta=+25℃

[Note 8-5] Ambient temperature when the backlight is lit (reference value).

9. Electrical characteristics

9-1 TFT-LCD panel driving section

Table 9-1 Ta= 25℃

Parameter		Symbol	MIN	TYP	MAX	Unit	Remarks
+3.3V	Supply voltage	Vcc	+3.0	+3.3	+3.6	V	[Note 9-1]
	Current dissipation	Icc	–	450	500	mA	[Note 9-2]
Permissive input ripple		V_{RF}	–	–	200	mVpp	
Input Low voltage		V_{IL}	−0.3	–	0.3Vcc	V	
Input High voltage		V_{IH}	0.7Vcc	–	3.6	V	[Note 9-3]
Low level Input current 1		I_{IL1}	–	–	1.0	μA	V_I=0V or V_{CC}
High level Input current 1		I_{IH1}	–	–	1.0		[Note 9-4]
Low level Input current 2		I_{IL2}	–	–	3.0	μA	V_I=0V or V_{CC}
High level Input current 2		I_{IH2}	–	220	365		[Note 9-5]
Low level Input current 3		I_{IL3}	–	220	365	μA	V_I=0V or V_{CC}
High level Input current 3		I_{IH3}	–	–	3.0		[Note 9-6]
Low level Input current 4		I_{IL4}	–	440	730	μA	V_I=0V or V_{CC}
High level Input current 4		I_{IH4}	–	–	6.0		[Note 9-7]
Low level Input current 5		I_{IL5}	–	1.72	2.20	mA	V_I=0V or V_{CC}
High level Input current 5		I_{IH5}	–	–	0.2		[Note 9-8]

[Note 9-1]

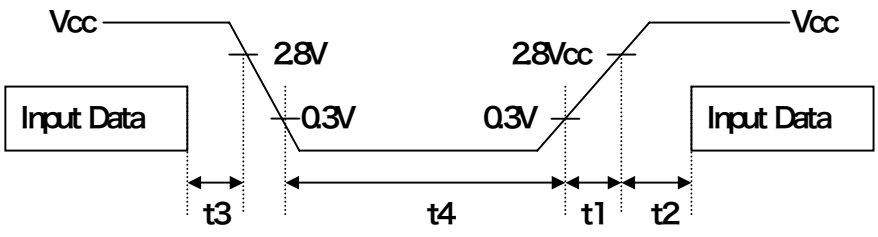
Vcc-turn-on and turn-off conditions

1<t1≦5ms

0≦t2≦5ms

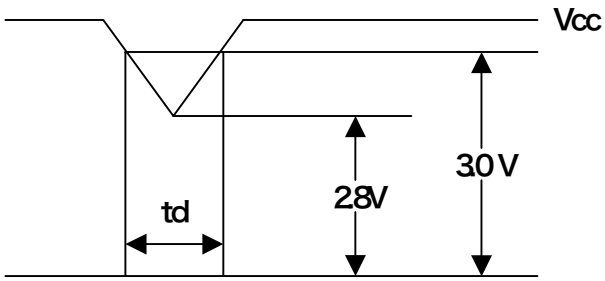
0<t3≦5ms

t4>1s



Vcc-dip conditions

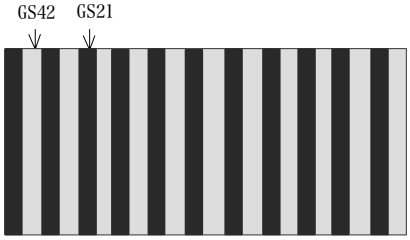
1) In case 2.8V≦Vcc≦3.0,td≦10ms
2) In case Vcc＜2.8V, Vcc-dip conditions should also follow the Vcc-turn-on and turn-off conditions



[Note 9-2]

Timing: Typical
Vcc : 3.3V
Set up serial data : Value in resetting
Situation: Typical current ; Black (V0) pattern
Maximum current ; Vertical stripe pattern alternating by 21 gray scale (GS21) with 42 gray scale (GS42) every 1 dot.

Typical current situation



Max current situation

[Caution] The stated data is current dissipation when the supply voltage is stabilized and is not momentary current dissipation when the supply voltage is turned-on.

[Note 9-3] DCLK,R0～R5,G0～G5,B0～B5,Hsync,DataEn,Vsync,SCK,SDI,HVR,RST

[Note 9-4] DCLK,R0～R5,G0～G5,B0～B5,

[Note 9-5] DataEn

[Note 9-6] Hsync,Vsync, RST

[Note 9-7] HVR

[Note 9-8] SCK,SDI,WC,SCS

9-2 Backlight driving section

The backlight system is an edge-lighting type with one CCFT (Cold Cathode Fluorescent Tube). The characteristics of Lamp are shown in the following table.

Table 9-2

Parameter	Symbol	MIN	TYP.	MAX	Unit	Remarks
lamp voltage	VL7	420	470	520	Vrms	L=(5.0)mArms
lamp current	L	4.5	5.0	5.5	mArms	In case normal [Per piece]
Discharge pipe electric power	WL	–	4.7	–	W	When the fixed case lights up
lamp frequency	fL	45	–	70	kHz	
kick-off voltage	VS	–	–	1750	Vrms	Ta=+25℃
		–	–	1800	Vrms	Ta=-30℃

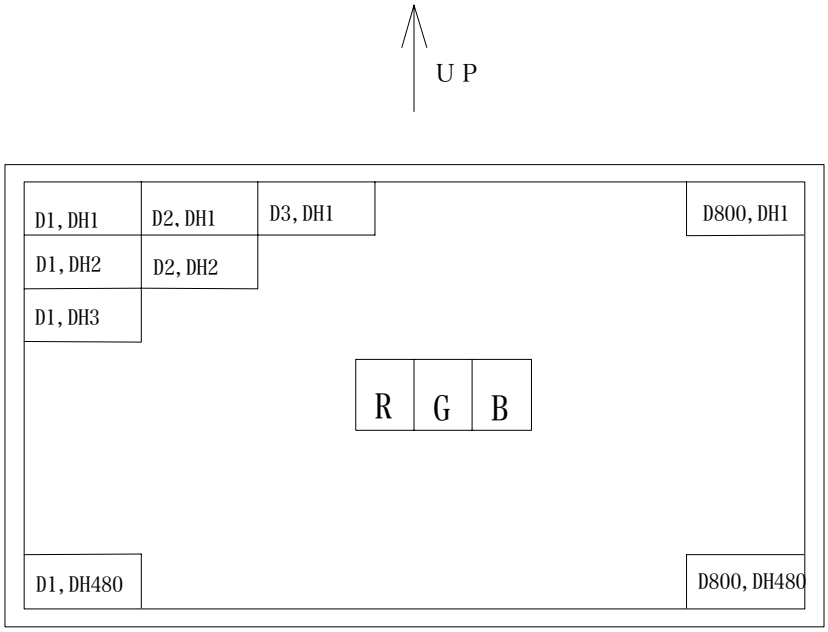
Inverter (HIU359A-S2[18pF] 50kHz)

[Caution]

Use the inverter which has the characteristics of the sine wave. With regards to the inverter, it should be negative/positive wave symmetry and the spike wave should not be occurred.

9-3 Input Data Signals and Display Position on the screen

Refer to the following figure



Display position of input data (H,V)

10. Input Signals, Basic Display Color and Gray Scale of Each Color

Table 10-1

	Colors & Gray scale	Gray Scale	Data signal R0	R1	R2	R3	R4	R5	0 :Low level voltage G0	G1	G2	G3	G4	G5	1 :High level voltage B0	B1	B2	B3	B4	B5
Basic color	Black	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	–	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	–	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	–	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	–	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	–	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	–	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	GS62	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS63	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
	⇩	GS62	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	GS63	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale of bleu	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
	⇩	GS62	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Bleu	GS63	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Each basic color can be displayed in 64 gray scales by 6 bit data signals. According to the combination of total 18 bit data signals, the 262,144-color display can be achieved on the screen.

11. Optical characteristics

・ Table 11-1 Ta=25℃, Vcc=+3.3V

Parameter		Symbol	Condition	Min	Typ.	Max	Unit	Remarks
Viewing angle range		θ21, θ22	CR=>5	60	65	—	° (degree)	[Note11-1,4]
		θ11		50	55	—	° (degree)	
		θ12		60	65	—	° (degree)	
Contrast ratio		CRmax	Optimal	100	—	—		[Note11-2]
Response time	Rise	τr	θ=0°	—	30	60	ms	[Note11-3]
	Fall	τd		—	50	100	ms	
White chromaticity		x	IL=5.0mArms θ=0°	0.263	0.313	0.363		[Note11-4]
		y		0.279	0.329	0.379		
Luminance		Y		500	625	—	cd/m^2	
Lamp lifetime	+25℃	—	continuation	10,000	—	—	hour	[Note11-5]
	-30℃	—	intermittent	2,000	—	—	time	[Note11-6]
Diffuse Reflectance		R		—	2.5	3.5	%	

DC/AC inverter for external connection is shown in the following figures.
Inverter：(HIU359A-S2(18pF))

※ Measure after 30 minutes of power on. The optical measurement of the characteristic is to be done in the condition which is equal to the darkroom or use the way of measuring described in the following figure 6 and figure 7.

Condition: Reflectance → Shimadzu Corporation.(Model:UV-3100PC) : C-light source
Hazes value →Nippon Denshoku Industries Co. Ltd. (Model:NDH2000)
(Haze value of the polarization plate of this module is 10% (typ).)

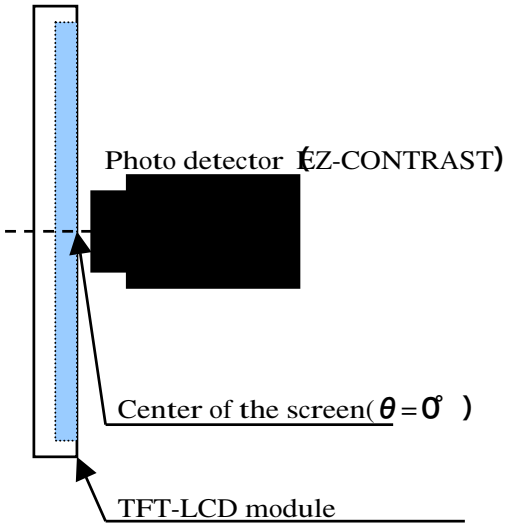


Fig. 6 The way of measuring
Viewing angle range/ Contrast/ Response time

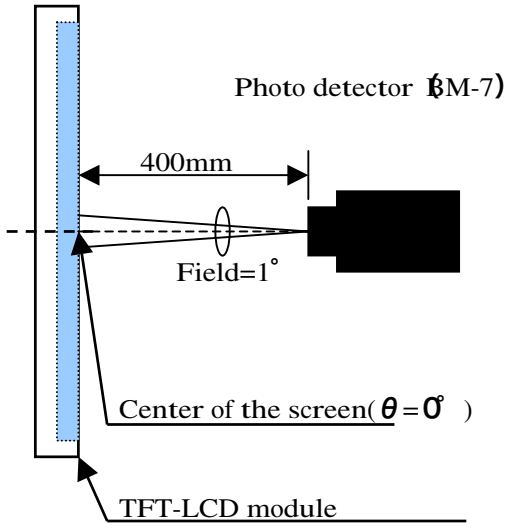
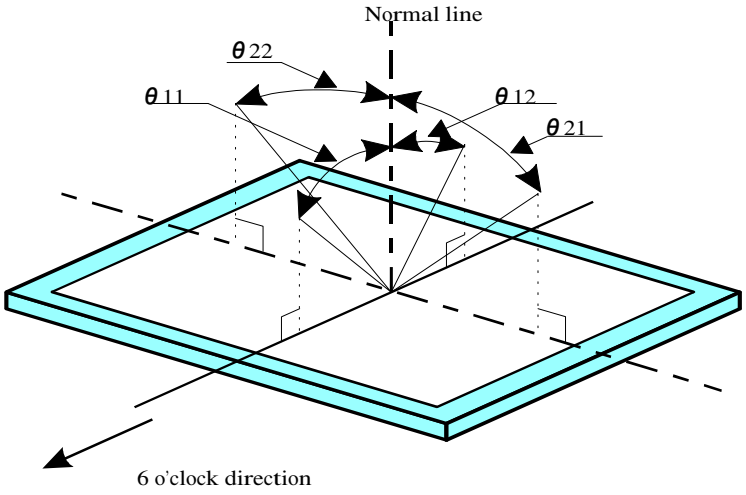


Fig. 7 The way of measuring
Luminance/ Chromaticity

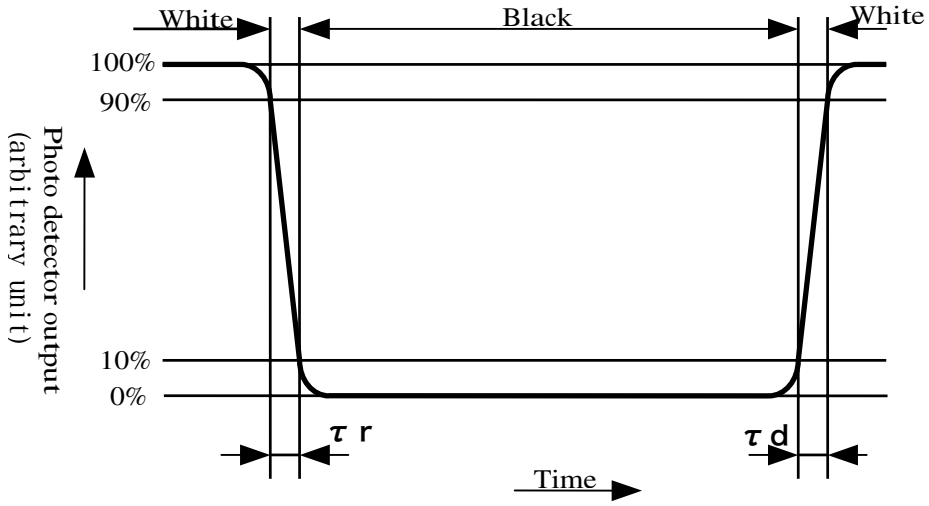
[Note 11-1] Viewing angle range is defined as follows.



[Note 11-2] Contrast ratio of transmission is defined as follows:

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output with LCD being "white"}}{\text{Photo detector output with LCD being "black"}}$$

[Note 11-3] Response time is obtained by measuring the transition time of photo detector output, when input signals are applied so as to make the area "black" to and from "white".

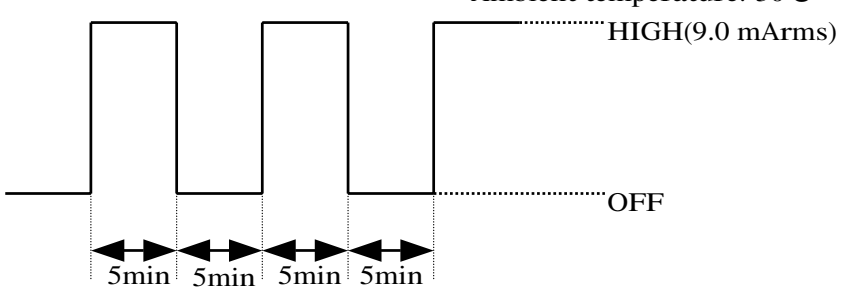


[Note 11-4] Measured on the center area of the panel (After 30 minutes operation)
DC/AC inverter driving frequency: 50 kHz

[Note 11-5] Lamp life time is defined as the time when the brightness of the panel is not become less than 50% of the original value in the continuous operation under the condition of lamp current IL= 5.0 mArms and PWM dimming 100%~5% (Ta=25℃).

[Note 11-6] The intermittent cycles is defined as a time when brightness is not become under 50% of the original value under the condition of following cycle.

Ambient temperature:-30℃



12. Display quality

The display quality of the color TFT-LCD module shall be in compliance with the Incoming Inspection Standards for TFT-LCD.

13. Handling instructions

13-1 Mounting of module

The TFT-LCD module is designed to be mounted on equipment using the mounting tabs in the four corners of the module at the rear side.

On mounting the module, as the 2.5 tapping screw fastening torque is (0.40) through (0.60)N•m is recommended, be sure to fix the module on the same plane, taking care not to wrap or twist the module.

Don't reach the pressure of touch-switches of the set side to a module directly, because images may be disturbed.

Power off the module when you connect the input/output connector.

Connect the metallic shielding cases of the module and the ground pattern of the inverter circuit firmly. If that connection is not perfect, there may be a possibility that the following problems happen.

a) The noise from the backlight unit will increase.

b) The output from inverter circuit will be unstable. Then, there is a possibility that some problems may happen.

c) In some cases, a part of module will heat up.

d) Don't pull a CCFT lead line with the force beyond 10N. It has the possibility of the breakage in the lamp, the connection part of the lead line, and so on.

13-2 Precautions in mounting

Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

Protection sheet is applied on the surface to protect it against scratches and dirties.

It is recommended to remove the protection sheet immediately before the use, taking care of static electricity.

Precautions in removing the protection sheet

A) Working environment

When the protection sheet is removed off, static electricity may cause dust to stick to the polarizer surface.

To avoid this, the following working environment is desirable.

a) Floor: Conductive treatment of 1MΩ or more on the tile
(conductive mat or conductive paint on the tile)

b) Clean room free form dust and with an adhesive mat on the doorway

c) Advisable humidity:50%～70% Advisable temperature:15℃～27℃

d) Workers shall wear conductive shoes, conductive work clothes, conductive gloves and an earth band.

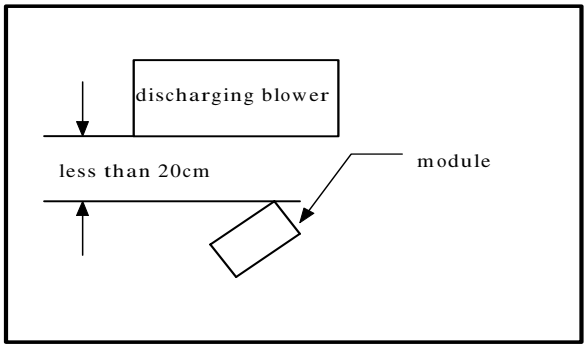
B) Working procedures

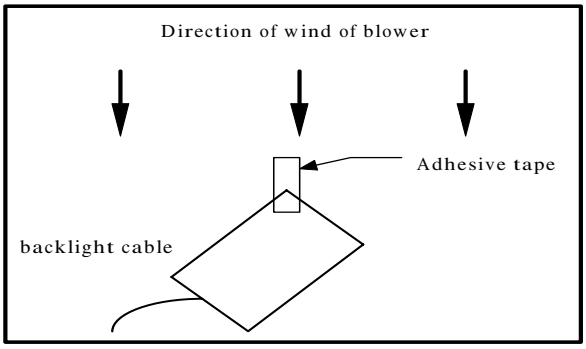
a) Direct the wind of discharging blower somewhat downward to ensure that module is blown sufficiently. Keep the distance between module and discharging blower within 20 cm.

b) Attach adhesive tape to the protection sheet part near discharging blower so as to protect polarizer against flaw.

c) Remove the protection sheet, pulling adhesive tape slowly to your side.

d) On removing the protection sheet, pass the module to the next work process to prevent the module to get dust.





e) Method of removing dust from polarizer

- Blow off dust with N2 blower for which static electricity preventive measure has been taken.
- Since polarizer is vulnerable, wiping should be avoided. But when the panel has stain or grease, to use adhesive tape is recommended to remove them softly from the panel.

When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth. For stubborn dirties, wipe the part, breathing on it. Wipe off water drop or finger grease immediately. Long contact with water may cause discoloration or spots. TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Handle with care. Since CMOS LSI is used in this module, take care of static electricity and earth your body when handling.

13-3 Caution of product design

The LCD module shall be protected against water or salt-water by the waterproof cover. Take measures against the interferential radiation from module, not to interfere surrounding appliances.
Because driving voltage for backlight is high, it is dangerous to use LCD module under the conditions which are deviated from specification.
The equipment for which the LCD module is used shall have fail-safe design so that the safety can be ensured in case abnormality of inverter circuit, etc. should occur.

13-4 Others

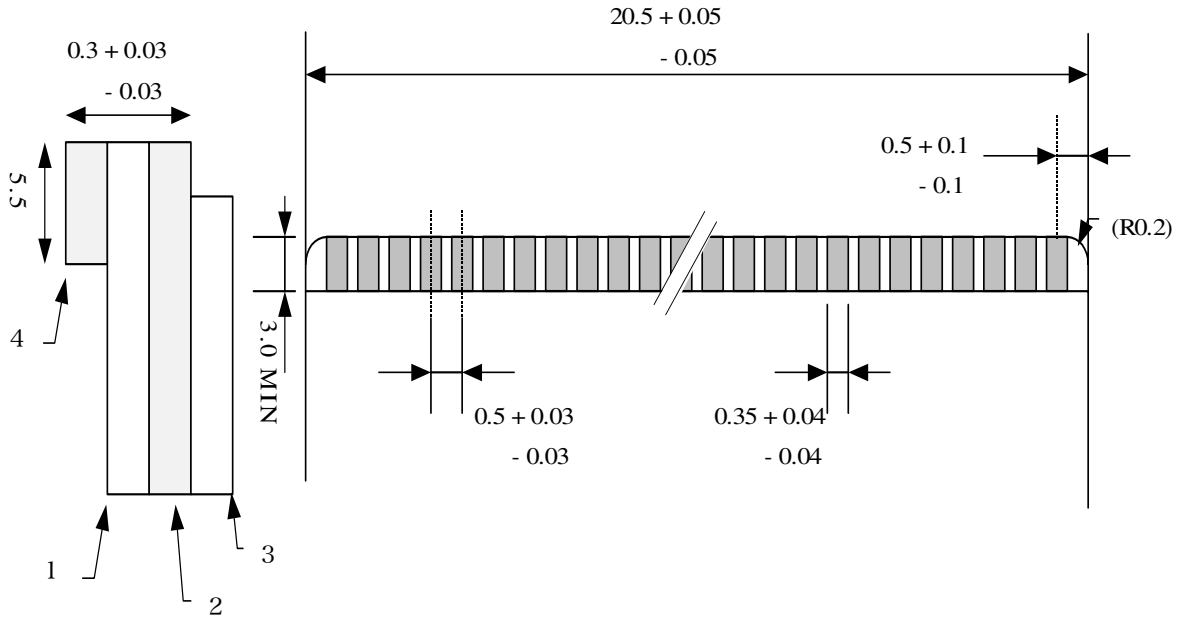
Do not expose the module to direct sunlight or intensive ultraviolet rays for several hours or more; liquid crystal is deteriorated by ultraviolet rays. Store the module at a temperature near the room temperature. If lower than the rated storage temperature, liquid crystal solidifies, causing the panel to be damaged. If higher than the rated storage temperature, liquid crystal turns into isotropic liquid and may not recover. If LCD panel breaks, there may be a possibility that the liquid crystal leaks out from the panel. Since the liquid crystal is injurious, do not put it into the eyes or mouth. When liquid crystal sticks to hands, feet or clothes, wash it out immediately with soap. Observe all other precautionary requirements in handling general electronic components.

14. Packing form

a)Piling number of cartons : 6 layers max
b)Package quantity in one carton 10 pcs
c)Carton size: 319(W)×484(H)×319(D) mm
d)Total mass of one carton filled with full modules: 6.0 kg
e)Conditions for storage.
Environment
①Temperature : 0～40℃
②Humidity : 60%RH or less at 40℃
No dew condensation at low temperature and high humidity.
③Atmosphere :Harmful gas, such as acid or alkali which corrodes electronic components and/or wires, must not be detected.
④Period : about 3 months
⑤Opening of the package : In order to prevent the LCD module from breakdown by electrostatic charges, please control the room humidity over 50%RH and open the package taking sufficient countermeasures against electrostatic charges, such as earth, etc.

15.Others

a) Disassembling the module may cause permanent damage and should be strictly avoided.
b) Be careful since image retention may occur when a fixed pattern is displayed for a long time.
c) Input/Output connector for TFT-LCD panel driving part
1) Fit FPC : Refer to the following figure
2) Keeping power of terminal : 0.9N/pin or more
[Every terminal is pulled out 25±3 mm/minute]
3) Endurance of insert/ pull out : Less than double of the initial resistance value
[The electrical resistance value of the contact changed by the repeated insertion / pulling out by 20 times to and from the matching FPC]

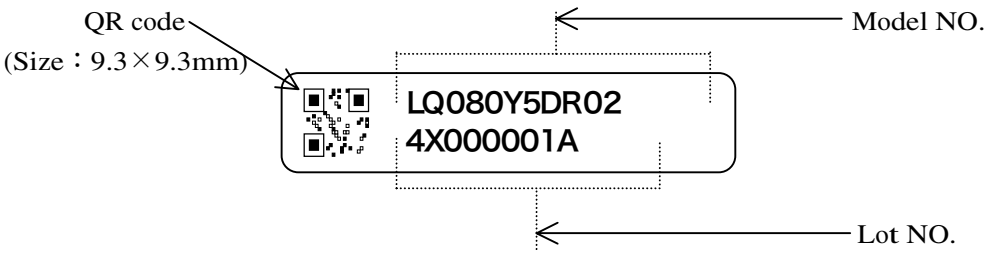


No.	Parameter	Material
1	Base material	Polyimide or the equivalent [25um thickness]
2	Copper leaf	Copper leaf [35um thickness] solder leaf [2um or less thickness]
3	Coverlay	Polyimide or the equivalent
4	Reinforced sheet	Polyester/ polyimide or the equivalent [188um thickness]

Fit FPC for Input/ Output connecter: 0.5mm pitch

16.Indication of lot number

①Attached location of the label : See Fig.8 (Outline Dimensions).
②Indicated contents of the label



contents of lot No. the 1st figure ･･ production year (ex. 2004 : 9)
the 2nd figure ･･ production month 1,2,3,･･････,9,X,Y,Z
the 3rd～7th figure ･･ serial No. 00001～
the 8th figure ･･ revision marks A,B,C･･

※ This label is used for a technical sample. A label changes from the time of mass production.

17. Reliability Test Conditions for TFT-LCD Module

Table 17-1

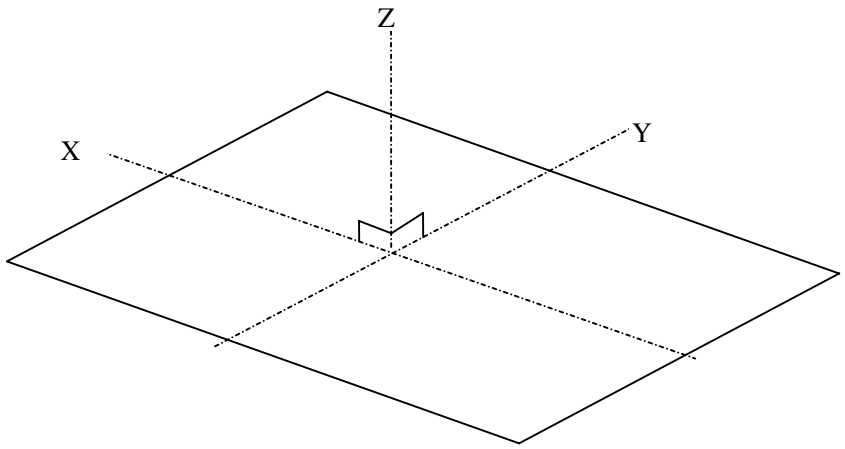
Remark) Temperature condition is based on operating temperature conditions on 9.Table 9-1.

No.	Test items	Test conditions
1	High temperature storage test	Ta= +85℃ 240h turn off LCD(No operation)
2	Low temperature storage test	Ta= -40℃ 240h turn off LCD (No operation)
3	High temperature and high humidity operating test	Tp=+60℃ 90%RH 240h Turn off B/L. Turn on LCD(Displayed Black image)
4	High temperature operating test	Tp= +85℃ 240h Turn on B/L. Turn on LCD at 85℃with panel surface
5	Low temperature operating test	Ta= -30℃ 240h Turn off B/L. Turn on LCD at -30℃with ambient temperature (Displayed Black image)
6	Electro static discharge test	±200V •200pF(0Ω) 1 time for each terminals
7	Shock test	980m/s² •6ms, ±X ;±Y ;±Z 3 times for each direction (JIS C0041, A-7 Condition C)
8	Vibration test	Frequency :8～33.3Hz, Stroke :1.3mm Frequency :33.3Hz～400Hz, Acceleration :28.4m/s² Sweep cycle :15 minutes X,Z 2 hours for each directions, 4 hours for Y direction (total 8 hours) (JIS D1601)
9	Heat shock test	Ta= -40℃ ～ +85℃ / 200 cycles (0.5h) (0.5h) Turn off B/L.

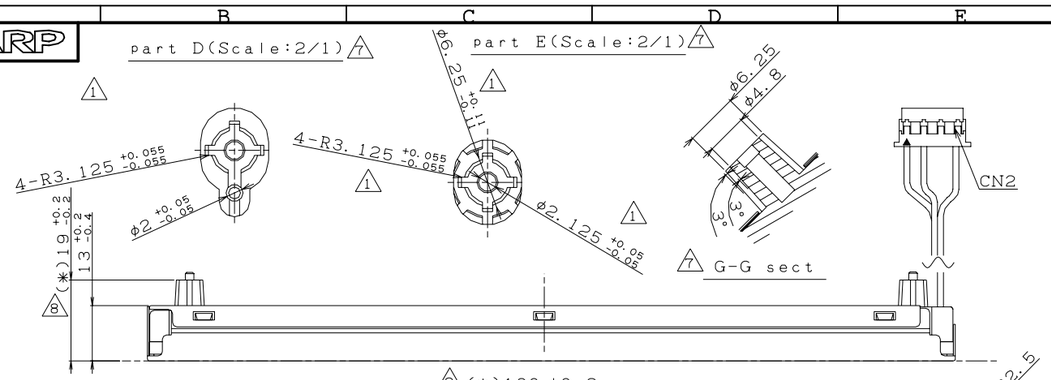
[Note] Ta= Ambient temperature, Tp= Panel temperature

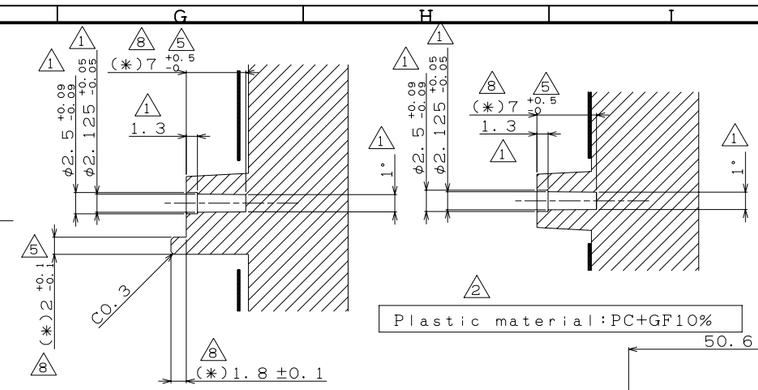
[Check items] In the standard condition, there shall be no practical problems that may affect the display function.

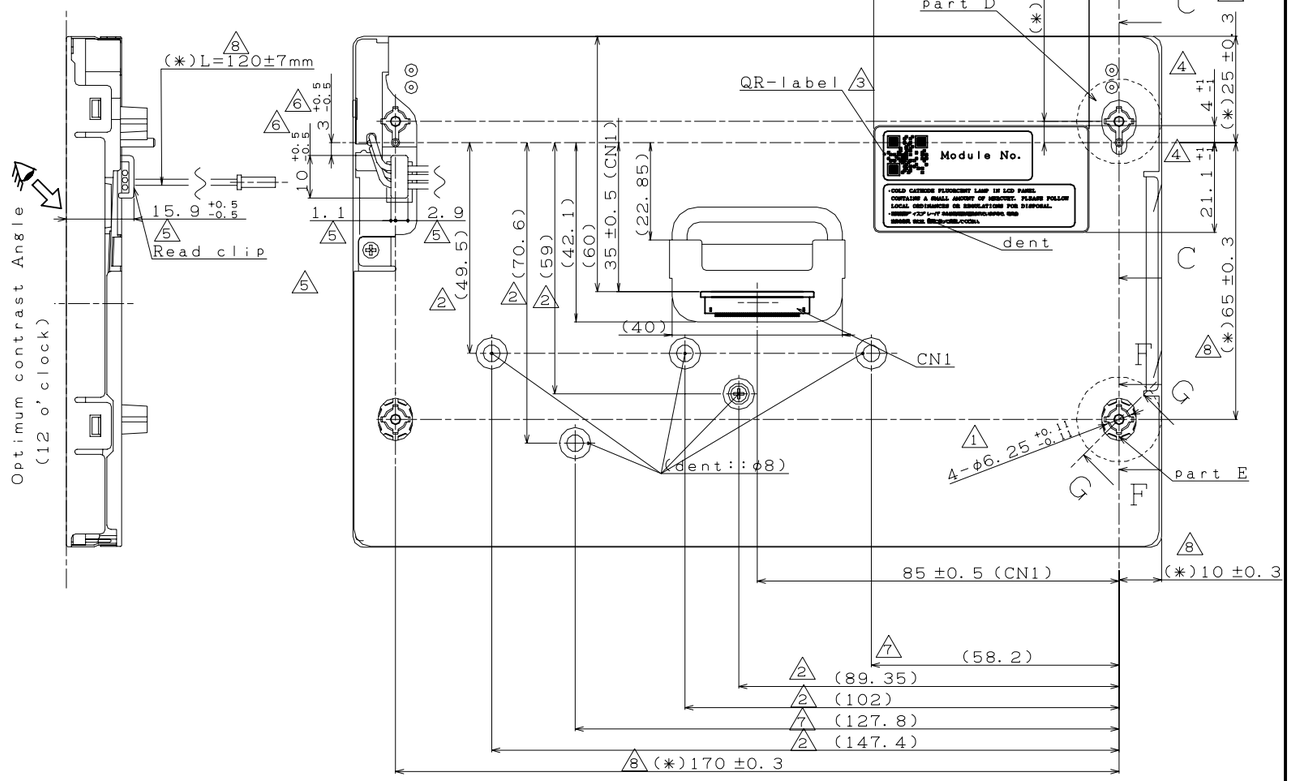
X,Y,Z directions are shown as follows:

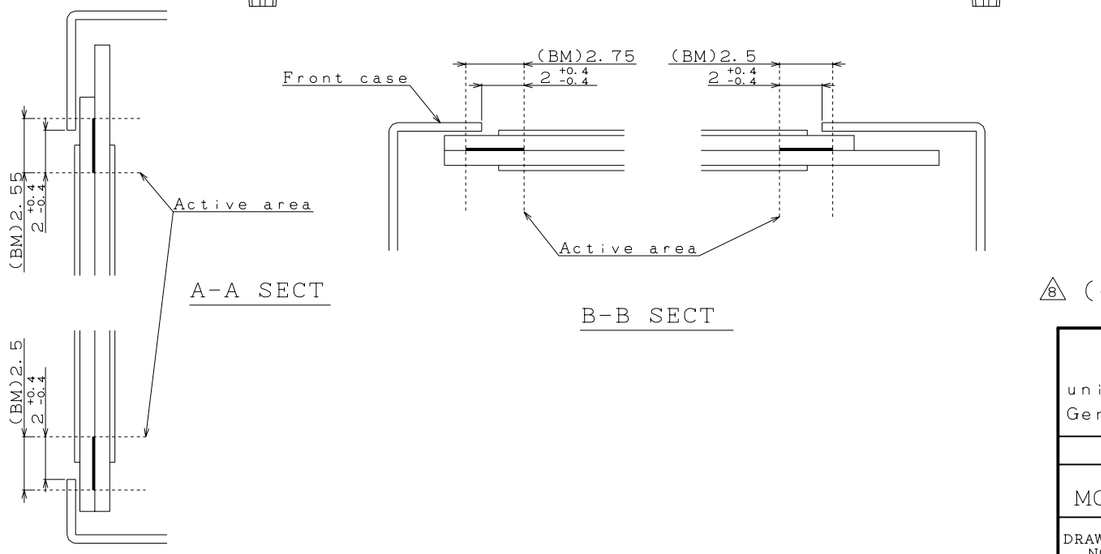


SHARP









CN1:I/O connector is 40FLZ-RSM1-R-TB(JST)
CN2:CCFT connector is BHR-04(4.0)VS-1(JST).

Take care in set design to hide the scratches and bubbles appeared on the polarizer or other frame area which is located outside of active area.

Since this module is under development, all the specified value is tentative. The technical literature is subject to change without notice.

(*) point for PPAP value.

unit:mm
General tolerance is ±0.3

DATE	2003.11.21
MODEL	LQ080Y5DR02
DRAWING NO	LCM-03107H
size	A3
SCALE	1/1

Please do not copy this material and do not disclose this to third party.

No.	DATE	REVISION	Sign.
8	04.06.07	(*)point for PPAP value. CCFT cable is change.	H.okuno
7	04.04.01	Dent area dimensions are change. Screw dome is change.	H.okuno
6	04.03.03	Read-clip is modification.	H.okuno
5	04.02.26	Tolerance is change. Outline dimensions are postscript. Read-clip added.	H.okuno
4	04.01.23	Dent area dimensions are postscript.	H.okuno

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MOBILE LCD DESIGN CENTER
ENGINEERING DEPT. II

Fig. 8 OUTLINE DIMENSIONS

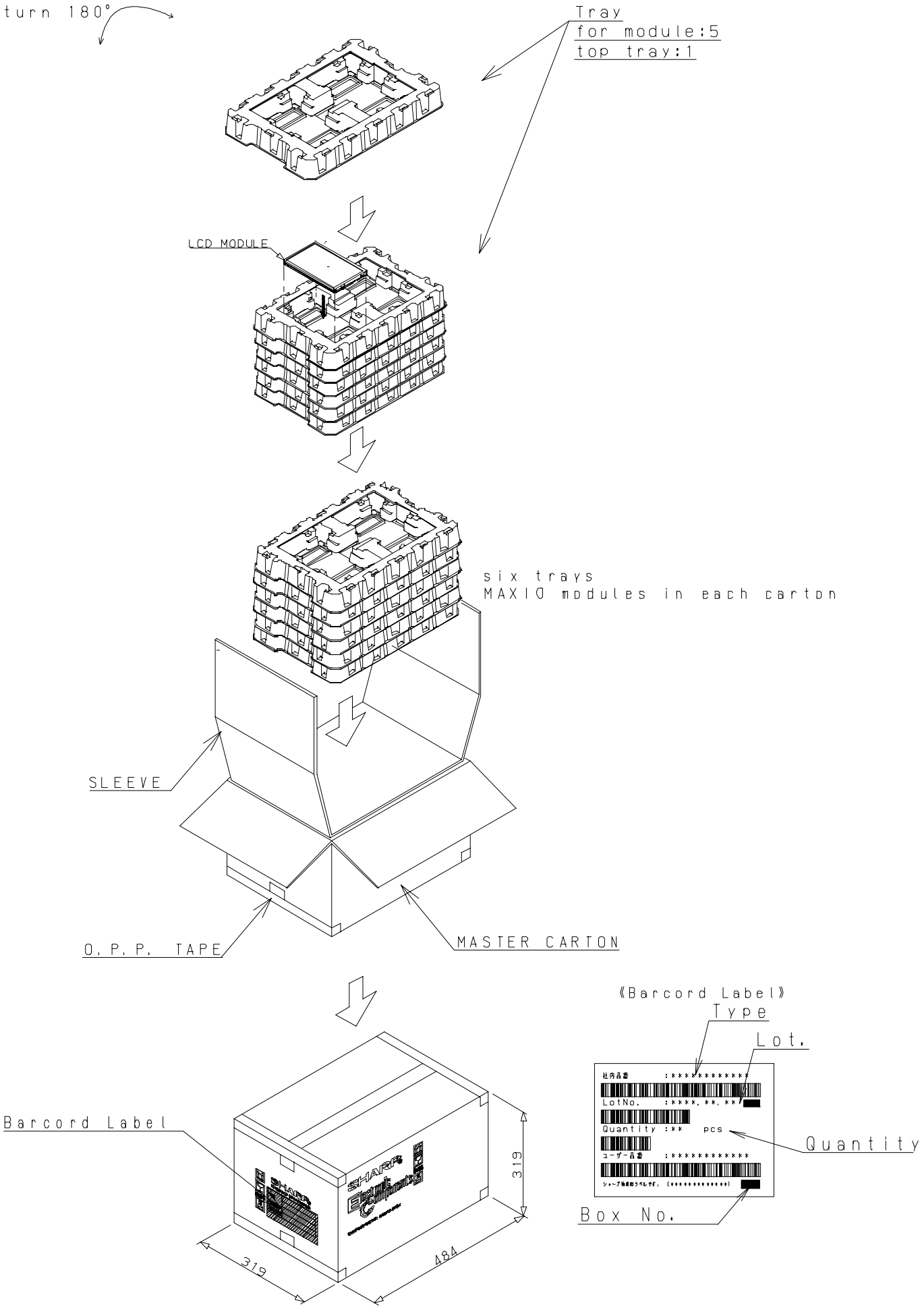

Fig. 9 Packing Form