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		APPLICABLE DIVISION MOBILE LCD CHINA DESIGN CENTER WUXI SHARP

SPECIFICATION

DEVICE SPECIFICATION for
TFT LCD Module
(320 × RGB × 240 dots)

Model No.

LQ035Q1DG04

☐CUSTOMER'S APPROVAL

DATE

BY

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1. Applicable Scope

This specification is applicable to TFT-LCD Module “LQ035Q1DG04”.
This LCD module is developed for PND (Personal Navigation Devices), not designed for Automotive build-in uses.

2. General Description

This module is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver IC, Input FPC, a back light unit and a touch panel. Graphics and texts can be displayed on a 320 × RGB × 240 dots panel with about 262k colors by supplying 18bit data signals (6bit × RGB), four timing signals, 3wires 24bit serial interface signals, logic (Typ. +3.3V), analog (Typ. +3.3V) supply voltages for TFT-LCD panel driving and supply voltage for back light.

3. Mechanical (Physical) Specifications

Item	Specifications	Unit
Screen size	3.47” QVGA	inch
Active area	70.56 (H) × 52.92 (V)	mm
Pixel format	320 (H) × 240 (V)	pixel
	1 Pixel = R+G+B dots	-
Pixel pitch	0.2205 (H) × 0.2205 (V)	mm
Pixel configuration	R,G,B vertical stripes	-
Display mode	Normally white	-
Unit outline dimensions *	76.9 (W) × 63.9 (H) × 4.25 (D)	mm
Mass	Approx. 41	g
Surface hardness	2H	-
Surface treatment	Anti glare	-

*The above-mentioned table indicates module sizes without some projections and FPC.
For detailed measurements and tolerances, please refer to 18. Outline Dimensions.

4. Input Terminal Names and Functions

Recommendation CN：[Entery] 6702-E50N-00R

Pin No.	Symbol	Description	Note
1	GND	GND(0V)	
2	GND	GND(0V)	
3	VDDIO	+3.3V power source	
4	VCI	+3.3V power source	
5	R0	NC	NC for 6bit mode
6	R1	NC	
7	R2	RED data signal(LSB)	
8	R3	RED data signal	
9	R4	RED data signal	
10	R5	RED data signal	
11	R6	RED data signal	
12	R7	RED data signal(MSB)	
13	G0	NC	NC for 6bit mode
14	G1	NC	
15	G2	GREEN data signal(LSB)	
16	G3	GREEN data signal	
17	G4	GREEN data signal	
18	G5	GREEN data signal	
19	G6	GREEN data signal	
20	G7	GREEN data signal(MSB)	
21	B0	NC	NC for 6bit mode
22	B1	NC	
23	B2	BLUE data signal(LSB)	
24	B3	BLUE data signal	
25	B4	BLUE data signal	
26	B5	BLUE data signal	
27	B6	BLUE data signal	
28	B7	BLUE data signal(MSB)	
29	GND	GND(0V)	
30	DOTCLK	Pixel clock signal	
31	CS	Chip select / Power On	
32	Hsync	Horizontal synchronizing signal	
33	Vsync	Vertical synchronizing signal	
34	EN	Data Enable	Note 1
35	GND	GND(0V)	
36	REST	Reset	
37	ID	NC on FPC	
38	SCL	Serial clock	
39	SDI	Serial data input	
40	GND	GND(0V)	

Pin No.	Symbol	Description	Note
41	X1	X right	
42	Y1	Y bottom	
43	X2	X left	
44	Y2	Y top	
45	GND	GND(0V)	
46	LED-	LED (Cathode side)	
47	Dummy	NC on FPC	
48	LED+	LED (Anode side)	
49	GND	GND(0V)	
50	GND	GND(0V)	

Note1) When use H/V mode, connect to VDDIO

5. Absolute Maximum Ratings

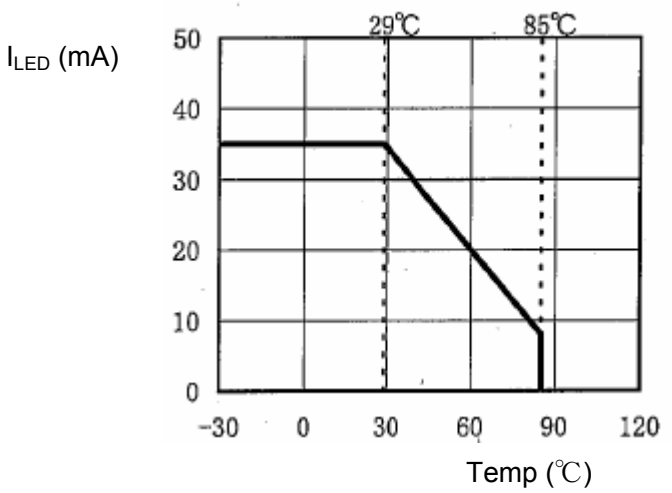
Item	Symbol	Conditions	Rated value	Unit	Remarks
Input voltage	VI	Ta = 25°C	-0.3 ~ V_{DDIO}+0.3	V	Note 1
Logic I/O power supply voltage	V_{DDIO}	Ta = 25°C	-0.3 ~ +4.0	V	
Analog power supply voltage	V_{CI}	Ta = 25°C	AGND-0.3 ~ +5.0	V	
Temperature for storage	Tstg	-	-30 ~ +80	°C	Note 2
Temperature for operation	Topr	-	-20 ~ +70	°C	Note 3
LED input electric current	I_{LED}	Ta = 25°C	35	mA	Note 4
LED electricity consumption	P_{LED}	Ta = 25°C	123	mW	Note 4

Note 1) RESB, SHUT, CSB, SDI, SCK, DEN, B5~B0, G5~G0, R5~R0, VSYNC, HSYNC, DOTCLK

Note 2) Humidity: 95%RH Max. (Ta≦40°C)
Maximum bulb temperature under 39°C (Ta>40°C) See to it that no dew will be condensed.

Note 3) Panel surface temperature prescribes.

Note 4) Power consumption of one LED (Ta = 25°C). (use 6 pieces LED)
Ambient temperature and the maximum input are fulfilling the following operating conditions.



Ambient temperature and the maximum input

6. Electrical Characteristics

6-1. TFT LCD Panel Driving

Ta = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Logic I/O power supply	DC voltage	V_{DDIO}	+2.5	+3.3	+3.6	V	
	DC Current	I_{VDDIO}	-	0.35	0.50	mA	Note 1
Analog power supply	DC voltage	V_{CI}	+3.0	+3.3	+3.6	V	
	DC Current	I_{VCI}	-	13	18	mA	Note 1
Permissive input Ripple voltage		$V_{RFVDDIO}$	-	-	100	mVp-p	Note 2
		V_{RFVCI}	-	-	100	mVp-p	Note 2
Logic Input Voltage	High	V_{IH}	0.8 V_{DDIO}	-	V_{DDIO}	V	Note 3
	Low	V_{IL}	0	-	0.2 V_{DDIO}	V	Note 3
Logic input Current		I_{IH} / I_{IL}	-1	-	1	μA	Note 3

Note 1) V_{DDIO} = V_{CI} = +3.3V

Current situation for I_{VDDIO}: Black & White checker flag pattern

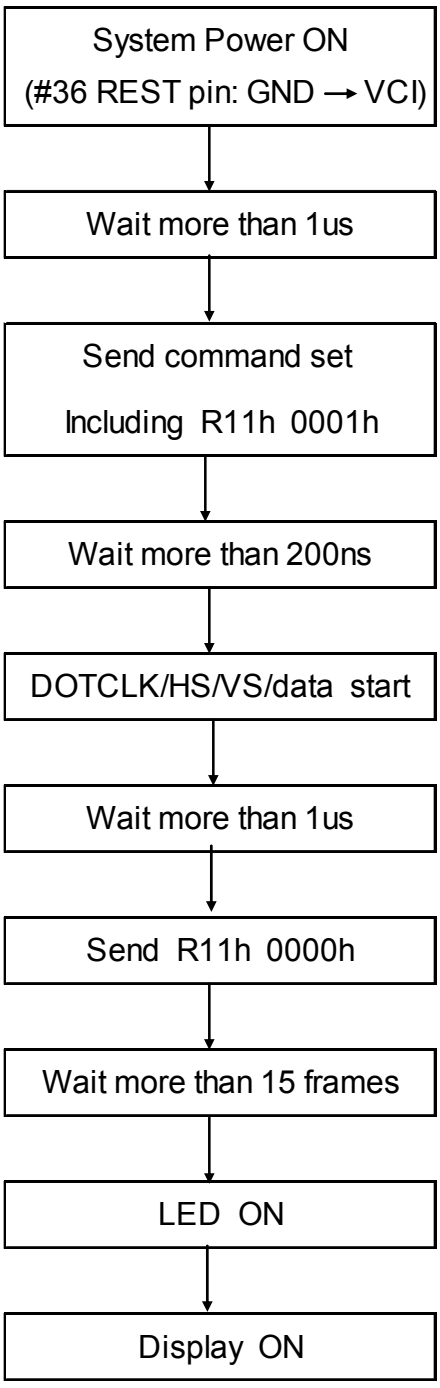
Current situation for I_{CI}: All black pattern

F_{DOTCLK}: 5MHz

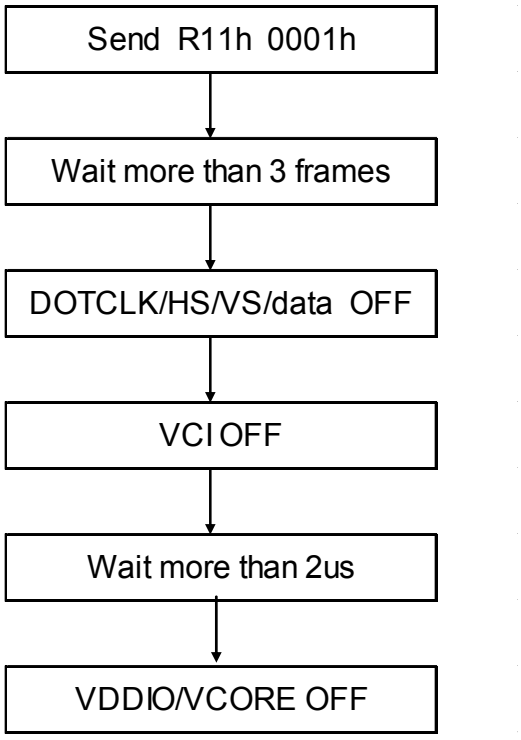
Note 2) V_{DDIO} = V_{CI} = +3.3V

Note 3) RESB, SHUT, CSB, SDI, SCK, DEN, B7~B0, G7~G0, R7~R0, VSYNC, HSYNC, DOTCLK

6-2. Start up sequence



6-3.Power down sequence



6-4. Register Setting

Reg. #	Register	Data (Gamma 2.2)	Remark
R01 h	Driver output control	2AEF h	
R02 h	LCD driving AC control	0300 h	
R03 h	Power control 1	080E h	
R0B h	Frame cycle control	D000 h	
R0C h	Power control 2	0005h	
R0D h	Power control 3	000F h	
R0E h	Power control 4	2C00 h	
R11 h	Shut and 8 color	0000 h	Note 1
R12 h	Entry Mode	0064 h	Note 2
R16 h	Pixel per line	9F86 h	Note3
R17 h	Vertical porch	0002 h	Note4
R1E h	Power control 5	0000 h	
R28 h	Extended command 1	0006 h	
R2A h	Extended command 2	0187 h	
R30 h	Gamma control 1	0000 h	
R31 h	Gamma control 2	0103 h	
R32 h	Gamma control 3	0001 h	
R33 h	Gamma control 4	0501 h	
R34 h	Gamma control 5	0607 h	
R35 h	Gamma control 6	0406 h	
R36 h	Gamma control 7	0707 h	
R37 h	Gamma control 8	0305 h	
R3A h	Gamma control 9	0F0F h	
R3B h	Gamma control 10	0F02 h	

***In case is HS/VS mode**

NOTE: R12h=0060h: DEN mode

R12h=0064h: HS/VS mode

Note 1)

Shut and 8 color (R11h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	CM	0	0	0	0	0	0	0	SHUT
POR		0	0	0	0	0	0	0	X	0	0	0	0	0	0	0	X

CM: When CM = 1, 8-color mode is selected.
When CM = 0, 262k color mode is selected.

SHUT: When SHUT = 1, the driver enters into the sleep mode. In the sleep mode, the internal display operations are halted.

Note: **The default setting of register bits CM and SHUT are defined by the logic stage of corresponding hardware pins. These bits will override the hardware setting once software command was sent to set the bits.**
Enter sleep mode automatically while VCI is lower than 2.4V +/-0.1V.

Note 2)

Entry Mode (R12h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	IF1	IF0	CMI	IFS1	IFS0	0	0
POR		0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0

R12h	18-bit parallel	DEN mode	SYNC mode
0060h	Yes	Yes	No
0064h	Yes	No	Yes

Note: **For DEN mode, minimum vertical porch = 2 and minimum horizontal porch = 4**

Note 3)

Pixel per line (R16h) (POR = 9F86h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
POR		1	0	0	1	1	1	1	1	1	0	0	0	0	1	1	0

Note: Number of dotclk for hsync active low period must be smaller than that of HBP

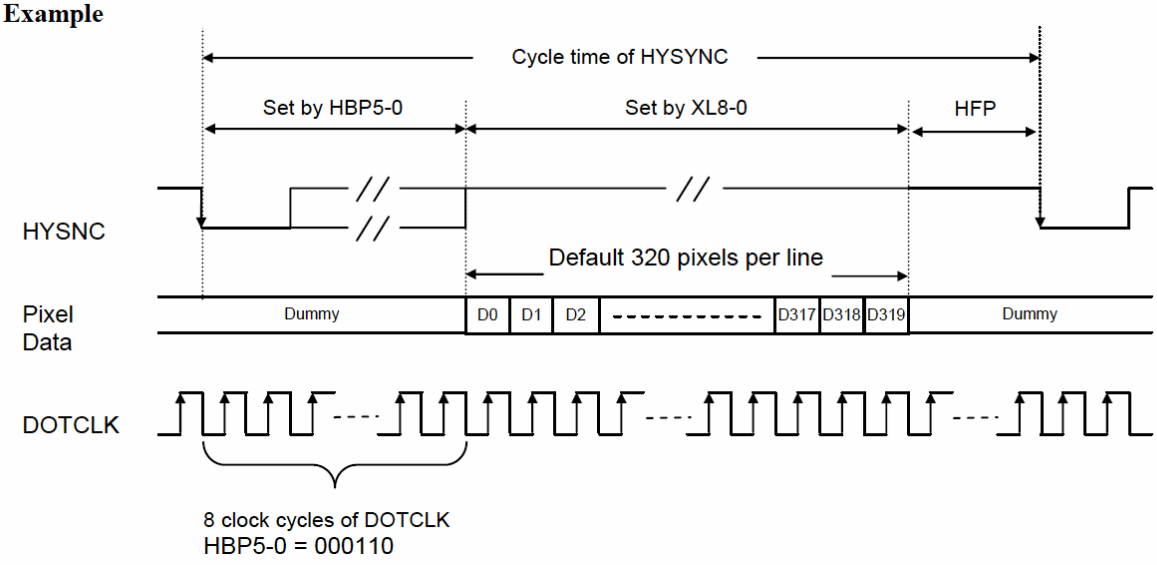
XL8-0: Set the number of valid pixel per line.

XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	No. of pixel per line
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
				:					: Step = 1 :
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1	1	320
1	0	1	*	*	*	*	*	*	Reserved
1	1	*	*	*	*	*	*	*	Reserved

HBP5-0: Set the delay period from falling edge of HSYNC signal to first valid data.

HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of clock cycle of DOTCLK
0	0	0	0	0	0	2
0	0	0	0	0	1	3
0	0	0	0	1	0	4
0	0	0	0	1	1	5
0	0	0	1	0	0	6
0	0	0	1	0	1	7
0	0	0	1	1	0	8
0	0	0	1	1	1	9
0	0	1	0	0	0	10
			:			: Step = 1 :
1	1	1	1	1	0	64
1	1	1	1	1	1	65

Example



The formula of setting for control signals: f_DOTCLK, t_HBP , t_HFP

t_VBP,t_VFP

fv=60±5HZ

fv=f_DOTCLK/(V_cycleXH_cycle)

V_cycle=240+t_VBP+t_VFP

H_cycle=320+t_HBP+t_HFP≤512

Note 4)

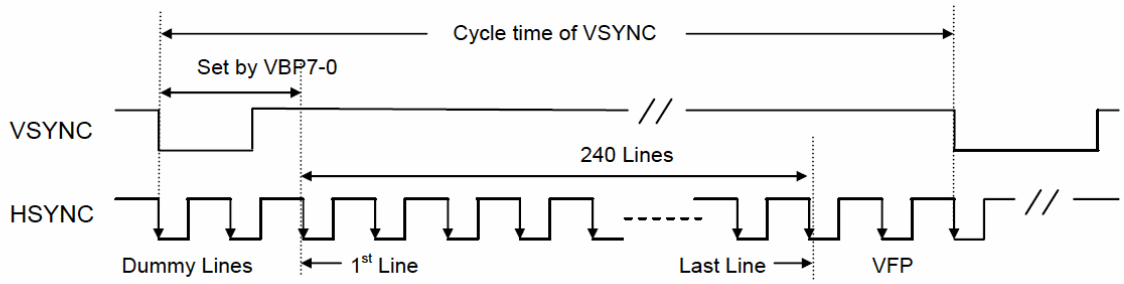
Vertical Porch (R17h) (POR = 0002h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

VBP7-0: Set the delay period from falling edge of VSYNC to first valid line. The line data within this delay period will be treated as dummy line.

VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
0	0	0	0	0	1	0	0	4
:	:	:	:	:	:	:	:	: Step = 1 :
1	1	1	0	1	1	1	1	239
1	1	1	1	0	0	0	0	240
1	1	1	1	*	*	*	*	Reserved

Example



The formula of setting for control signals: f_DOTCLK, t_HBP , t_HFP

t_VBP,t_VFP

fv=60±5HZ

fv=f_DOTCLK/(V_cycleXH_cycle)

V_cycle=240+t_VBP+t_VFP

H_cycle=320+t_HBP+t_HFP≤512

6-5. Back light driving

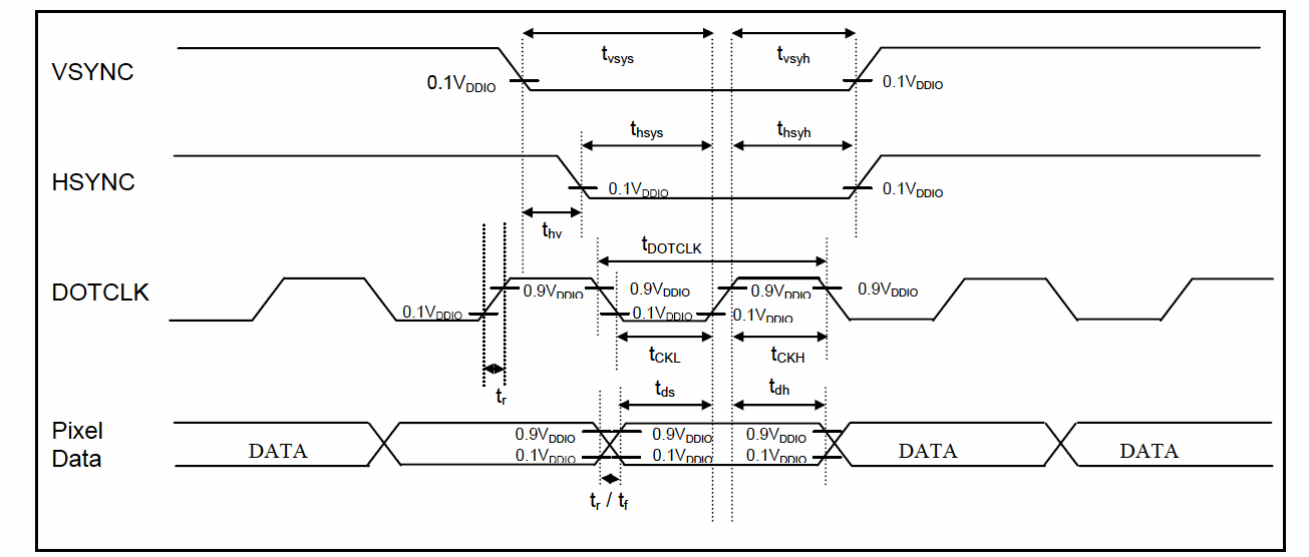
The back light system has 6 LEDs

[GM4BW643B2A]

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Rated Voltage	V_{BL}	-	19.2	21	V	
Rated Current	I_L	-	20	-	mA	Ta=25°C
Power consumption	W_L	-	400	-	mW	

7. Timing characteristics of input signals

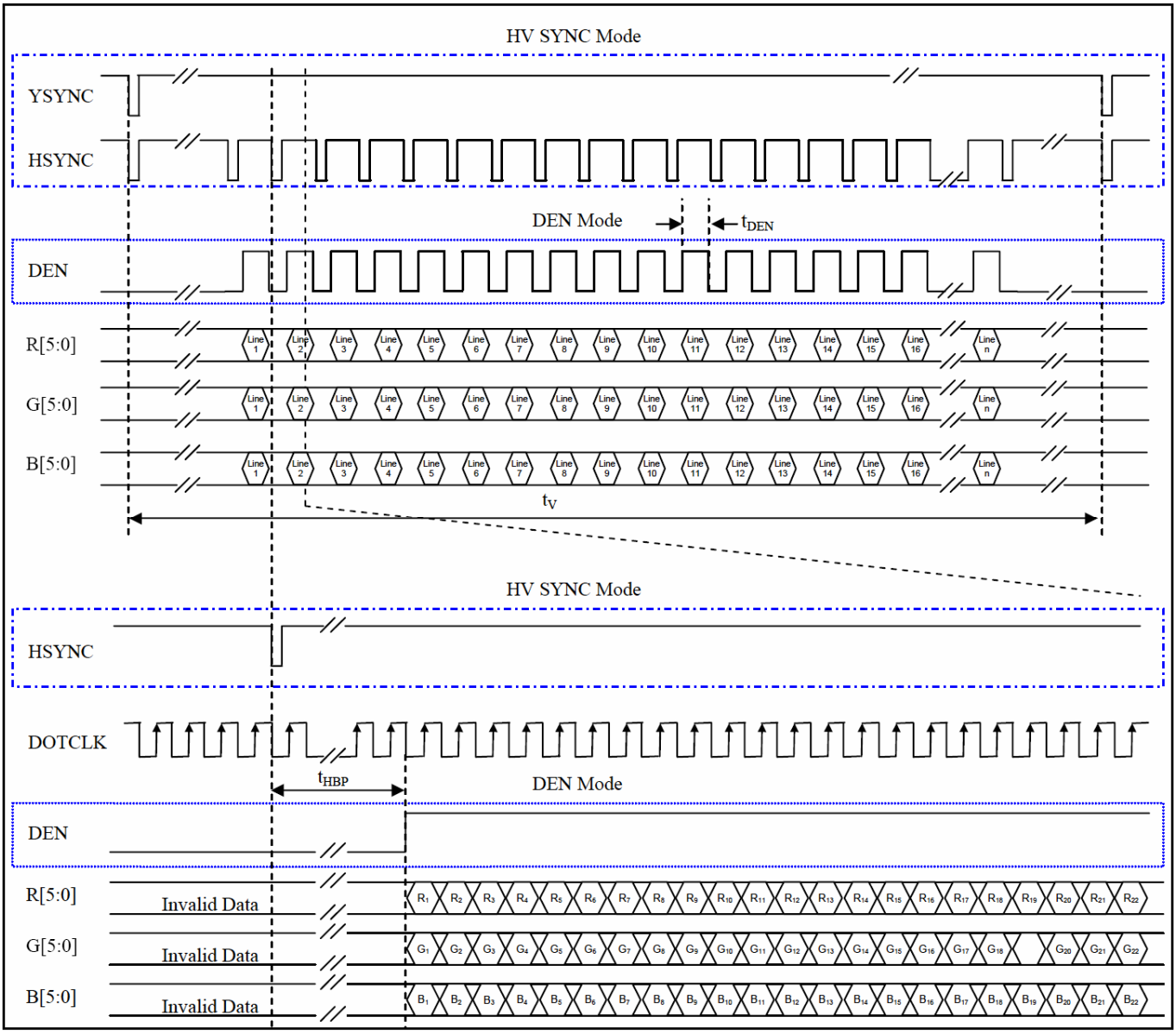
7-1. Pixel Clock Timing



Pixel Clock Timing

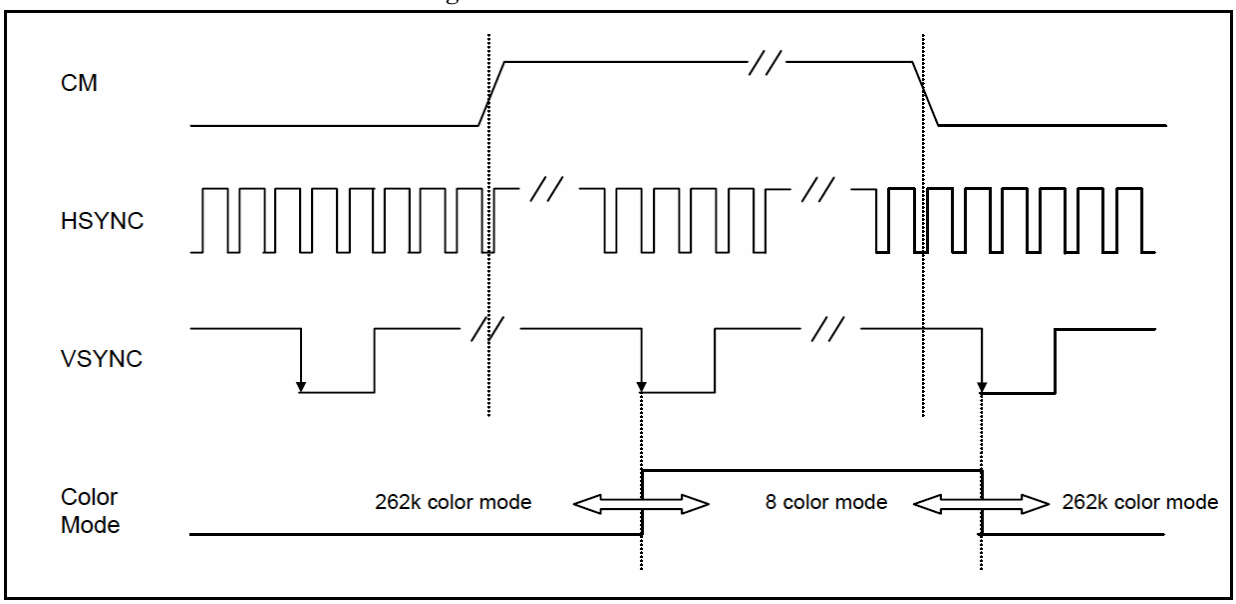
Characteristics	Symbol	Target Min	Target Typ	Target Max	Units
DOTCLK Frequency	f_{DOTCLK}	-	5	8	MHz
DOTCLK Period	t_{DOTCLK}	125	200	-	nSec
Pixel Clock Period	t_{PIXCLK}	-	1	-	t_{DOTCLK}
Pixel Clock Frequency	f_{PIXCLK}	-	5	8	MHz
Vertical Sync Setup Time	t_{vsys}	5	-	-	nSec
Vertical Sync Hold Time	t_{vsyh}	5	-	-	nSec
Horizontal Sync Setup Time	t_{hsys}	5	-	-	nSec
Horizontal Sync Hold Time	t_{hsyh}	5	-	-	nSec
Phase difference of Sync Signal Falling Edge	t_{hv}	0	-	320	t_{DOTCLK}
DOTCLK Low Period	t_{CKL}	16	-	-	nSec
DOTCLK High Period	t_{CKH}	16	-	-	nSec
Data Setup Time	t_{ds}	10	-	-	nSec
Data Hold Time	t_{dh}	10	-	-	nSec
Reset Pulse Width	t_{RES}	2.5	-	-	uSec
Rise / Fall Time	t_r / t_f	5	-	25	nSec

7-2. 18-bit RGB Interface Timing Diagram & Transaction Example



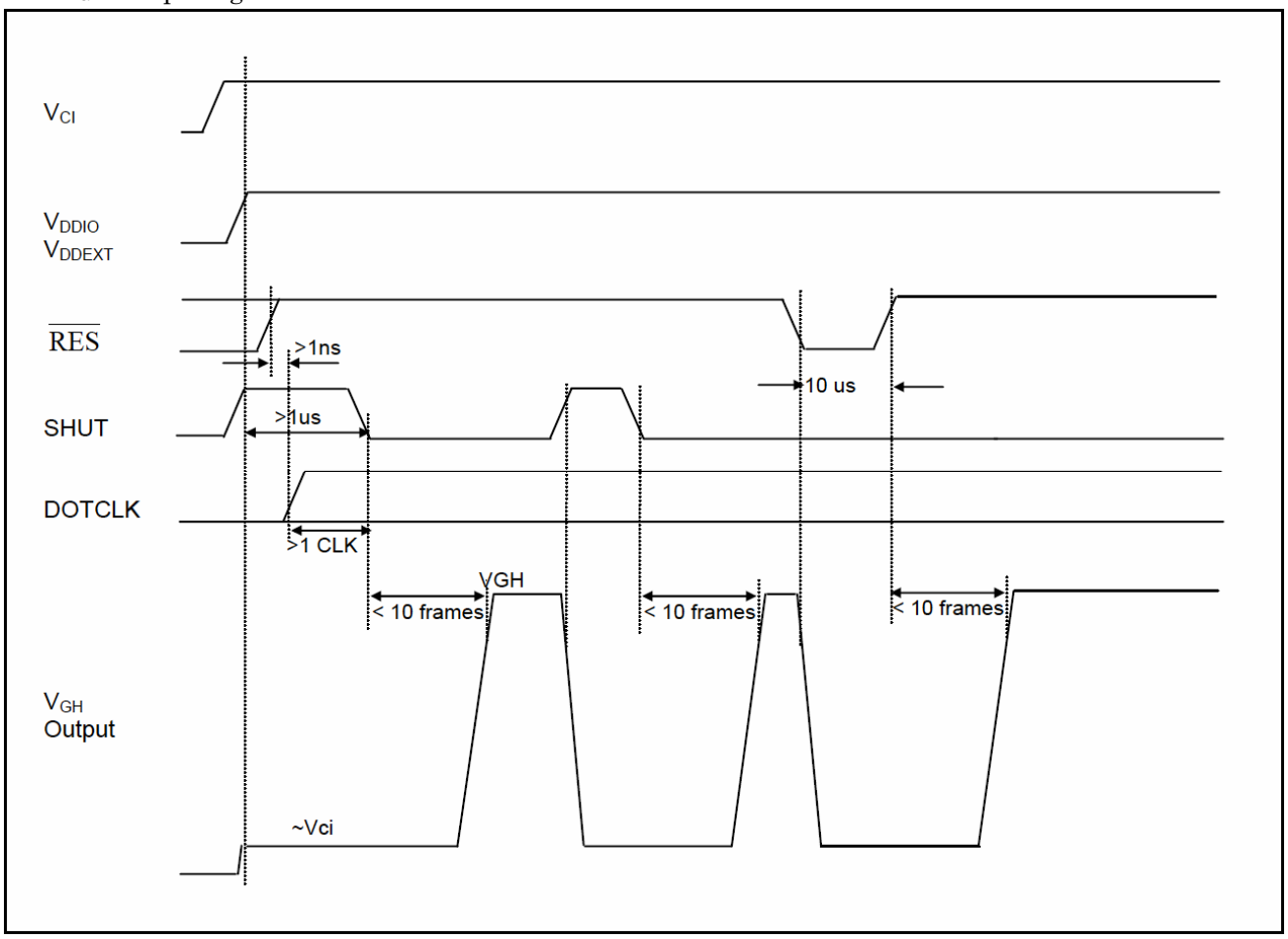
Characteristics		Symbol	HV SYNC Mode	DEN Mode	Units
Serial Clock Frequency		$1/t_{DOTCLK}$	5	5	MHz
Horizontal	One Line Period	t_H	336	336	t_{DOTCLK}
	Active Data Period	t_{data}	320	320	t_{DOTCLK}
	Horizontal Back Porch	t_{HBP}	8	-	t_{DOTCLK}
	Horizontal Front Porch	t_{vsys}	8	-	t_{DOTCLK}
	Data Enable Period	t_{DEN}	-	320	t_{DOTCLK}
Vertical	One Field Period	t_V	244	244	t_H
	Active Line Period	t_{AL}	240	240	t_H
	Vertical Back Porch	t_{VBP}	2	-	t_H
	Vertical Front Porch	t_{VFP}	2	-	t_H

7-3. Color Mode Conversion Timing



Note: The color mode conversion starts at the first falling edge of VSYNC after stage change of CM.

7-4. V_{GH} Output against SHUT & RESB



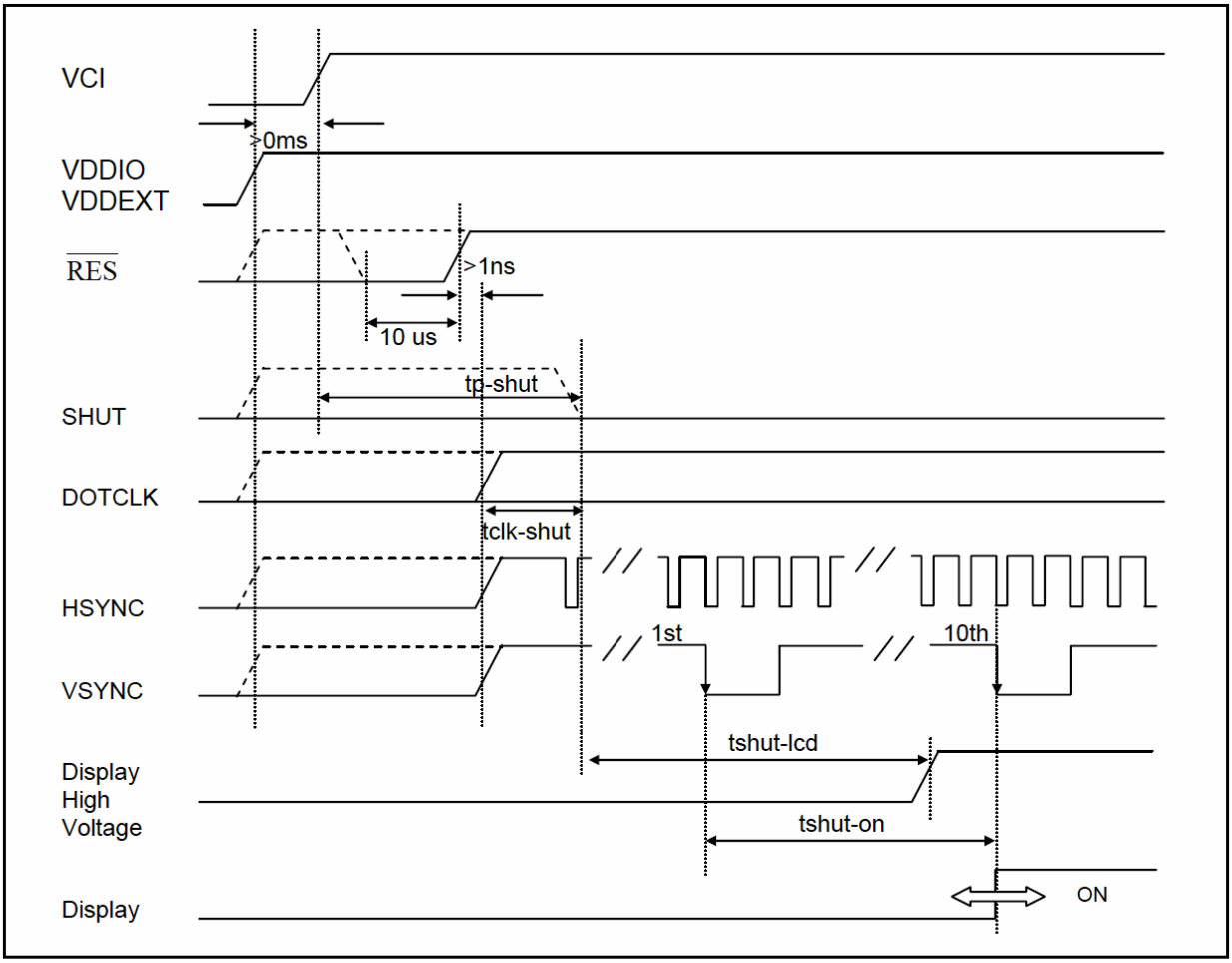
Note1: The minimum cycle time of SHUT is 10 + 2 frames.

Note2: DOTCLK must be provided for boosting of VGH. The above timing diagram assumed voltages and DOTCLK are continuous supplied after power on.

Note3: VGH will be forced to VCI at the low stage of RES.

Note4: The minimum pulse width of RESET is 10us.

7-5. Power Up Sequence

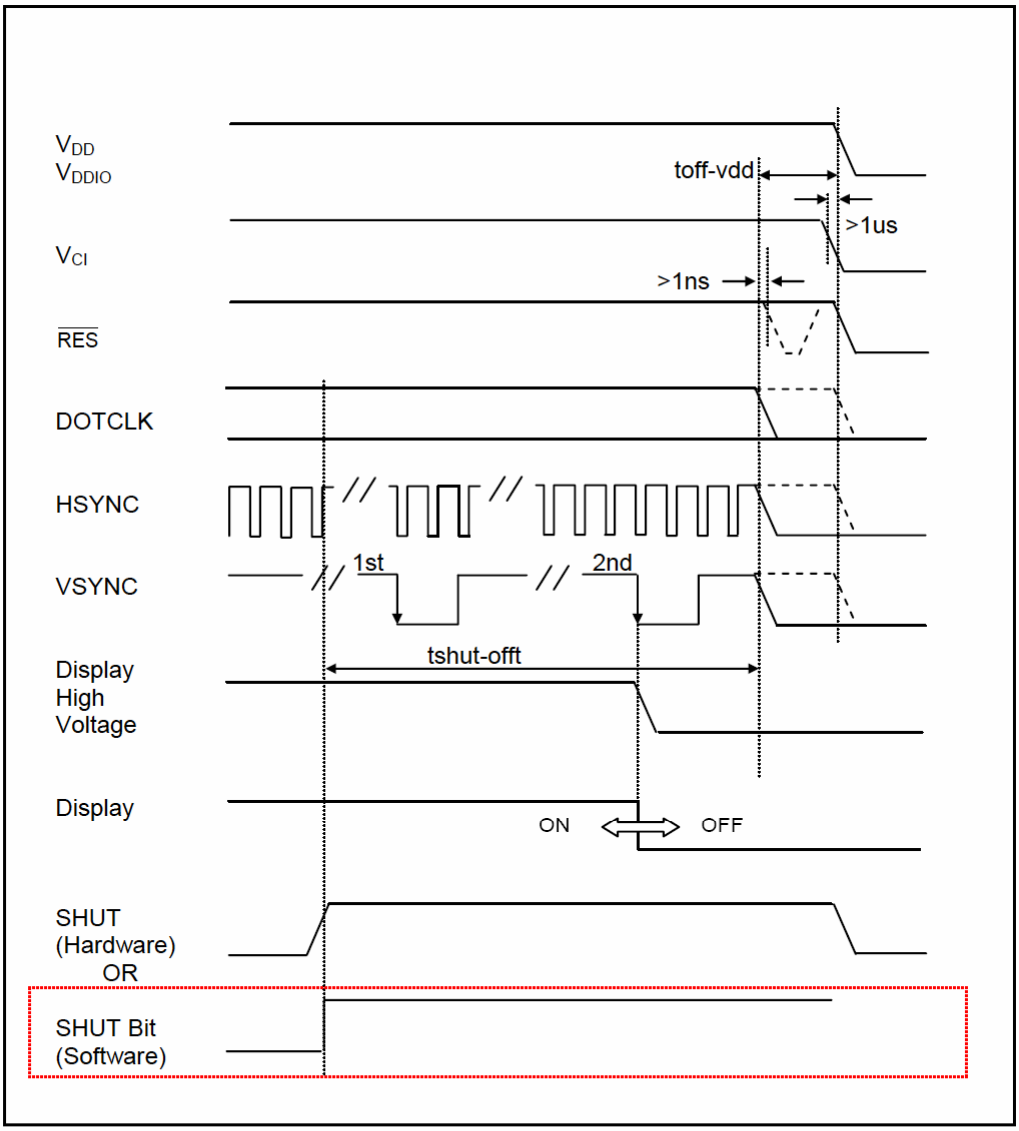


Characteristics	Symbol	Target Min	Target Typ	Target Max	Units
V_{DDEXT} / V_{DDIO} on to falling edge of SHUT	tp-shut	1	-	-	µsec
Start of DOTCLK to SHUT low	tclk-shut	1	-	-	DOTCLK
Falling edge of SHUT to LCD power on	tshut-lcd	-	-	164	msec
Falling edge of SHUT to display start	tshut-on	-	-	10	frame
-- 1 line: 336 clk -- 1 frame: 244 line -- PIXCLK = 5.0MHz		-	164	-	msec

Note1: It is necessary to input DOTCLK before the falling edge of SHUT.

Note2: Display starts at 10th falling edge of VSTNC after the falling edge of SHUT.

7-6. Power Down Sequence



Characteristics	Symbol	Target Min	Target Typ	Target Max	Units
Rising edge of SHUT to display off -- 1 line: 336 clk -- 1 frame: 244 line -- PIXCLK = 5.0 MHz	tshut-off	2	-	-	frame
		32.8	-	-	msec
Input-signal-off to V_{DDEXT} / V_{DDIO} off	toff-vdd	1	-	-	µsec

Note1: DOTCLK must be maintained at lease 2 frames after the rising edge of SHUT.

Note2: Display become off at the 2nd falling edge of VSTNC after the falling edge of SHUT.

Note3: If RESET signal is necessary for power down, provide it after the 2-frames-cycle of the SHUT period.

7-7. SPI Interface Timing Diagram & Transaction Example (24bit)

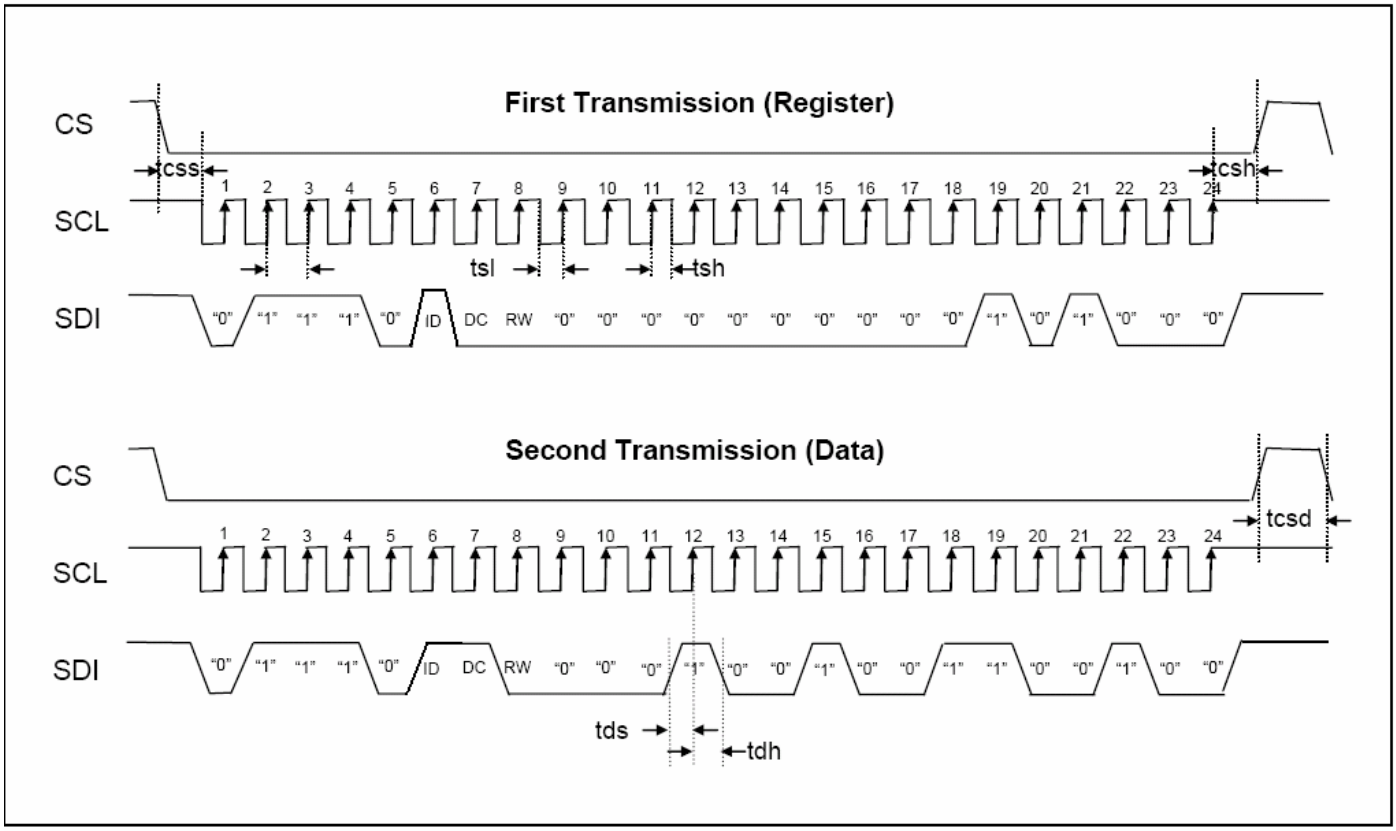


Figure 15-6 - SPI Interface Timing Diagram & Transaction Example

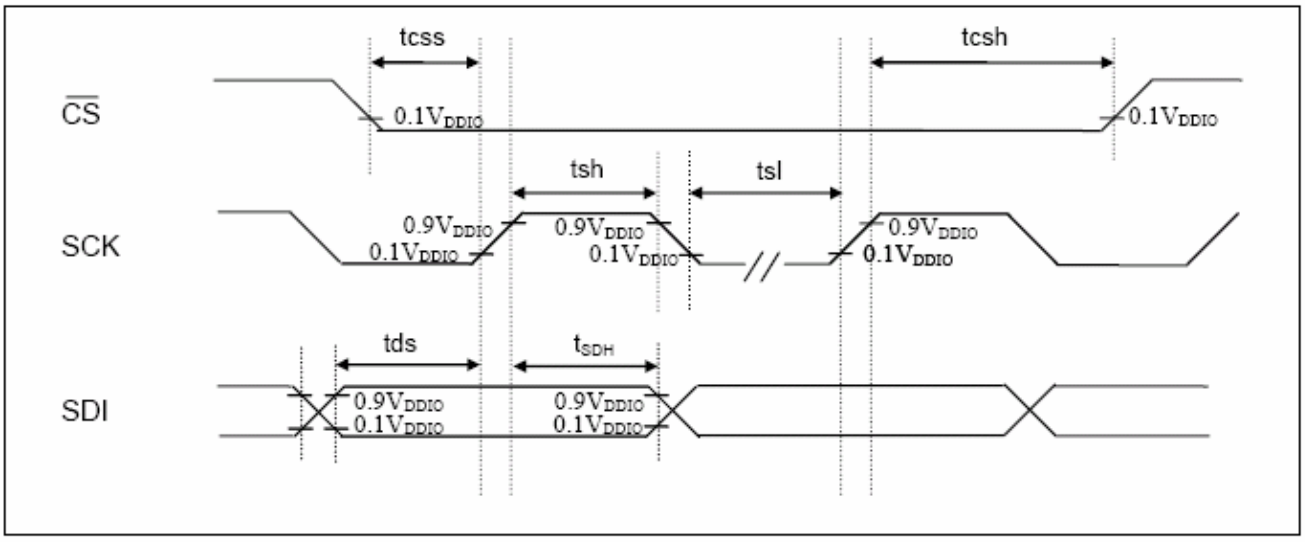
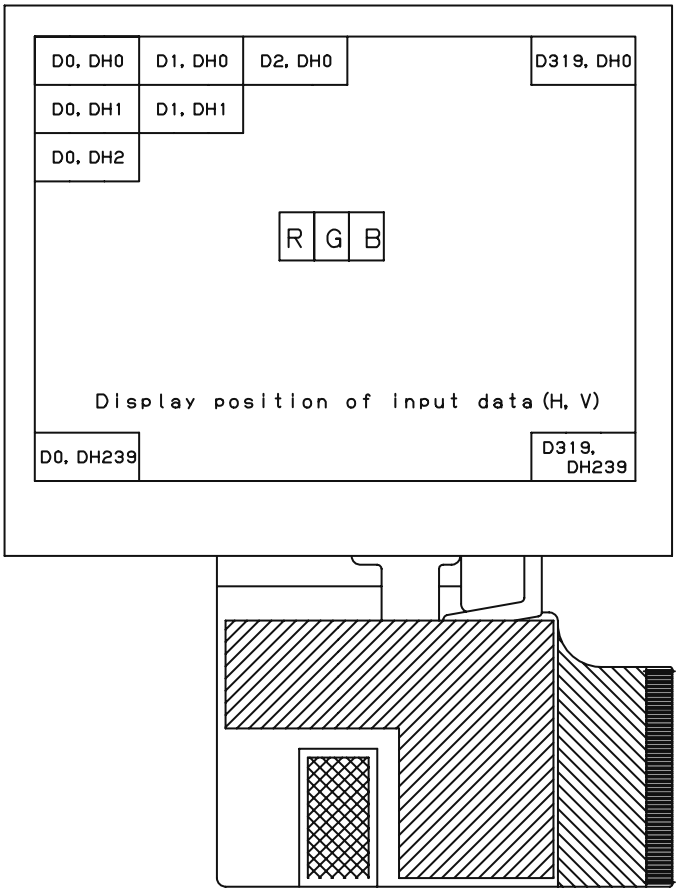


Figure 15-7 - SPI Interface Timing Diagram

Characteristics	Symbol	Target Min	Target Typ	Target Max	Units
Serial Clock Frequency	fclk	-	-	20	MHz
Serial Clock Cycle Time	tclk	50	-	-	nsec
Clock Low Width	tsl	25	-	-	nsec
Clock High Width	tsh	25	-	-	nsec
Chip Select Setup Time	tcss	0	-	-	nsec
Chip Select Hold Time	tcsh	10	-	-	nsec
Chip Select High Delay Time	tcsd	20	-	-	nsec
Data Setup Time	tds	5	-	-	nsec
Data Hold Time	tdh	10	-	-	nsec

7-8. Input Data Signals and Display Position on the screen



Please refer to Input Terminal Names and Functions

8. Input Signals, Basic Display Colors and Gray Scale of Each Color

	Colors & Gray Scale	Gray Scale	Date signal																	
			R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5
			LSB					MSB	LSB					MSB	LSB					MSB
Basic Color	Black	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	–	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	–	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	–	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	–	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	–	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	–	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	GS62	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS63	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
	⇩	GS62	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	GS63	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
	⇩	GS62	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Blue	GS63	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

0: Low level voltage, 1: High level voltage

Each basic color can be displayed in 64 gray scales from 6 bit data signals.
According to the combination of 18 bit data signals, the 262k color display can be achieved on the screen.

9. Optical Characteristics

Ta = 25°C, V_{DDIO} = +3.3V, V_{CI} = +3.3V

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range (Without Wide View)	Horizontal	θ21	CR＞10	-	60	-	deg.	【Note1,4】
		θ22		-	60	-	deg.	
	Vertical	θ11		-	40	-	deg.	
		θ12		-	60	-	deg.	
Contrast ratio		CR	Optimum viewing angle	100	300	-		【Note2,4】
Response Time	Rise	Tr	θ=0°	-	30	45	ms	【Note3,4】
	Decay	Td		-	30	45	ms	
Chromaticity of White		x		0.26	0.31	0.36		【Note4】
		y		0.29	0.34	0.39		
Chromaticity of Red		X		0.54	0.59	0.64		【Note4】
		Y		0.25	0.30	0.35		
Chromaticity of Green		X		0.27	0.32	0.37		【Note4】
		Y		0.50	0.55	0.60		
Chromaticity of Blue		X		0.08	0.13	0.18		【Note4】
		y		0.04	0.09	0.14		
Luminance of white		X_{L1}		250	320	-	cd/m^2	I_{LED}=20mA 【Note6】
NTSC ratio					50	-	%	
Uniformity		U		70	80	-	%	【Note5】

* The optical characteristics measurements are operated under a stable luminescence (I_{LED} = 20mA) and a dark condition. (Refer to Fig.9-1)

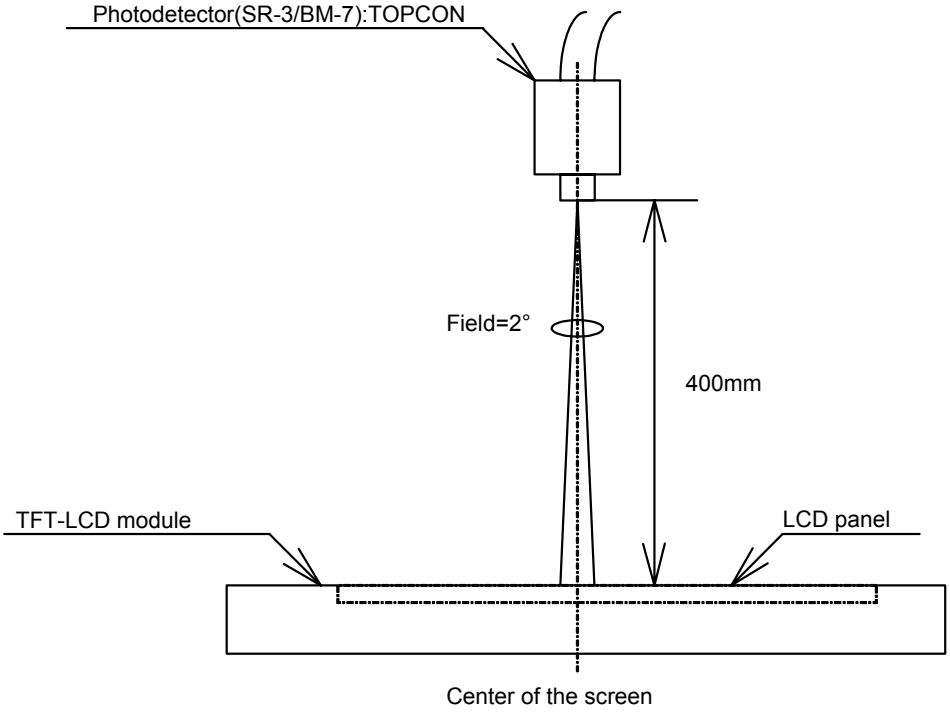
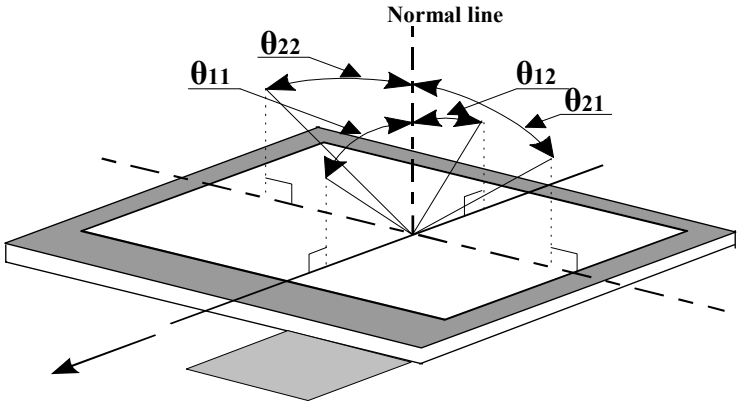


Fig.9-1 Optical characteristics measurement method

【 Note 1 】Definitions of viewing angle range



6 o'clock direction

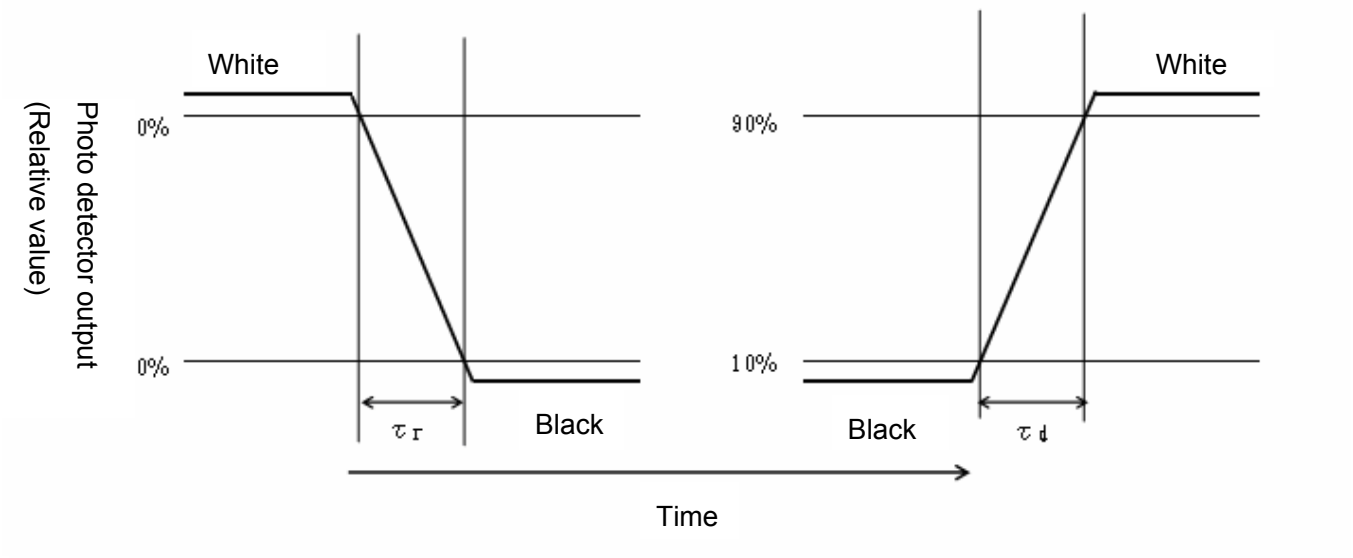
【 Note 2 】Definition of contrast ratio

The contrast ratio is defined as the following

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

【 Note 3 】Definition of response time

The response time is defined as the following figure and shall be measured by switching the input signal for "Black" and "White"

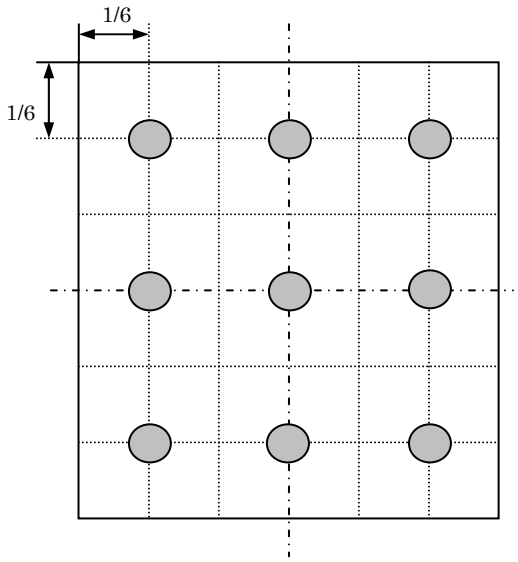


【 Note 4 】This shall be measured at center of the screen.

【 Note 5 】Definition of Uniformity

$$\text{Uniformity} = \frac{\text{Minimum Brightness}}{\text{Maximum Brightness}} \times 100\,(\%)$$

The brightness should be measured on the 9-point as shown in the right figure.



【 Note 6 】This shall be measured on the 9-point as shown in the right figure.

$$\text{Luminance of white} = \frac{\text{Summation of the 9 - point Brightness}}{9}$$

10. Touch panel characteristics

Parameter	Min.	Typ.	Max.	Unit	Remark
Input voltage	-	5.0	7.0	V	
Resistor between terminals(XL-XR)	200	603	900	Ω	Provisional specification
Resistor between terminals(YU-YD)	200	372	900	Ω	
Line linearity(X direction)	-	-	1.5	%	
Line linearity(Y direction)	-	-	1.5	%	
Insuration resistance	20	-	-	MΩ	at DC25V
Minimum tension for detecting	-	-	0.79	N	

Note) For use of finger input

11. Handling of modules

11-1. Inserting the FPC into its connector and pulling it out

1) Be sure to turn off the power supply and the signals when inserting or disconnecting the cable.
2) Please insert for too much stress not to join FPC in the case of insertion of FPC.

11-2. About handling of FPC

1) The bending radius of the FPC should be more than 0.6mm, and it should be bent evenly.
2) Do not dangle the LCD module by holding the FPC, or do not give any stress to it.

11-3. Mounting of the module

1) The module should be held on to the plain surface. Do not give any warping or twisting stress to the module.
2) Please consider that GND can ground a modular metal portion etc. so that static electricity is not charged to a module.
3) Design guidance for touch panel (T/P)
   a) Example of housing design
      (1) If a consumer will put a palm on housing in normal usage, care should be taken as follows.
      (2) Keep the gap, for example 0.3 to 0.7mm, between bezel edge and T/P surface.
      The reason is to avoid the bezel edge from contacting T/P surface that may cause a “short” with bottom layer. (See Fig.11-3-1)
      (3) Insertion a cushion material is recommended.
      (4) The cushion material should be limited just on the busbar insulation paste area.
      If it is over the transparent insulation paste area, a ”short” may be occurred.
      (5) There is one where a resistance film is left in the T/P part of the end of the pole.
      Design to keep insulation from the perimeter to prevent from mis-operation and so on.

b) Mounting on display and housing bezel

(1) In all cases, the T/P should be supported from the backside of the Plastic.

(2) Do not to use an adhesive-tape to bond it on the front of T/P and hang it to the housing bezel.

(3) Never expand the T/P top layer (PET-film) like a balloon by internal air pressure.
The life of the T/P will be extremely short.

(4) Top layer, PET, dimension is changing with environmental temperature and humidity.
Avoid a stress from housing bezel to top layer, because it may cause “waving”.

(5) The input to the touch panel sometimes distorts touch panel itself.

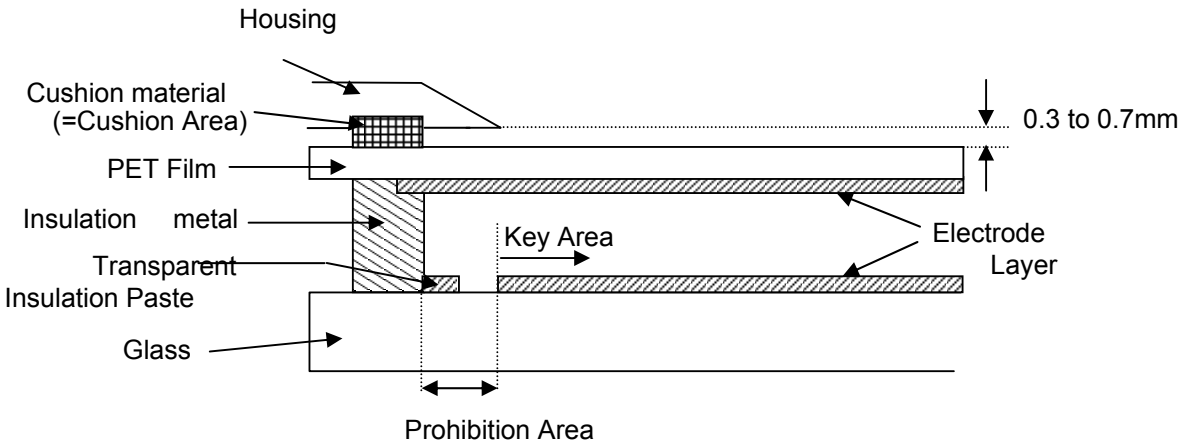


Fig.11-3-1

11-4. Cautions in assembly / Handling pre cautions

As the polarizer can be easily scratched, be most careful in handling it.

1) Work environments in assembly.
Working under the following environments is desirable:

a) Implement more than 1MΩ conductive treatment (by placing a conductive mat or applying conductive paint) on the floor or tiles.

b) No dusts come in to the working room. Place an adhesive, anti-dust mat at the entrance of the room.

c) Humidity of 50 to 70% and temperature of 15 to 27°C are desirable.

d) All workers wear conductive shoes, conductive clothes, conductive fingerstalls and grounding belts without fail.

e) Use a blower for electrostatic removal. Set it in a direction slightly tilt downward so that each Module can be well subjected to its wind. Set the blower at an optimum distance between the blower and the module.

2) How the remove dust on the polarizer

a) Blow out dust by the use of an N2 blower with antistatic measures taken. Use of an ionized air Gun is recommendable.

b) When the panel surface is soiled, wipe it with soft cloth.

3) In the case of the module’s metal part (shield case) is stained, wipe it with a piece of dry, soft cloth.
If rather difficult, give a breath on the metal part to clean better.

4) If water dropped, etc. remains stuck on the polarizer for a long time, it is apt to get discolored or cause stains. Wipe it immediately.
5) As a glass substrate is used for the TFT-LCD panel, if it is dropped on the floor or hit by something hard, it may be broken or chipped off.
6) Since CMOS LSI is used in this module, take care of static electricity and take the human earth into consideration when handling.

11-5. Others

1) Regarding storage of LCD modules, avoid storing them at direct sunlight-situation.
   You are requested to store under the following conditions:
   (Environmental conditions of temperature/humidity for storage)
   a) Temperature: 0 to 40°C
   b) Relative humidity : 95% or less
      As average values of environments (temperature and humidity) for storing, use the following control guidelines:
      Summer season: 20 to 35°C, 85% or less Winter season: 5 to 15°C, 85% or less
      If stored under the conditions of 40°C and 95% RH, cumulative time of storage must be less than 240 hours.
2) If stored at temperatures below the rated values, the inner liquid crystal may freeze, causing cell destruction. At temperatures exceeding the rated values for storage, the liquid crystal may become isotropic liquid, making it no longer possible to come back to its original state in some cases.
3) If the LCD is broken, do not drink liquid crystal in the mouth. If the liquid crystal adheres to a hand or foot or to clothes, immediately cleanse it with soap.
4) If a water drop or dust adheres to the polarizer, it is apt to cause deterioration. Wipe it immediately.
5) Be sure to observe other caution items for ordinary electronic parts and components.
6) If local pressure joins T/P surface for a long time, it will become the cause of generating of Newton's ring.

12. Reliability test items

No.	Test item	Conditions
1	High temperature storage test	Ta = 80°C 240h
2	Low temperature storage test	Ta = -30°C 240h
3	High temperature & high humidity operation test	Ta = 40°C ; 95%RH 240h (No condensation)
4	High temperature operation test	Ta = 70°C 240h
5	Low temperature operation test	Ta = -20°C 240h
6	Vibration test (non- operating)	Frequency range: 10 to 55Hz Stroke: 1.5mm Sweep time: 1minutes Test period: 2 hours for each direction of X,Y,Z
7	Shock test	Direction: ±X, ±Y, ±Z, Time: Third for each direction. Impact value: 980m/s², Action time 6ms
8	Thermal shock test	Ta=-20°C to 70°C /10 cycles (30 min) (30min)
9	Point activation test (Touch panel)	Hit it 100,000 times with a silicon rubber. Hitting force : 2.4 N Hitting speed : 2 times per second
10	Electro static discharge test	±200V·200pF(0Ω) to Terminals(Contact) (1 time for each terminals) ±4kV•150pF(330Ω) to Housing bezel or T/P(Contact) ±8kV•150pF(330Ω) to Housing bezel or T/P(in Air)

【Note】Ta = Ambient temperature, Tp = Panel temperature

【Check items】

(a)Test No.1 to No.8

In the standard condition, there shall be no practical problems that may affect the display function.

(b)Test No.9

The measurements after the tests are satisfied “10 Touch panel characteristics”.

13. Display Grade

The standard regarding the grade of color LCD displaying modules should be based on the delivery inspection standard.

14. Delivery Form

14-1. Carton storage conditions

1) Carton piling-up: Max 8 rows

2) Environments

Temperature: 0～40°C

Humidity: 65% RH or less (at 40°C)

There should be no dew condensation even at a low temperature and high humidity.

3) Packing form: As shown in 16. LCD module packing carton

※Cartons are weak against damp, and they are apt to be smashed easily due to the compressive pressure applied when piled up. The above environmental conditions of temperature and humidity are set in consideration of reasonable pile-up for storage.

14-2. Packing composition

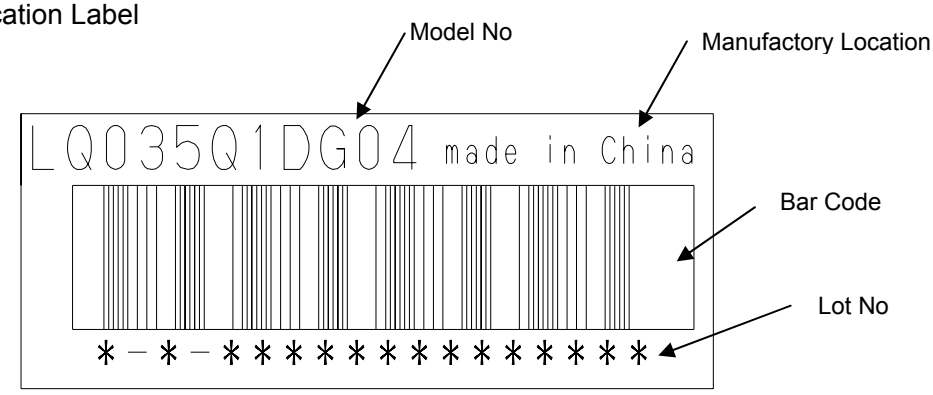
Name	quantity	Note
Carton size	1	575×360×225 (mm)
Tray	12	Material: Electrification prevention polypropylene
(The number of Module)	12	12 unit/tray: 120 unit/carton
Electrification prevention bag	2	Material: Electrification prevention polyethylene 680mm(length)×500mm(depth)×50μm(thin)

Carton weight (120 modules): Approx. 9.8kg

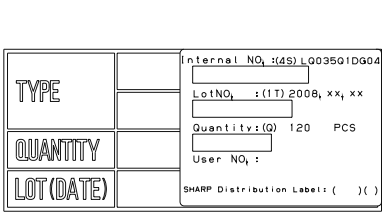
15. Lot No. marking

The lot No. will be indicated on individual labels. The location is as shown

Indication Label



16. LCD module packing carton



[Quantities]
1 tray: 12 modules (MAX)
1 sleeve: 60 modules (MAX)
1 carton: 120 modules (MAX)

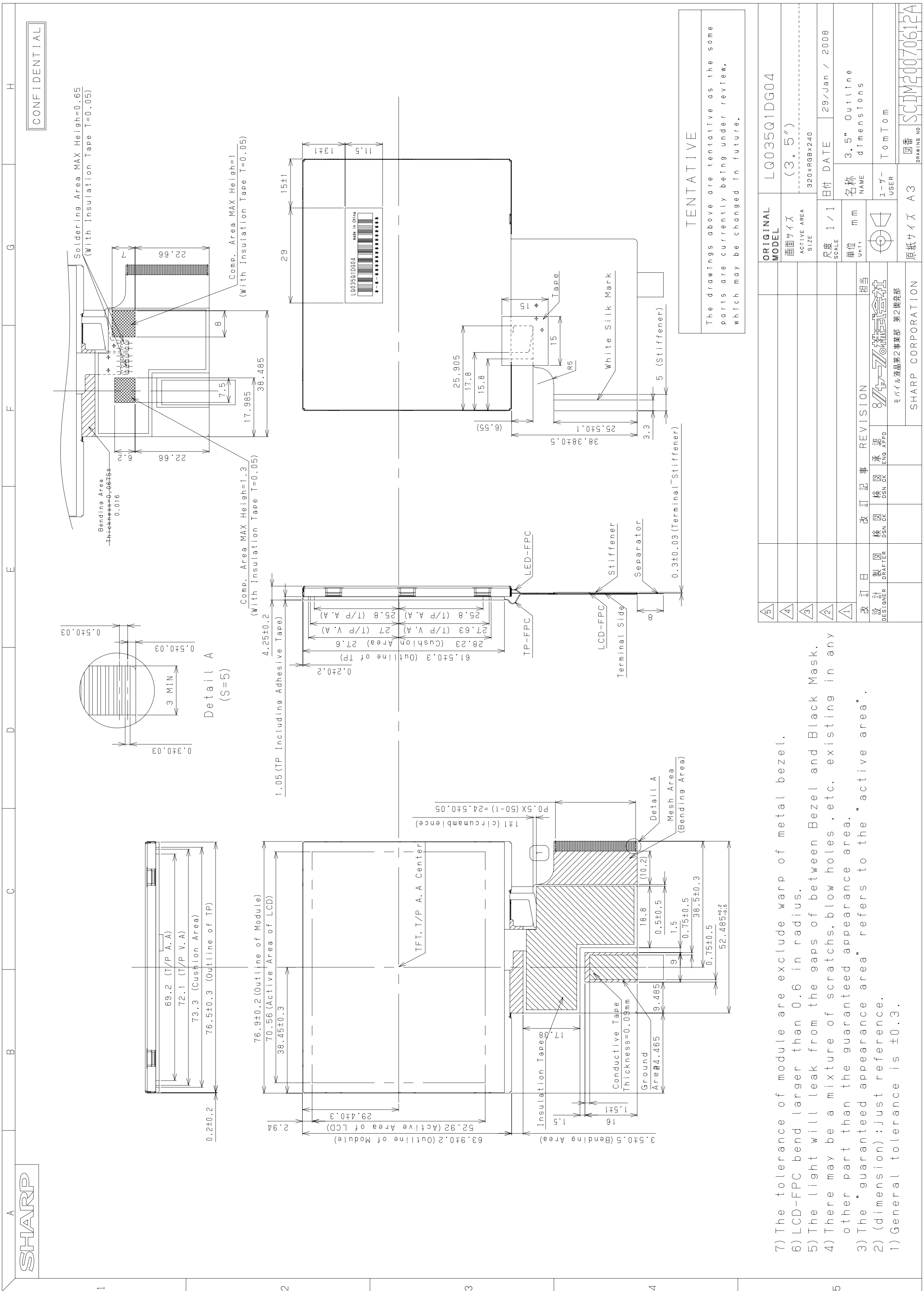
17. Others

1 Disassembling the module can cause permanent damage and you should be strictly avoided.

2 Please be careful that you don’t keep the screen displayed fixed pattern image for a long time, since retention may occur.

3 If you pressed down a liquid crystal display screen with your finger and so on, the alignment disorder of liquid crystal will occur. And then It will become display fault.
Therefore, be careful not to touch the screen directly, and to consider not stressing to it.

4 If any problem arises regarding the items mentioned in this specification sheet or otherwise, it should be discussed and settled mutually in a good faith for remedy and/or improvement.


CONFIDENTIAL
TENTATIVE
The drawings above are tentative as the some parts are currently being under review, which may be changed in future.
7) The tolerance of module are exclude warp of metal bezel.
6) LCD-FPC bend larger than 0.6 in radius.
5) The light will leak from the gaps of between Bezel and Black Mask.
4) There may be a mixture of scratchs,blow holes,etc. existing in any other part than the guaranteed appearance area.
3) The "guaranteed appearance area" refers to the "active area".
2) (dimension):just reference.
1) General tolerance is ±0.3.
ORIGINAL MODEL
LQ035Q1DG04
画面サイズ ACTIVE AREA SIZE
(3.5")
320xRGBx240
尺度 SCALE 1/1
日付 DATE 29/Jan/2008
単位 Unit mm
名称 NAME 3.5" Outline dimensions
ユーザー USER TomTom
原紙サイズ A3
図番 DRAWING NO SCDM2007061PA
SHARP CORPORATION
Detail A (S=5)
76.9±0.2(Outline of Module)
70.56(Active Area of LCD)
63.9±0.2(Outline of Module)
52.92(Active Area of LCD)
61.5±0.3 (Outline of TP)
76.5±0.3 (Outline of TP)
73.3 (Cushion Area)
72.1 (T/P V.A)
69.2 (T/P A.A)
TFT, T/P A.A Center
LED-FPC
TP-FPC
LCD-FPC
Stiffener
Separator
White Silk Mark
Tape
Mesh Area (Bending Area)
Conductive Tape Thickness=0.09mm
Insulation Tape
Ground Area
Comp. Area MAX Heigh=1.3 (With Insulation Tape T=0.05)
Comp. Area MAX Heigh=1 (With Insulation Tape T=0.05)
Soldering Area MAX Heigh=0.65 (With Insulation Tape T=0.05)