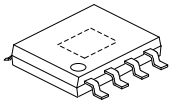
1.0A LOW DROPOUT LINEAR REGULATOR WITH OUTPUT VOLTAGE SETTING OPTIONS



HSOP-8

■ DESCRIPTION

The UTC **LR1802** is a typical LDO that features output voltage setting options, very low dropout voltage as low as 0.3V at output current 1.0A, an enable input and the soft-start reduces inrush current of the load capacitors and minimizes stress on the input power source during start-up. An enable pin to further reduce power dissipation while shutdown..

The UTC **LR1802** is stable with any type of output capacitor of 10μF or more. A precision reference and feedback control deliver 3% accuracy.

■ FEATURES

* Low V_{IN} and wide V_{IN} range: 1.0V~5.5V
* Bias voltage (V_{PP}) range: 3.0V~5.5V
* Low V_{OUT} range: 0.8V~3.3V
* 300mV dropout @1.0A, V_{PP}=5V
* 3% output Voltage
* output voltage setting options
* Programmable soft-start provides linear voltage startup
* Stable with output capacitor≥10μF

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
LR1802L-SH2-R	LR1802G-SH2-R	HSOP-8	Tape Reel

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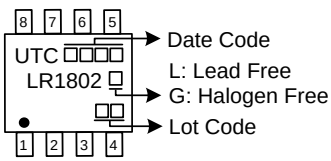
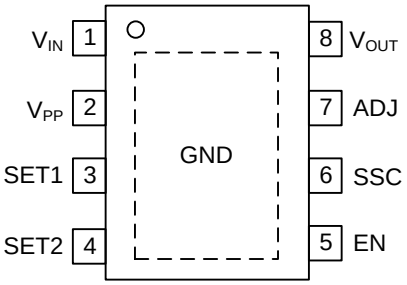
LR1802G-SH2-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) SH2: HSOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



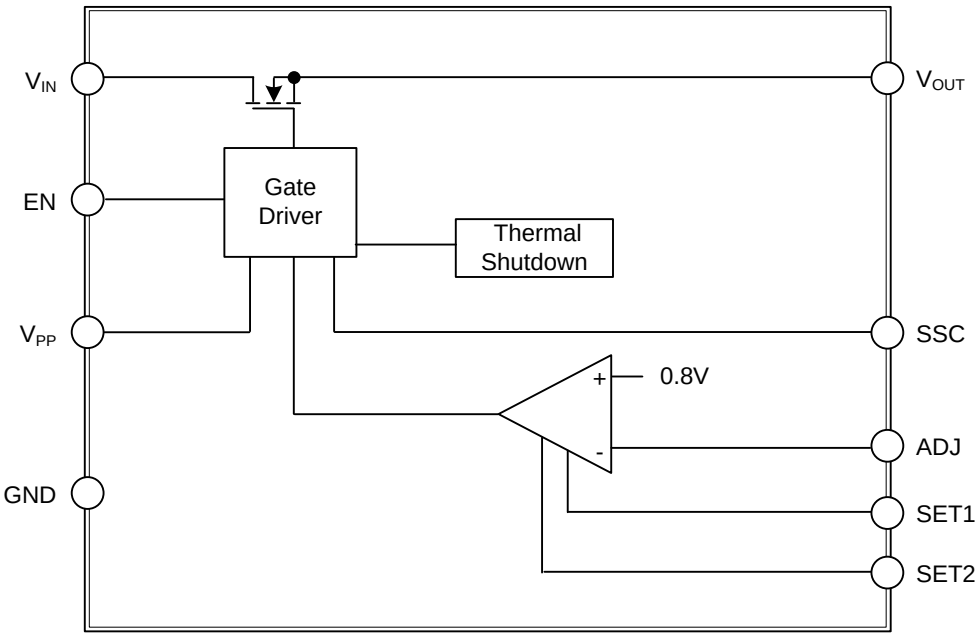
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V_{IN}	Input voltage. Large bulk capacitance should be placed closely to this pin, A 10uF ceramic capacitor is recommended at this pin
2	V_{PP}	Input voltage for controlling circuit
3	SET1	Output voltage setting pin. Pull-high: 1, Pull-Low; 0
4	SET2	Output voltage setting pin. Pull-high: 1, Pull-Low; 0
5	EN	Enable input. Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. The device will be disabled if this pin is left open
6	SSC	Inrush current limit pin
7	ADJ	Resistor ratio of external feedback for output voltage by VO=0.8*(R1+R2)/R2 Volts
8	V_{OUT}	The power output of the device. A pull low resistance exists when device deactivated by EN pin

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage (V_{PP}, V_{IN}, EN, ADJ, V_{OUT}, SSC, SET1, SET2)	V_{IN}	7	V
Power Dissipation	P_D	Internally limited	W
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	$-65 \le T_J \le +150$	°C
Operation Conditions			
V_{IN} Voltage	V_{IN}	1.0 ~ 5.5	V
V_{PP} Voltage	V_{PP}	3 ~ 5.5	V
($V_{PP} \ge V_{IN}$ for normal operation) Temperature Range	T_{OPR}	$-40 \le T_A \le +85$	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction To Ambient	θ_{JA}	143	°C/W

■ ELECTRICAL CHARACTERISTICS

V_{PP}=5V, V_{IN} =3.3V, V_{EN}=V_{PP}, I_{OUT} =10mA, C_{IN}=10µF, C_{OUT} =10µF, T_A=T_J=25°C
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/ of MAX limits are 100% tested at +25°C unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}						
Input Voltage Range	V_{IN}	V_{IN}>V_O	1.0		5.5	V
V_{PP}						
V_{PP} Voltage Range	V_{PP}	V_{PP}>V_O+1V and V_{PP}>3V	3		5.5	V
V_{OUT}						
Output Voltage	V_O	Externally set voltage V_{IN}=V_O+0.5V $V_{O(S)}$: V_O Voltage setting	$V_{O(S)}$-3%	$V_{O(S)}$	$V_{O(S)}$+3%	V
Line Regulation		V_{IN}=(V_O+0.5V)~5V, I_{OUT}=100mA ($\Delta V_{OUT}/\Delta V_{IN}$*$V_{OUT}$		0.8		%/v
Ripple ejection		f=1kHz		70		dB
Load Regulation		10mA≤I_O≤1A		0.6		%
Dropout Voltage	V_D	I_O=1A, V_O=1.8V		300		mV
Short Circuit Current				500		mA
V_{OUT} Pull Low Resistance		V_{EN}=0V		60		Ω
V_{OUT}						
Soft Start Time	T_{SS}	C_{SS}: Capacitor on SSC pin V_{IN}=V_O+1V, I_{OUT}=1A, C_{SS}=3nF Time period when V_{SSC} rises from 0~0.8V		0.6		mS
		C_{SS}: Capacitor on SSC pin V_{IN}=V_O+1V, I_{OUT}=1A, C_{SS}=0nF Time period when V_{SSC} rises from 0~0.8V		0.06		mS

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADJ						
Reference Voltage	V_{REF}	V_{ADJ}= V_O	0.784	0.8	0.816	V
Adjust Pin Current	I_{ADJ}				100	nA
EN						
EN Pin Voltage High	V_{ENH}		1.6			V
EN Pin Voltage Low	V_{ENL}				0.4	V
EN Pin Down Resistor	R_{EN}			2.0		MΩ
SET1, SET2						
SET1, SET2 Pin Voltage High	V_{SET1H}, V_{SET2H}		V_{PP}-0.5			V
SET1, SET2 Pin Voltage Low	V_{SET1L}, V_{SET2L}				0.5	V
Over Temperature Protection						
Over Temperature	T_{OT}			150		°C
Over Temperature Hysteresis	T_{OTHY}			30		°C

■ OUTPUT VOLTAGE SETTING OPTION

Internal V_O setting table:

SET1	SET2	V_{OUT}
0	0	0.9
0	F	1.05
0	1	1.2
F	0	1.5
F	F	ADJ mode
F	1	1.5
1	0	1.8
1	F	2.5
1	1	3.3

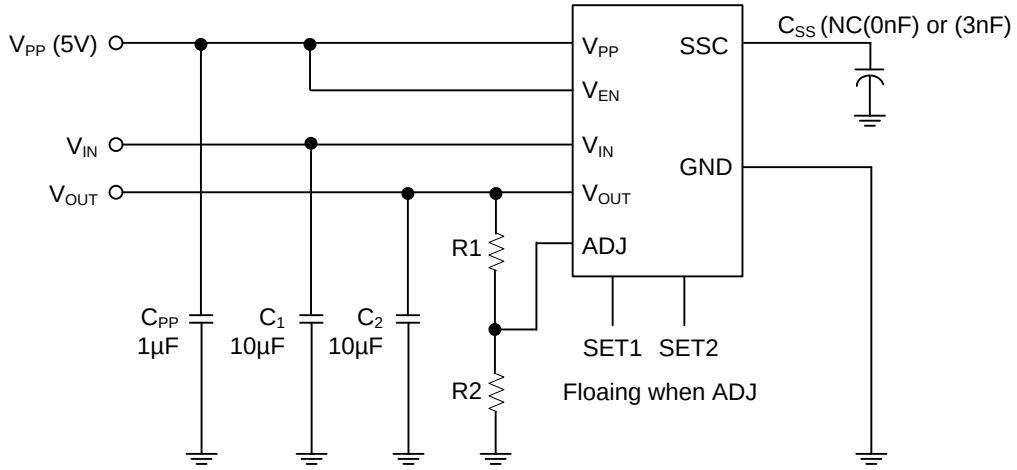
* 0: pin voltage low, 1: pin voltage high, F: pin floating

External V_O setting:

V_O={(R1+R2)/R2}*V_{ADJ}

* If ADJ pin is connected to gnd, V_O follows internal V_O setting
* ADJ pin has the priority than set1 pin and set2 pin

■ TYPICAL APPLICATION CIRCUIT



$$V_{OUT}=\frac{0.8(R1+R2)}{R2}\text{Volts}$$

R2<120KΩ is recommended